



QUALITY SEMICONDUCTOR, INC.

**October
1991**



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DATABOOK

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SRAM
FIFO
FCT
QUICKSWITCH™

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with the instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component of a life support device or system is one whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Data Sheet Identification	Product Status	Definition
Advance Information	In Design or Prototype	This data sheet contains the key specifications for product development. The specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data may be published at a later date. QSI reserves the right to make changes to these specifications at any time without notice in order to improve the design and supply the best possible product.
(none)	Full Production	This data sheet contains final specifications. QSI reserves the right to make changes to these specifications at any time without notice in order to improve the design and supply the best possible product.

GENERAL INFORMATION

PRODUCT SELECTOR GUIDE

SRAM

Part No.	Density	Organization	Features	Availability
8768	16K	4Kx4	Common I/O	1Q92
8769	16K	4Kx4	Fast Chip Select	1Q92
8780	16K	4Kx4	Cache Tag	1Q92
88160	128K	8Kx16	Cache Data RAM	2Q92
88180	144K	8Kx18	Cache Data RAM	2Q92
88181	144K	8Kx18	Burst Mode SRAM	2Q92
88182	144K	8Kx18	Cache Tag RAM	2Q92
83280	256K	32Kx8	Common I/O	2Q92
83283	256K	32Kx8	Fast Address bit	2Q92
83285	256K	32Kx8	Low Power	NOW
83289	256K	32Kx8	Fast Chip Select	2Q92
83290	288K	32Kx9	Common I/O	2Q92
83291	288K	32Kx9	Burst Mode	2Q92
86440	256K	64Kx4	Common I/O	2Q92
86442	256K	64Kx4	Cache Tag	2Q92
86444	256K	64Kx4	Separate I/O	2Q92
86446	256K	64Kx4	Output Enable	2Q92
86447	256K	64Kx4	Address Latch	2Q92
86448	256K	64Kx4	Address Register	2Q92
86449	256K	64Kx4	Separate I/O	2Q92
812880	1024K	128Kx8	Common I/O	4Q92
8881	64K	16Kx4	Separate I/O	NOW
8882	64K	16Kx4	Separate I/O	NOW
8883	64K	16Kx4	Cache Tag	NOW
8885	64K	16Kx4	Output Enable, 2 CS	NOW
8886	64K	16Kx4	Output Enable	NOW
8888	64K	16Kx4	22-pin, 12 ns	NOW

FIFO

Part No.	Density	Organization	Features	Availability
7201	4K	512x9	15 ns	NOW
7202	8K	1Kx9	15 ns	NOW
7203	16K	2Kx9	15 ns	1Q92
7204	32K	4Kx9	15 ns	1Q92
7211	4K	512x9	15 ns, OE	4Q91
7212	8K	1Kx9	15 ns, OE	4Q91
7223	16K	2Kx9	50Mhz, clocked	1Q92
7229	32K	4Kx9	50Mhz, clocked	1Q92
7306	256K	64Kx4	50Mhz, clocked	2Q92
7316	256K	64Kx4	Burst Mode Dual Port	2Q92

GENERAL INFORMATION

PRODUCT SELECTOR GUIDE - Continued

FCT Logic

Std.	25Ω	Function	Common NO	Bits	Invert	Availability
Part No.	Part No.					
240	2240	Buffer	Cache Data RAM	8	X	NOW
241	2241	Buffer	Cache Data RAM	8		NOW
244	2244	Buffer	Cache Data RAM	8		NOW
540	2540	Buffer	Cache Tag RAM	8	X	NOW
541	2541	Buffer	Cache Tag RAM	8		NOW
827	2827	Buffer	Common NO	10		NOW
828	2828	Buffer	Cache Tag RAM	10	X	NOW
373	2373	Latch	Cache Tag RAM	8		NOW
533	2533	Latch	Cache Tag RAM	8	X	NOW
841	2841	Latch	Cache Tag RAM	10		NOW
843	2843	Latch	Cache Tag RAM	9		NOW
845	2845	Latch	Cache Tag RAM	8		NOW
273	2273	Register with Clear	Cache Tag RAM	8		NOW
374	2374	Register	Cache Tag RAM	8		NOW
377	2377	Register with Clock Enable	Cache Tag RAM	8	X	NOW
534	2534	Register	Cache Tag RAM	8		NOW
821	2821	Register	Cache Tag RAM	10		NOW
823	2823	Register	Cache Tag RAM	9		NOW
825	2825	Register	Cache Tag RAM	8		NOW
29520	292520	Pipeline Registers	Cache Tag RAM	8		NOW
29521	292521	Pipeline Registers	Cache Tag RAM	8		NOW
245	2245	Transceiver	Cache Tag RAM	8		NOW
833	2833	Transceiver w/ Reg. Parity	Cache Tag RAM	8		NOW
853	2853	Transceiver with Latched Parity	Cache Tag RAM	8		NOW
861	2861	Transceiver	Cache Tag RAM	10		NOW
862	2862	Transceiver	Cache Tag RAM	10	X	NOW
863	2863	Transceiver	Cache Tag RAM	9		NOW
864	2864	Transceiver	Cache Tag RAM	9	X	NOW

Std.	25Ω	Function	Common NO	Bits	Invert	Availability
Part No.	Part No.					
7501	7201	Transceiver	Cache Tag RAM	4K		NOW
7502	7202	Transceiver	Cache Tag RAM	8K		NOW
7503	7203	Transceiver	Cache Tag RAM	16K		NOW
7504	7204	Transceiver	Cache Tag RAM	32K		NOW
7511	7211	Transceiver	Cache Tag RAM	4K		NOW
7512	7212	Transceiver	Cache Tag RAM	8K		NOW
7523	7223	Transceiver	Cache Tag RAM	16K		NOW
7524	7224	Transceiver	Cache Tag RAM	32K		NOW
7506	7206	Transceiver	Cache Tag RAM	4K		NOW
7516	7216	Transceiver	Cache Tag RAM	8K		NOW

GENERAL INFORMATION

FCT Logic - Continued

Std.	25Ω				
Part No.	Part No.	Function	Bits	Invert	Availability
543	2543	Latch Transceiver	8		NOW
544	2544	Latch Transceiver	8	X	NOW
2952	292052	Registered Transceiver	8		NOW
2953	292053	Registered Transceiver	8	X	NOW
646	2646	Registered Transceiver	8		NOW
648	2648	Registered Transceiver	8	X	NOW
651	2651	Registered Transceiver	8		NOW
652	2652	Registered Transceiver	8	X	NOW
138	-	3-8 Decoder, Neg Out		X	NOW
139	-	Dual 2-4 Decoder, Neg Out		X	NOW
238	-	3-8 Decoder, Pos Out			NOW
239	-	Dual 2-4 Decoder, Pos Out			NOW
151	2151	8-input Multiplexer	1		NOW
153	2153	Dual 4-input Multiplexer	2		NOW
157	2157	Quad 2-input Multiplexer	4		NOW
158	2158	Quad 2-input Multiplexer	4	X	NOW
161	2161	4-bit Synchronous Counter	4		NOW
163	2163	4-bit Synchronous Counter	4		NOW
191	2191	4-bit Up/Down Counter	4		1Q92
193	2193	4-bit Up/Down Counter	4		1Q92
299	2299	8-bit Universal Shift Register	8		1Q92
280	-	Parity Generator	9	-	NOW
521	-	Identity Comparator	8	-	NOW
1280	-	Registered Parity Generator	9	-	NOW

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GENERAL INFORMATION

FCT Logic - Continued

Part No.	Pin	Function	Pin	Power	Availability
1580	-	Registered Parity Generator	9	-	NOW
821	-	Identity Comparator	8	-	NOW
280	-	Parity Generator	9	-	NOW
259	2599	8-bit Universal Shift Register	8	-	1Q82
193	2193	4-bit Up/Down Counter	4	-	1Q82
191	2191	4-bit Up/Down Counter	4	-	1Q82
183	2183	4-bit Synchronous Counter	4	-	NOW
181	2181	4-bit Synchronous Counter	4	-	NOW
189	2189	Quad 2-input Multiplexer	4	X	NOW
157	2157	Quad 2-input Multiplexer	4	-	NOW
153	2153	Dual 4-input Multiplexer	2	-	NOW
151	2151	8-input Multiplexer	1	-	NOW
239	-	Dual 2-4 Decoder, Pos Out	-	-	NOW
238	-	3-8 Decoder, Pos Out	-	-	NOW
139	-	Dual 2-4 Decoder, Neg Out	-	X	NOW
138	-	3-8 Decoder, Neg Out	-	X	NOW
882	2882	Registered Transceiver	8	X	NOW
881	2881	Registered Transceiver	8	-	NOW
918	2818	Registered Transceiver	8	X	NOW
848	2848	Registered Transceiver	8	-	NOW
2923	2823	Registered Transceiver	8	X	NOW
2922	2822	Registered Transceiver	8	-	NOW
244	2844	Latch Transceiver	8	X	NOW
243	2843	Latch Transceiver	8	-	NOW

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NUMERICAL PRODUCT INDEX

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29FCT2053	29FCT52	Register Transceiver	8	X	X	4-27
29FCT2520	29FCT520	Pipeline Register	8		X	4-35
29FCT2521	29FCT520	Pipeline Register	8		X	4-35
29FCT52	29FCT52	Register Transceiver	8			4-27
29FCT520	29FCT520	Pipeline Register	8			4-35
29FCT521	29FCT520	Pipeline Register	8			4-35
29FCT53	29FCT52	Register Transceiver	8	X		4-27
FCT1280	FCT280	Parity Generator/Checker	9			4-115
FCT138	FCT138	3->8 Decoder, Neg Output	3	X		4-43
FCT139	FCT138	Dual 2->4 Decoder, Neg Output	2	X		4-43
FCT151	FCT151	8-input Multiplexer	1			4-55
FCT153	FCT153	Dual 4-input Multiplexer	2			4-61
FCT157	FCT157	Quad 2-input Multiplexer	4			4-67
FCT158	FCT157	Quad 2-input Multiplexer	4	X		4-67
FCT161	FCT161	4-bit Synchronous Counter	4			4-73
FCT163	FCT161	4-bit Synchronous Counter	4			4-73
FCT191	FCT191	4-bit Up/Down Counter	4			4-81
FCT193	FCT193	4-bit Up/Down Counter	4			4-89
FCT2151	FCT151	8-input Multiplexer	1	X		4-55
FCT2153	FCT153	Dual 4-input Multiplexer	2	X		4-61
FCT2157	FCT157	Quad 2-input Multiplexer	4	X		4-67
FCT2158	FCT157	Quad 2-input Multiplexer	4	X	X	4-67
FCT2161	FCT161	4-bit Synchronous Counter	4	X		4-73
FCT2163	FCT161	4-bit Synchronous Counter	4	X		4-73
FCT2191	FCT191	4-bit Up/Down Counter	4	X		4-81
FCT2193	FCT193	4-bit Up/Down Counter	4	X		4-89
FCT2240	FCT240	Buffer	8	X	X	4-97
FCT2241	FCT240	Buffer	8		X	4-97
FCT2244	FCT240	Buffer	8		X	4-97
FCT2245	FCT245	Transceiver	8		X	4-103
FCT2273	FCT273	Register with Clear	8	X		4-109
FCT2299	FCT299	8-bit Universal Shift Register	8	X		4-123
FCT2373	FCT373	Latch	8	X		4-129
FCT2374	FCT374	Register	8	X		4-135
FCT2377	FCT377	Register with Clock Enable	8	X		4-141
FCT238	FCT138	3->8 Decoder, Pos Output	3			4-43
FCT239	FCT139	Dual 2->4 Decoder, Pos Output	2			4-49
4-178		Register Transceiver	8			
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4-187		Register Transceiver	8			
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			Bits	Invert	25Ω	
FCT240	FCT240	Buffer	8	X		4-97
FCT241	FCT240	Buffer	8			4-97
FCT244	FCT240	Buffer	8			4-97
FCT245	FCT245	Transceiver	8			4-103
FCT2540	FCT540	Buffer	8		X	4-153
FCT2541	FCT540	Buffer	8		X	4-153
FCT2543	FCT543	Latch Transceiver	8		X	4-159
FCT2544	FCT543	Latch Transceiver	8	X	X	4-159
FCT2573	FCT573	Latch	8			4-167
FCT2574	FCT574	Register	8		X	4-173
FCT2646	FCT646	Register Transceiver	8		X	4-179
FCT2648	FCT646	Register Transceiver	8	X	X	4-179
FCT2651	FCT651	Register Transceiver	8	X	X	4-187
FCT2652	FCT651	Register Transceiver	8		X	4-187
FCT273	FCT273	Register with Clear	8			4-109
FCT280	FCT280	Parity Generator/Checker	9			4-115
FCT2821	FCT821	Register	10		X	4-195
FCT2823	FCT821	Register	9		X	4-195
FCT2825	FCT821	Register	8		X	4-195
FCT2827	FCT827	Buffer	10		X	4-205
FCT2828	FCT827	Buffer	10	X	X	4-205
FCT2833	FCT833	Transceiver w/ Reg. Parity	8		X	4-211
FCT2841	FCT841	Latch	10		X	4-213
FCT2843	FCT841	Latch	9		X	4-213
FCT2845	FCT841	Latch	8		X	4-213
FCT2853	FCT853	Transceiver w/ Latched Parity	8		X	4-211
FCT2861	FCT861	Transceiver	10		X	4-223
FCT2862	FCT861	Transceiver	10	X	X	4-223
FCT2863	FCT861	Transceiver	9		X	4-223
FCT2864	FCT861	Transceiver	9	X	X	4-223
FCT299	FCT299	8-bit Universal Shift Register	8			4-123
FCT373	FCT373	Latch	8			4-129
FCT374	FCT374	Register	8			4-135
FCT377	FCT377	Register with Clock Enable	8			4-141
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FCT544	FCT543	Latch Transceiver	8	X		4-159
FCT573	FCT573	Latch	8			4-167
FCT574	FCT574	Register	8			4-173
FCT646	FCT646	Register Transceiver	8			4-179
FCT648	FCT646	Register Transceiver	8	X		4-179
FCT651	FCT651	Register Transceiver	8	X		4-187
FCT652	FCT651	Register Transceiver	8			4-187
FCT821	FCT821	Register	10			4-195
FCT823	FCT821	Register	9			4-195
FCT825	FCT821	Register	8			4-195
FCT827	FCT827	Buffer	10			4-205
FCT828	FCT827	Buffer	10	X		4-205
FCT833	FCT833	Transceiver w/ Reg. Parity	8			4-211

GENERAL INFORMATION

Part No.	Data Sheet	Description	Output Drive			Page
			Bits	Invert	25Ω	
FCT841	FCT841	Latch	10			4-213
FCT843	FCT841	Latch	9			4-213
FCT845	FCT841	Latch	8			4-213
FCT853	FCT833	Transceiver with Latched Parity	8			4-211
FCT861	FCT861	Transceiver	10			4-223
FCT862	FCT861	Transceiver	10	X		4-223
FCT863	FCT861	Transceiver	9			4-223
FCT864	FCT861	Transceiver	9	X		4-223
Part No.	Data Sheet	Description	Bits	Density		Page
QS7201	QS7201	512 X 9 FIFO	9	4.5 K		3-5
QS7202	QS7201	1K X 9 FIFO	9	9K		3-5
QS7203	QS7204	2 X 9 FIFO	9	18K		3-21
QS7204	QS7204	4K X 9 FIFO	9	36K		3-21
QS7211	QS7211	512 X 9 FIFO with OE	9	4.5K		3-39
QS7212	QS7211	1K X 9 FIFO with OE	9	9K		3-39
QS7223	QS7224	2K X 9 FIFO, Clocked I/F	9	18K		3-53
QS7224	QS7224	4K X 9 FIFO, Clocked I/F	9	36K		3-53
QS7306	QS7306	64K X 4 FIFO, Clocked I/F	4	256K		3-67
QS7316	QS7316	64K X 4 Burst Mode Dual Port RAM	4	256K		3-69
Part No.	Data Sheet	Description	Bits	Density		Page
QST3353	QST3353	QuickSwitch Bus Exchange	10			5-17
QST3354	QST3354	QuickSwitch Bus Connect	10			5-23
QST3355	QST3355	QuickSwitch Bus Exchange	10			5-17
QST3356	QST3356	QuickSwitch Bus Connect	10			5-23

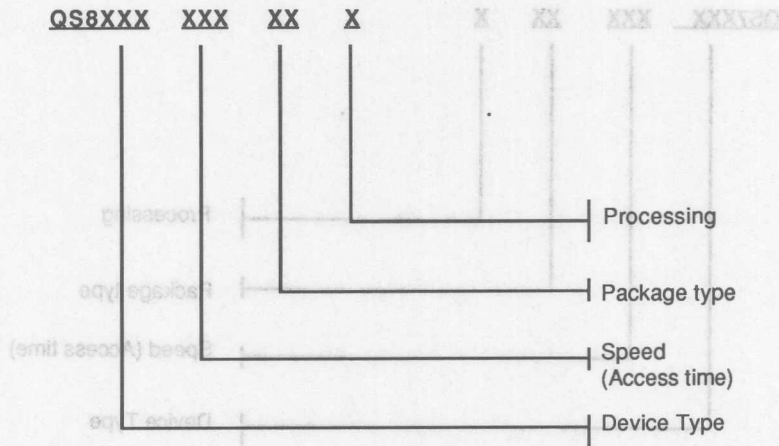
GENERAL INFORMATION

Part No.	Data Sheet	Description	Bits	Density	Page	
QS812880	QS812880	128Kx8 SRAM	8	1024K	2-129	
QS8768	QS8768	4Kx4 SRAM	4	16K	2-5	
QS8769	QS8769	4Kx4 SRAM Fast Chip Select	4	16K	2-13	
QS8780	QS8780	4Kx4 Cache Tag RAM with Reset	4	16K	2-21	
QS83280	QS83280	32Kx8 SRAM	8	256K	2-81	
QS83283	QS83283	32Kx8 SRAM, Fast Address Bit	8	256K	2-89	
QS83285	QS83285	32Kx8 SRAM, Low Power	8	256K	2-91	
QS83289	QS83289	32Kx8 SRAM, Fast Chip Select	8	256K	2-99	
QS83290	QS83290	32Kx9 SRAM	9	288K	2-101	
QS83291	QS83291	32Kx9 SRAM, Burst Mode	9	288K	2-103	
QS86440	QS86440	64Kx4 SRAM, Common I/O	4	256K	2-105	
QS86442	QS86442	64Kx4 SRAM, Cache Tag	4	256K	2-113	
QS86444	QS86444	64Kx4 SRAM, Separate I/O	4	256K	2-115	
QS86446	QS86446	64Kx4 SRAM, Output Enable	4	256K	2-117	
QS86447	QS86447	64Kx4 SRAM, Address Latch	4	256K	2-125	
QS86448	QS86448	64Kx4 SRAM, Address Register	4	256K	2-127	
QS86449	QS86444	64Kx4 SRAM, Separate I/O	4	256K	2-115	
QS88160	QS88180	8Kx16 Cache Data SRAM	16	128K	2-67	
QS88180	QS88180	8Kx18 Cache Data SRAM	18	128K	2-67	
QS88181	QS88181	8Kx18 Burst Mode SRAM	18	144K	2-77	
QS88182	QS88182	8Kx18 Cache Tag SRAM	18	144K	2-79	
QS8881	QS8881	16Kx4 SRAM, Separate I/O	4	64K	2-31	
QS8882	QS8881	16Kx4 SRAM, Separate I/O	4	64K	2-31	
QS8883	QS8883	16Kx4 SRAM, Tag	4	64K	2-41	
QS8885	QS8886	16Kx4 SRAM, OE	4	64K	2-51	
QS8886	QS8886	16Kx4 SRAM, OE, 2 CS	4	64K	2-51	
QS8888	QS8888	16Kx4 SRAM, 22 pin	4	64K	2-59	
Output Drive						
Part No.	Data Sheet	Description	Bits	Invert	25Ω	Page
QST3383	QST3383/53	QuickSwitch Bus Exchange	10			5-17
QST3384	QST3384/54	QuickSwitch Bus Connect	10		X	5-23
QST3353	QST3383/53	QuickSwitch Bus Exchange	10			5-17
QST3354	QST3384/54	QuickSwitch Bus Connect	10		X	5-23

GENERAL INFORMATION

ORDERING INFORMATION

SRAM



1

Processing:

Blank - Standard Commercial, 0-70 °C
 B - MIL-STD 883, -55°C to +125 °C
 M - Commercial, -55°C to +125 °C

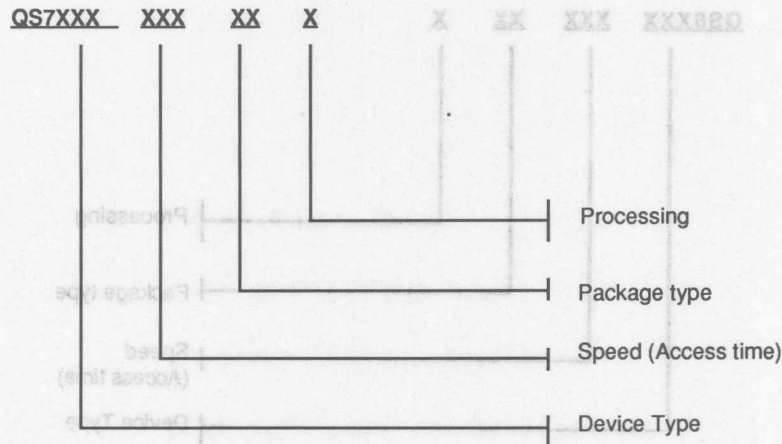
Package Type:

P - Plastic DIP, 300 mil
 D - Ceramic DIP, 300 mil
 L - Leadless Ceramic Chip Carrier
 SO - Small Outline IC, 300 mil
 S1 - Small Outline IC, 150 mil
 Z - Plastic ZIP
 Q - QSOP, Quarter Size Outline Package, 150 mil

GENERAL INFORMATION

ORDERING INFORMATION

FIFO



Processing:

Blank - Standard Commercial, 0-70 °C
 B - MIL-STD 883, -55°C to +125 °C
 M - Commercial, -55°C to +125 °C

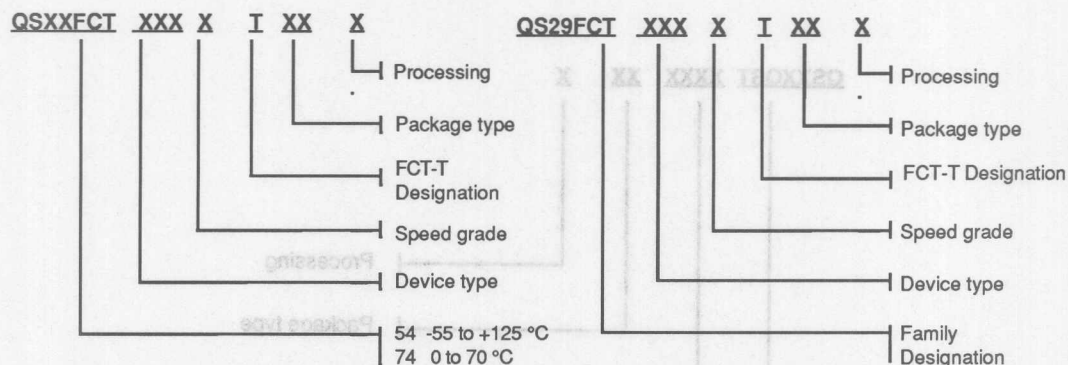
Package Type:

P - Plastic DIP, 300 mil
 D - Ceramic DIP, 300 mil
 L - Leadless Ceramic Chip Carrier
 SO - Small Outline IC, 300 mil
 S1 - Small Outline IC, 150 mil
 Z - Plastic ZIP
 Q - QSOP, Quarter Size Outline Package, 150 mil

GENERAL INFORMATION

ORDERING INFORMATION

29FCT-T



Speed Grades:

Blank - Standard

A
B
C
D

Processing:

Blank - Standard Commercial, 0-70 °C
B - MIL-STD 883 Military -55°C to +125 °C
M - Commercial, -55°C to +125 °C (29FCT Only)

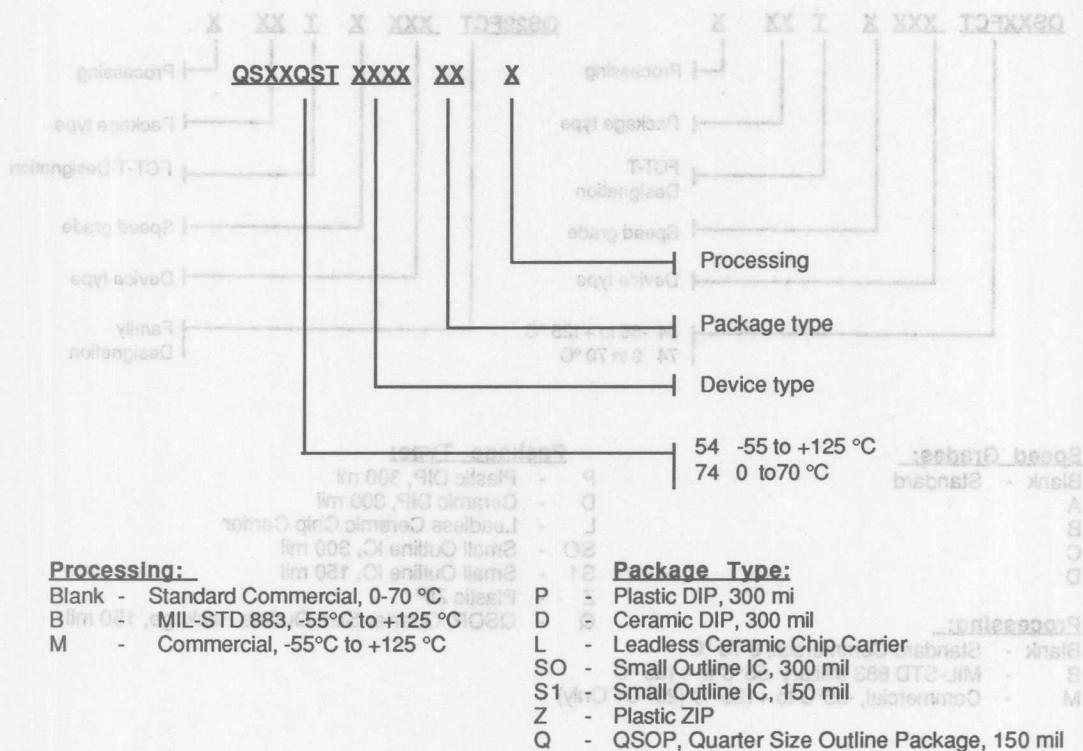
Package Type:

P - Plastic DIP, 300 mil
D - Ceramic DIP, 300 mil
L - Leadless Ceramic Chip Carrier
SO - Small Outline IC, 300 mil
S1 - Small Outline IC, 150 mil
Z - Plastic ZIP
Q - QSOP, Quarter Size Outline Package, 150 mil

GENERAL INFORMATION

ORDERING INFORMATION

QUICKSWITCH



Cross Reference

STATIC RAM

IDT	QSI	IDT (continued)	QSI (continued)
IDT6168LA-10	QS8768-10	IDT71682-25	QS8762-25
IDT6168LA-12	QS8768-12	IDT71682-35	QS8762-35
IDT6168LA-15	QS8768-15	IDT7188L15	QS8888-15
IDT6168LA-20	QS8768-20	IDT7188L20	QS8888-20
IDT6168LA-25	QS8768-25	IDT7188L25	QS8888-25
IDT6168LA-35	QS8768-35	IDT7188L35	QS8888-35
IDT6168SA-10	QS8768-10	IDT7188S15	QS8888-15
IDT6168SA-12	QS8768-12	IDT7188S20	QS8888-20
IDT6168SA-15	QS8768-15	IDT7188S25	QS8888-25
IDT6168SA-20	QS8768-20	IDT7188S35	QS8888-35
IDT6168SA-25	QS8768-25	IDT71981S15	QS8881-15
IDT6168SA-35	QS8768-35	IDT71981S20	QS8881-20
IDT6178S-12	QS8780-12	IDT71981S25	QS8881-25
IDT6178S-15	QS8780-15	IDT71981S35	QS8881-35
IDT6178S-20	QS8780-20	IDT71982S15	QS8882-15
IDT6178S-25	QS8780-25	IDT71982S20	QS8882-20
IDT6198L15	QS8886-15	IDT71982S25	QS8882-25
IDT6198L20	QS8886-20	IDT71982S35	QS8882-35
IDT6198L25	QS8886-25	IDT7198L15	QS8885-15
IDT6198L35	QS8886-35	IDT7198L20	QS8885-20
IDT6198S15	QS8886-15	IDT7198L25	QS8885-25
IDT6198S20	QS8886-20	IDT7198L35	QS8885-35
IDT6198S25	QS8886-25	IDT7198S15	QS8885-15
IDT6198S35	QS8886-35	IDT7198S20	QS8885-20
IDT61B98-10	QS8886-10	IDT7198S25	QS8885-25
IDT61B98-12	QS8886-12	IDT7198S35	QS8885-35
IDT71256L-15	QS83280-15	IDT71B256-15	QS83280-15
IDT71256L-20	QS83280-20	IDT71B256-20	QS83280-20
IDT71256L-25	QS83280-25	IDT71B258S-15	QS86440-15
IDT71256L-30	QS83280-30	IDT71B258S-20	QS86440-20
IDT71256L-45	QS83280-45		
IDT71256S-15	QS83280-15		
IDT71256S-20	QS83280-20		
IDT71256S-25	QS83280-25		
IDT71256S-30	QS83280-30		
IDT71256S-45	QS83280-45		
IDT71258L-15	QS86440-15		
IDT71258L-20	QS86440-20		
IDT71258L-25	QS86440-25		
IDT71258L-35	QS86440-35		
IDT71258S-15	QS86440-15		
IDT71258S-20	QS86440-20		
IDT71258S-25	QS86440-25		
IDT71258S-35	QS86440-35		
IDT71681-10	QS8761-10		
IDT71681-12	QS8761-12		
IDT71681-15	QS8761-15		
IDT71681-20	QS8761-20		
IDT71681-25	QS8761-25		
IDT71681-35	QS8761-35		
IDT71682-10	QS8762-10		
IDT71682-12	QS8762-12		
IDT71682-15	QS8762-15		
IDT71682-20	QS8762-20		

CYPRESS

CY7C161-20
 CY7C161-25
 CY7C161-35
 CY7C161A-15
 CY7C161A-20
 CY7C161A-25
 CY7C161A-35
 CY7C162-20
 CY7C162-25
 CY7C162-35
 CY7C162A-15
 CY7C162A-20
 CY7C162A-25
 CY7C162A-35
 CY7C164-15
 CY7C164-20
 CY7C164-25
 CY7C164-35
 CY7C164A-15
 CY7C164A-20

QSI

QS8881-20
 QS8881-25
 QS8881-35
 QS8881-15
 QS8881-20
 QS8881-25
 QS8881-35
 QS8882-20
 QS8882-25
 QS8882-35
 QS8882-15
 QS8882-20
 QS8882-25
 QS8882-35
 QS8888-15
 QS8888-20
 QS8888-25
 QS8888-35
 QS8888-15
 QS8888-20

STATIC RAM

1-18

Cross Reference

STATIC RAM

MICRON (Continued)	QSI	PERFORMANCE (Continued)	QSI
MCM6269-35	QS8769-35	P4C188-15	QS8888-15
MCM6288-12	QS8888-12	P4C188-20	QS8888-20
MCM6288-15	QS8888-15	P4C188-25	QS8888-25
MCM6288-20	QS8888-20	P4C188-35	QS8888-35
MCM6288-25	QS8888-25	P4C198-15	QS8886-15
MCM6288-35	QS8888-35	P4C198-20	QS8886-20
MCM6290-12	QS8886-12	P4C198-25	QS8886-25
MCM6290-15	QS8886-15	P4C198-35	QS8886-35
MCM6290-20	QS8886-20	P4C1981-15	QS8881-15
MCM6290-25	QS8886-25	P4C1981-20	QS8881-20
MCM6290-35	QS8886-35	P4C1981-25	QS8881-25
		P4C1982-15	QS8882-15
		P4C1982-20	QS8882-20
		P4C1982-25	QS8882-25
		P4C198A-15	QS8885-15
		P4C198A-20	QS8885-20
		P4C198A-25	QS8885-25
PERFORMANCE	QSI	TI	QSI
P4C1258-20	QS86440-20	SN74ACT2140A	QS88180-25
P4C1258-25	QS86440-25		
P4C1258-35	QS86440-35		
P4C168-12	QS8768-12		
P4C168-15	QS8768-15		
P4C168-20	QS8768-20		
P4C168-25	QS8768-25		
P4C168-35	QS8768-35		
P4C1681-12	QS8761-12		
P4C1681-15	QS8761-15		
P4C1681-20	QS8761-20		
P4C1681-25	QS8761-25		
P4C1681-35	QS8761-35		
P4C1682-12	QS8762-12		
P4C1682-15	QS8762-15		
P4C1682-20	QS8762-20		
P4C1682-25	QS8762-25		
P4C1682-35	QS8762-35		
		TOSHIBA	QSI
		TC55416-15	QS8888-15
		TC55416-20	QS8888-20
		TC55416-25	QS8888-25
		TC55416-35	QS8888-35
		TC55417-15	QS8886-15
		TC55417-20	QS8886-20
		TC55417-25	QS8886-25
		TC55417-35	QS8886-35

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Cross Reference

FIFO

MOSTEK	QSI	ISI	QMA
MK4501-65	QS7201-50	Q87501-80	Q87501-80
MK4501-80	QS7201-80	Q87501-80	Q87501-80
MK4501-120	QS7201-80	Q87501-80	Q87501-80
MK4503A-15	QS7203-15	Q87501-80	Q87501-80
MK4503A-25	QS7203-25	Q87501-80	Q87501-80
MK4503A-35	QS7203-35	Q87501-80	Q87501-80
MK4503A-50	QS7203-50	Q87501-80	Q87501-80
SAMSUNG		QMA	
KM75C01-15	QS7201-15	Q87501-80	Q87501-80
KM75C01-20	QS7201-20	Q87501-80	Q87501-80
KM75C01-25	QS7201-25	Q87501-80	Q87501-80
KM75C01-35	QS7201-35	Q87501-80	Q87501-80
KM75C01-50	QS7201-50	Q87501-80	Q87501-80
KM75C01-80	QS7201-80	Q87501-80	Q87501-80
KM75C02-15	QS7202-15	Q87501-80	Q87501-80
KM75C02-20	QS7202-20	Q87501-80	Q87501-80
KM75C02-25	QS7202-25	Q87501-80	Q87501-80
KM75C02-35	QS7202-35	Q87501-80	Q87501-80
KM75C02-50	QS7202-50	Q87501-80	Q87501-80
KM75C02-80	QS7202-80	Q87501-80	Q87501-80
SHARP		QMA	
LH5496-15	QS7201-15	Q87501-80	Q87501-80
LH5496-20	QS7201-20	Q87501-80	Q87501-80
LH5496-25	QS7201-25	Q87501-80	Q87501-80
LH5496-35	QS7201-35	Q87501-80	Q87501-80
LH5496-50	QS7201-50	Q87501-80	Q87501-80
LH5496-80	QS7201-80	Q87501-80	Q87501-80
LH5497-20	QS7202-20	Q87501-80	Q87501-80
LH5497-25	QS7202-25	Q87501-80	Q87501-80
LH5497-35	QS7202-35	Q87501-80	Q87501-80
LH5497-50	QS7202-50	Q87501-80	Q87501-80
LH5498A-15	QS7203-15	Q87501-80	Q87501-80
LH5498A-25	QS7203-25	Q87501-80	Q87501-80
LH5498A-35	QS7203-35	Q87501-80	Q87501-80
LH5498A-50	QS7203-50	Q87501-80	Q87501-80
LH5499A-15	QS7204-15	Q87501-80	Q87501-80
LH5499A-25	QS7204-25	Q87501-80	Q87501-80
LH5499A-35	QS7204-35	Q87501-80	Q87501-80
LH5499A-50	QS7204-50	Q87501-80	Q87501-80

Cross Reference

FCT-T LOGIC

HARRIS	QSI (Continued)	IDT (Continued)	QSI (Continued)
CD74FCT240	QST4FCT240T	IDT74FCT138A	QS74FCT138AT
CD74FCT241	QST4FCT241T	IDT74FCT138AT	QS74FCT138AT
CD74FCT244	QST4FCT244T	IDT74FCT138C	QS74FCT138CT
CD74FCT245	QST4FCT245T	IDT74FCT138CT	QS74FCT138CT
CD74FCT273	QS74FCT273T	IDT74FCT139	QS74FCT139T
CD74FCT29520A	QS29FCT520AT	IDT74FCT139A	QS74FCT139AT
CD74FCT29521A	QS29FCT521AT	IDT74FCT139AT	QS74FCT139AT
CD74FCT2952A	QS29FCT52AT	IDT74FCT139C	QS74FCT139CT
CD74FCT2953A	QS29FCT53AT	IDT74FCT139CT	QS74FCT139CT
CD74FCT373	QST4FCT373T	IDT74FCT139T	QS74FCT139T
CD74FCT374	QST4FCT374T	IDT74FCT151AT	QS74FCT151AT
CD74FCT377	QS74FCT377T	IDT74FCT151T	QS74FCT151T
CD74FCT533	QS74FCT533T	IDT74FCT157AT	QS74FCT157AT
CD74FCT534	QS74FCT534T	IDT74FCT157T	QS74FCT157T
CD74FCT540	QS74FCT540T	IDT74FCT161	QS74FCT161T
CD74FCT541	QS74FCT541T	IDT74FCT161A	QS74FCT161AT
CD74FCT543	QS74FCT543T	IDT74FCT161AT	QS74FCT161AT
CD74FCT544	QS74FCT544T	IDT74FCT161T	QS74FCT161T
CD74FCT573	QS74FCT573T	IDT74FCT163	QS74FCT163T
CD74FCT574	QS74FCT574T	IDT74FCT163A	QS74FCT163AT
CD74FCT640	QS74FCT640T	IDT74FCT163AT	QS74FCT163AT
CD74FCT646	QS74FCT646T	IDT74FCT163T	QS74FCT163T
CD74FCT648	QS74FCT648T	IDT74FCT191	QS74FCT191T
CD74FCT651	QS74FCT651T	IDT74FCT191A	QS74FCT191AT
CD74FCT652	QS74FCT652T	IDT74FCT191AT	QS74FCT191AT
CD74FCT821A	QS74FCT821AT	IDT74FCT191T	QS74FCT191T
CD74FCT823A	QS74FCT823AT	IDT74FCT193	QS74FCT193T
CD74FCT827A	QS74FCT827AT	IDT74FCT193A	QS74FCT193AT
CD74FCT828A	QS74FCT828AT	IDT74FCT193AT	QS74FCT193AT
CD74FCT841A	QS74FCT841AT	IDT74FCT193T	QS74FCT193T
CD74FCT843A	QS74FCT843AT	IDT74FCT240	QST4FCT240T
CD74FCT861A	QS74FCT861AT	IDT74FCT240A	QS74FCT240AT
CD74FCT862A	QS74FCT862AT	IDT74FCT240AT	QS74FCT240AT
CD74FCT863A	QS74FCT863AT	IDT74FCT240C	QS74FCT240CT
CD74FCT864A	QS74FCT864AT	IDT74FCT240CT	QS74FCT240CT
IDT29FCT520A	QS29FCT520AT	IDT74FCT240T	QST4FCT240T
IDT29FCT520AT	QS29FCT520AT	IDT74FCT241	QST4FCT241T
IDT29FCT520B	QS29FCT520BT	IDT74FCT241A	QS74FCT241AT
IDT29FCT520BT	QS29FCT520BT	IDT74FCT241AT	QS74FCT241AT
IDT29FCT521AT	QS29FCT521AT	IDT74FCT241C	QS74FCT241CT
IDT29FCT521BT	QS29FCT521BT	IDT74FCT241CT	QS74FCT241CT
IDT29FCT52A	QS29FCT52AT	IDT74FCT241T	QST4FCT241T
IDT29FCT52AT	QS29FCT52AT	IDT74FCT244	QST4FCT244T
IDT29FCT52B	QS29FCT52BT	IDT74FCT244A	QS74FCT244AT
IDT29FCT52BT	QS29FCT52BT	IDT74FCT244AT	QS74FCT244AT
IDT29FCT53A	QS29FCT53AT	IDT74FCT244C	QS74FCT244CT
IDT29FCT53AT	QS29FCT53AT	IDT74FCT244CT	QS74FCT244CT
IDT29FCT53B	QS29FCT53BT	IDT74FCT244T	QST4FCT244T
IDT29FCT53BT	QS29FCT53BT	IDT74FCT245	QST4FCT245T
IDT74FCT138	QST4FCT138T	IDT74FCT245A	QS74FCT245AT
		IDT74FCT245AT	QS74FCT245AT
		IDT74FCT245C	QS74FCT245CT
		IDT74FCT245CT	QS74FCT245CT

Cross Reference

FCT-T LOGIC

IDT (Continued)	QSI (Continued)	IDT (Continued)	QSI
IDT74FCT245T	QST4FCT245T	IDT74FCT540	QS74FCT540T
IDT74FCT251AT	QS74FCT251AT	IDT74FCT540A	QS74FCT540AT
IDT74FCT251T	QS74FCT251T	IDT74FCT540AT	QS74FCT540AT
IDT74FCT257AT	QS74FCT257AT	IDT74FCT540T	QS74FCT540T
IDT74FCT257T	QS74FCT257T	IDT74FCT541	QS74FCT541T
IDT74FCT273	QS74FCT273T	IDT74FCT541A	QS74FCT541AT
IDT74FCT273A	QS74FCT273AT	IDT74FCT541AT	QS74FCT541AT
IDT74FCT273AT	QS74FCT273AT	IDT74FCT541T	QS74FCT541T
IDT74FCT273C	QS74FCT273CT	IDT74FCT543	QS74FCT543T
IDT74FCT273CT	QS74FCT273CT	IDT74FCT543A	QS74FCT543AT
IDT74FCT273T	QS74FCT273T	IDT74FCT543AT	QS74FCT543AT
IDT74FCT299	QS74FCT299T	IDT74FCT543T	QS74FCT543T
IDT74FCT299A	QS74FCT299AT	IDT74FCT573	QS74FCT573T
IDT74FCT299AT	QS74FCT299AT	IDT74FCT573A	QS74FCT573AT
IDT74FCT299T	QS74FCT299T	IDT74FCT573AT	QS74FCT573AT
IDT74FCT373	QST4FCT373T	IDT74FCT573T	QS74FCT573T
IDT74FCT373A	QS74FCT373AT	IDT74FCT574	QS74FCT574T
IDT74FCT373AT	QS74FCT373AT	IDT74FCT574A	QS74FCT574AT
IDT74FCT373C	QS74FCT373CT	IDT74FCT574AT	QS74FCT574AT
IDT74FCT373CT	QS74FCT373CT	IDT74FCT574T	QS74FCT574T
IDT74FCT373T	QST4FCT373T	IDT74FCT640	QS74FCT640T
IDT74FCT374	QST4FCT374T	IDT74FCT640A	QS74FCT640AT
IDT74FCT374A	QS74FCT374AT	IDT74FCT640AT	QS74FCT640AT
IDT74FCT374AT	QS74FCT374AT	IDT74FCT640C	QS74FCT640CT
IDT74FCT374C	QS74FCT374CT	IDT74FCT640CT	QS74FCT640CT
IDT74FCT374CT	QS74FCT374CT	IDT74FCT640T	QS74FCT640T
IDT74FCT374T	QST4FCT374T	IDT74FCT646	QS74FCT646T
IDT74FCT377	QS74FCT377T	IDT74FCT646A	QS74FCT646AT
IDT74FCT377A	QS74FCT377AT	IDT74FCT646AT	QS74FCT646AT
IDT74FCT377AT	QS74FCT377AT	IDT74FCT646C	QS74FCT646CT
IDT74FCT377C	QS74FCT377CT	IDT74FCT646CT	QS74FCT646CT
IDT74FCT377CT	QS74FCT377CT	IDT74FCT646T	QS74FCT646T
IDT74FCT377T	QS74FCT377T	IDT74FCT648AT	QS74FCT648AT
IDT74FCT521	QS74FCT521T	IDT74FCT648CT	QS74FCT648CT
IDT74FCT521A	QS74FCT521AT	IDT74FCT648T	QS74FCT648T
IDT74FCT521AT	QS74FCT521AT	IDT74FCT651AT	QS74FCT651AT
IDT74FCT521B	QS74FCT521BT	IDT74FCT651T	QS74FCT651T
IDT74FCT521BT	QS74FCT521BT	IDT74FCT652AT	QS74FCT652AT
IDT74FCT521C	QS74FCT521CT	IDT74FCT652T	QS74FCT652T
IDT74FCT521CT	QS74FCT521CT	IDT74FCT821A	QS74FCT821AT
IDT74FCT521T	QS74FCT521T	IDT74FCT821AT	QS74FCT821AT
IDT74FCT533	QS74FCT533T	IDT74FCT821B	QS74FCT821BT
IDT74FCT533A	QS74FCT533AT	IDT74FCT821BT	QS74FCT821BT
IDT74FCT533AT	QS74FCT533AT	IDT74FCT821C	QS74FCT821CT
IDT74FCT533C	QS74FCT533CT	IDT74FCT821CT	QS74FCT821CT
IDT74FCT533CT	QS74FCT533CT	IDT74FCT823A	QS74FCT823AT
IDT74FCT533T	QS74FCT533T	IDT74FCT823AT	QS74FCT823AT
IDT74FCT534	QS74FCT534T	IDT74FCT823B	QS74FCT823BT
IDT74FCT534A	QS74FCT534AT	IDT74FCT823BT	QS74FCT823BT
IDT74FCT534AT	QS74FCT534AT	IDT74FCT823C	QS74FCT823CT
IDT74FCT534C	QS74FCT534CT	IDT74FCT823CT	QS74FCT823CT
IDT74FCT534CT	QS74FCT534CT	IDT74FCT825A	QS74FCT825AT
IDT74FCT534T	QS74FCT534T	IDT74FCT825AT	QS74FCT825AT

1

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Cross Reference

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PERFORMANCE (Continued)	QSI	SIGNETICS	QSI
P74PCT257A	QS74FCT257T	74ABT2952	QS29FCT52BT
P74PCT257B	QS74FCT257AT	74ABT2953	QS29FCT53BT
P74PCT258A	QS74FCT258T	74ABT240	QS74FCT240CT
P74PCT258B	QS74FCT258AT	74ABT241	QS74FCT241CT
P74PCT273	QS74FCT273T	74ABT244	QS74FCT244CT
P74PCT273A	QS74FCT273AT	74ABT245	QS74FCT245CT
P74PCT299	QS74FCT299T	74ABT373	QS74FCT373CT
P74PCT299A	QS74FCT299AT	74ABT374	QS74FCT374CT
P74PCT373	QS74FCT373T	74ABT377	QS74FCT377CT
P74PCT373A	QS74FCT373AT	74ABT533	QS74FCT533CT
P74PCT374	QS74FCT374T	74ABT534	QS74FCT534CT
P74PCT374A	QS74FCT374AT	74ABT540	QS74FCT540AT
P74PCT377	QS74FCT377T	74ABT541	QS74FCT541AT
P74PCT377A	QS74FCT377AT	74ABT543	QS74FCT543AT
P74PCT521	QS74FCT521T	74ABT544	QS74FCT544AT
P74PCT521A	QS74FCT521AT	74ABT573	QS74FCT573AT
P74PCT521B	QS74FCT521BT	74ABT574	QS74FCT574AT
P74PCT533	QS74FCT533T	74ABT646	QS74FCT646CT
P74PCT533A	QS74FCT533AT	74ABT648	QS74FCT648CT
P74PCT534	QS74FCT534T	74ABT651	QS74FCT651AT
P74PCT534A	QS74FCT534AT	74ABT652	QS74FCT652AT
P74PCT543	QS74FCT543T	74ABT821	QS74FCT821BT
P74PCT543A	QS74FCT543AT	74ABT823	QS74FCT823BT
P74PCT544	QS74FCT544T	74ABT825	QS74FCT825BT
P74PCT544A	QS74FCT544AT	74ABT827	QS74FCT827BT
P74PCT573	QS74FCT573T	74ABT841	QS74FCT841BT
P74PCT573A	QS74FCT573AT	74ABT843	QS74FCT843BT
P74PCT574	QS74FCT574T	74ABT845	QS74FCT845BT
P74PCT574A	QS74FCT574AT	74ABT861	QS74FCT861BT
P74PCT640	QS74FCT640T	74ABT863	QS74FCT863BT
P74PCT640A	QS74FCT640AT		
P74PCT646	QS74FCT646T	TI	QSI
P74PCT646A	QS74FCT646AT	SN74ABT2952	QS29FCT52BT
P74PCT648	QS74FCT648T	SN74ABT2953	QS29FCT53BT
P74PCT648A	QS74FCT648AT	SN74ABT2240	QS74FCT2240CT
P74PCT651	QS74FCT651T	SN74ABT2241	QS74FCT2241CT
P74PCT651A	QS74FCT651AT	SN74ABT2244	QS74FCT2244CT
P74PCT652	QS74FCT652T	SN74ABT240	QS74FCT240CT
P74PCT652A	QS74FCT652AT	SN74ABT241	QS74FCT241CT
P74PCT821A	QS74FCT821AT	SN74ABT244	QS74FCT244CT
P74PCT821B	QS74FCT821BT	SN74ABT245	QS74FCT245CT
P74PCT823A	QS74FCT823AT	SN74ABT299	QS74FCT299AT
P74PCT823B	QS74FCT823BT	SN74ABT373	QS74FCT373CT
P74PCT825A	QS74FCT825AT	SN74ABT374	QS74FCT374CT
P74PCT825B	QS74FCT825BT	SN74ABT533	QS74FCT533CT
P74PCT827A	QS74FCT827AT	SN74ABT534	QS74FCT534CT
P74PCT827B	QS74FCT827BT	SN74ABT540	QS74FCT540AT
P74PCT828A	QS74FCT828AT	SN74ABT541	QS74FCT541AT
P74PCT828B	QS74FCT828BT	SN74ABT573	QS74FCT573AT
P74PCT841A	QS74FCT841AT	SN74ABT574	QS74FCT574AT
P74PCT841B	QS74FCT841BT	SN74ABT646	QS74FCT646CT
P74PCT843A	QS74FCT843AT	SN74ABT648	QS74FCT648CT
P74PCT843B	QS74FCT843BT	SN74ABT651	QS74FCT651AT

Cross Reference

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TI Q (Continued)	QSI Q	QSI Q	PERFORMANCE (Continued)
SN74ABT652	Q	QS74FCT652AT	P74PCT527A
SN74ABT821	Q	QS74FCT821BT	P74PCT527B
SN74ABT823	Q	QS74FCT823BT	P74PCT528A
SN74ABT825	Q	QS74FCT825BT	P74PCT528B
SN74ABT827	Q	QS74FCT827BT	P74PCT529
SN74ABT828	Q	QS74FCT828BT	P74PCT529A
SN74ABT841	Q	QS74FCT841BT	P74PCT529B
SN74ABT843	Q	QS74FCT843BT	P74PCT530A
SN74ABT845	Q	QS74FCT845BT	P74PCT530B
SN74ABT861	Q	QS74FCT861BT	P74PCT531A
SN74ABT864	Q	QS74FCT864BT	P74PCT531B
SN74BCT2952	Q	QS29FCT52AT	P74PCT532A
SN74BCT2953	Q	QS29FCT53AT	P74PCT532B
SN74BCT240	Q	QST4FCT240T	P74PCT533A
SN74BCT241	Q	QST4FCT241T	P74PCT533B
SN74BCT244	Q	QST4FCT244T	P74PCT534A
SN74BCT245	Q	QST4FCT245T	P74PCT534B
SN74BCT299	Q	QS74FCT299T	P74PCT535A
SN74BCT373	Q	QST4FCT373T	P74PCT535B
SN74BCT374	Q	QST4FCT374T	P74PCT536A
SN74BCT533	Q	QS74FCT533T	P74PCT536B
SN74BCT534	Q	QS74FCT534T	P74PCT537A
SN74BCT540	Q	QS74FCT540T	P74PCT537B
SN74BCT541	Q	QS74FCT541T	P74PCT538A
SN74BCT543	Q	QS74FCT543T	P74PCT538B
SN74BCT544	Q	QS74FCT544T	P74PCT539A
SN74BCT573	Q	QS74FCT573T	P74PCT539B
SN74BCT574	Q	QS74FCT574T	P74PCT540A
SN74BCT646	Q	QS74FCT646T	P74PCT540B
SN74BCT648	Q	QS74FCT648T	P74PCT541A
SN74BCT651	Q	QS74FCT651T	P74PCT541B
SN74BCT652	Q	QS74FCT652T	P74PCT542A
SN74BCT821	Q	QS74FCT821AT	P74PCT542B
SN74BCT823	Q	QS74FCT823AT	P74PCT543A
SN74BCT825	Q	QS74FCT825AT	P74PCT543B
SN74BCT828	Q	QS74FCT828AT	P74PCT544A
SN74BCT2240	Q	QS74FCT2240T	P74PCT544B
SN74BCT2241	Q	QS74FCT2241T	P74PCT545A
SN74BCT2244	Q	QS74FCT2244T	P74PCT545B
SN74BCT2827	Q	QS74FCT2827AT	P74PCT546A
SN74BCT2828	Q	QS74FCT2828AT	P74PCT546B
SN74BCT2829	Q	QS74FCT2829AT	P74PCT547A
SN74BCT2830	Q	QS74FCT2830AT	P74PCT547B
SN74BCT2831	Q	QS74FCT2831AT	P74PCT548A
SN74BCT2832	Q	QS74FCT2832AT	P74PCT548B
SN74BCT2833	Q	QS74FCT2833AT	P74PCT549A
SN74BCT2834	Q	QS74FCT2834AT	P74PCT549B
SN74BCT2835	Q	QS74FCT2835AT	P74PCT550A
SN74BCT2836	Q	QS74FCT2836AT	P74PCT550B
SN74BCT2837	Q	QS74FCT2837AT	P74PCT551A
SN74BCT2838	Q	QS74FCT2838AT	P74PCT551B
SN74BCT2839	Q	QS74FCT2839AT	P74PCT552A
SN74BCT2840	Q	QS74FCT2840AT	P74PCT552B
SN74BCT2841	Q	QS74FCT2841AT	P74PCT553A
SN74BCT2842	Q	QS74FCT2842AT	P74PCT553B
SN74BCT2843	Q	QS74FCT2843AT	P74PCT554A
SN74BCT2844	Q	QS74FCT2844AT	P74PCT554B
SN74BCT2845	Q	QS74FCT2845AT	P74PCT555A
SN74BCT2846	Q	QS74FCT2846AT	P74PCT555B
SN74BCT2847	Q	QS74FCT2847AT	P74PCT556A
SN74BCT2848	Q	QS74FCT2848AT	P74PCT556B
SN74BCT2849	Q	QS74FCT2849AT	P74PCT557A
SN74BCT2850	Q	QS74FCT2850AT	P74PCT557B
SN74BCT2851	Q	QS74FCT2851AT	P74PCT558A
SN74BCT2852	Q	QS74FCT2852AT	P74PCT558B
SN74BCT2853	Q	QS74FCT2853AT	P74PCT559A
SN74BCT2854	Q	QS74FCT2854AT	P74PCT559B
SN74BCT2855	Q	QS74FCT2855AT	P74PCT560A
SN74BCT2856	Q	QS74FCT2856AT	P74PCT560B
SN74BCT2857	Q	QS74FCT2857AT	P74PCT561A
SN74BCT2858	Q	QS74FCT2858AT	P74PCT561B
SN74BCT2859	Q	QS74FCT2859AT	P74PCT562A
SN74BCT2860	Q	QS74FCT2860AT	P74PCT562B
SN74BCT2861	Q	QS74FCT2861AT	P74PCT563A
SN74BCT2862	Q	QS74FCT2862AT	P74PCT563B
SN74BCT2863	Q	QS74FCT2863AT	P74PCT564A
SN74BCT2864	Q	QS74FCT2864AT	P74PCT564B
SN74BCT2865	Q	QS74FCT2865AT	P74PCT565A
SN74BCT2866	Q	QS74FCT2866AT	P74PCT565B
SN74BCT2867	Q	QS74FCT2867AT	P74PCT566A
SN74BCT2868	Q	QS74FCT2868AT	P74PCT566B
SN74BCT2869	Q	QS74FCT2869AT	P74PCT567A
SN74BCT2870	Q	QS74FCT2870AT	P74PCT567B
SN74BCT2871	Q	QS74FCT2871AT	P74PCT568A
SN74BCT2872	Q	QS74FCT2872AT	P74PCT568B
SN74BCT2873	Q	QS74FCT2873AT	P74PCT569A
SN74BCT2874	Q	QS74FCT2874AT	P74PCT569B
SN74BCT2875	Q	QS74FCT2875AT	P74PCT570A
SN74BCT2876	Q	QS74FCT2876AT	P74PCT570B
SN74BCT2877	Q	QS74FCT2877AT	P74PCT571A
SN74BCT2878	Q	QS74FCT2878AT	P74PCT571B
SN74BCT2879	Q	QS74FCT2879AT	P74PCT572A
SN74BCT2880	Q	QS74FCT2880AT	P74PCT572B
SN74BCT2881	Q	QS74FCT2881AT	P74PCT573A
SN74BCT2882	Q	QS74FCT2882AT	P74PCT573B
SN74BCT2883	Q	QS74FCT2883AT	P74PCT574A
SN74BCT2884	Q	QS74FCT2884AT	P74PCT574B
SN74BCT2885	Q	QS74FCT2885AT	P74PCT575A
SN74BCT2886	Q	QS74FCT2886AT	P74PCT575B
SN74BCT2887	Q	QS74FCT2887AT	P74PCT576A
SN74BCT2888	Q	QS74FCT2888AT	P74PCT576B
SN74BCT2889	Q	QS74FCT2889AT	P74PCT577A
SN74BCT2890	Q	QS74FCT2890AT	P74PCT577B
SN74BCT2891	Q	QS74FCT2891AT	P74PCT578A
SN74BCT2892	Q	QS74FCT2892AT	P74PCT578B
SN74BCT2893	Q	QS74FCT2893AT	P74PCT579A
SN74BCT2894	Q	QS74FCT2894AT	P74PCT579B
SN74BCT2895	Q	QS74FCT2895AT	P74PCT580A
SN74BCT2896	Q	QS74FCT2896AT	P74PCT580B
SN74BCT2897	Q	QS74FCT2897AT	P74PCT581A
SN74BCT2898	Q	QS74FCT2898AT	P74PCT581B
SN74BCT2899	Q	QS74FCT2899AT	P74PCT582A
SN74BCT2900	Q	QS74FCT2900AT	P74PCT582B
SN74BCT2901	Q	QS74FCT2901AT	P74PCT583A
SN74BCT2902	Q	QS74FCT2902AT	P74PCT583B
SN74BCT2903	Q	QS74FCT2903AT	P74PCT584A
SN74BCT2904	Q	QS74FCT2904AT	P74PCT584B
SN74BCT2905	Q	QS74FCT2905AT	P74PCT585A
SN74BCT2906	Q	QS74FCT2906AT	P74PCT585B
SN74BCT2907	Q	QS74FCT2907AT	P74PCT586A
SN74BCT2908	Q	QS74FCT2908AT	P74PCT586B
SN74BCT2909	Q	QS74FCT2909AT	P74PCT587A
SN74BCT2910	Q	QS74FCT2910AT	P74PCT587B
SN74BCT2911	Q	QS74FCT2911AT	P74PCT588A
SN74BCT2912	Q	QS74FCT2912AT	P74PCT588B
SN74BCT2913	Q	QS74FCT2913AT	P74PCT589A
SN74BCT2914	Q	QS74FCT2914AT	P74PCT589B
SN74BCT2915	Q	QS74FCT2915AT	P74PCT590A
SN74BCT2916	Q	QS74FCT2916AT	P74PCT590B
SN74BCT2917	Q	QS74FCT2917AT	P74PCT591A
SN74BCT2918	Q	QS74FCT2918AT	P74PCT591B
SN74BCT2919	Q	QS74FCT2919AT	P74PCT592A
SN74BCT2920	Q	QS74FCT2920AT	P74PCT592B
SN74BCT2921	Q	QS74FCT2921AT	P74PCT593A
SN74BCT2922	Q	QS74FCT2922AT	P74PCT593B
SN74BCT2923	Q	QS74FCT2923AT	P74PCT594A
SN74BCT2924	Q	QS74FCT2924AT	P74PCT594B
SN74BCT2925	Q	QS74FCT2925AT	P74PCT595A
SN74BCT2926	Q	QS74FCT2926AT	P74PCT595B
SN74BCT2927	Q	QS74FCT2927AT	P74PCT596A
SN74BCT2928	Q	QS74FCT2928AT	P74PCT596B
SN74BCT2929	Q	QS74FCT2929AT	P74PCT597A
SN74BCT2930	Q	QS74FCT2930AT	P74PCT597B
SN74BCT2931	Q	QS74FCT2931AT	P74PCT598A
SN74BCT2932	Q	QS74FCT2932AT	P74PCT598B
SN74BCT2933	Q	QS74FCT2933AT	P74PCT599A
SN74BCT2934	Q	QS74FCT2934AT	P74PCT599B
SN74BCT2935	Q	QS74FCT2935AT	P74PCT600A
SN74BCT2936	Q	QS74FCT2936AT	P74PCT600B
SN74BCT2937	Q	QS74FCT2937AT	P74PCT601A
SN74BCT2938	Q	QS74FCT2938AT	P74PCT601B
SN74BCT2939	Q	QS74FCT2939AT	P74PCT602A
SN74BCT2940	Q	QS74FCT2940AT	P74PCT602B
SN74BCT2941	Q	QS74FCT2941AT	P74PCT603A
SN74BCT2942	Q	QS74FCT2942AT	P74PCT603B
SN74BCT2943	Q	QS74FCT2943AT	P74PCT604A
SN74BCT2944	Q	QS74FCT2944AT	P74PCT604B
SN74BCT2945	Q	QS74FCT2945AT	P74PCT605A
SN74BCT2946	Q	QS74FCT2946AT	P74PCT605B
SN74BCT2947	Q	QS74FCT2947AT	P74PCT606A
SN74BCT2948	Q	QS74FCT2948AT	P74PCT606B
SN74BCT2949	Q	QS74FCT2949AT	P74PCT607A
SN74BCT2950	Q	QS74FCT2950AT	P74PCT607B
SN74BCT2951	Q	QS74FCT2951AT	P74PCT608A
SN74BCT2952	Q	QS74FCT2952AT	P74PCT608B
SN74BCT2953	Q	QS74FCT2953AT	P74PCT609A
SN74BCT2954	Q	QS74FCT2954AT	P74PCT609B
SN74BCT2955	Q	QS74FCT2955AT	P74PCT610A
SN74BCT2956	Q	QS74FCT2956AT	P74PCT610B
SN74BCT2957	Q	QS74FCT2957AT	P74PCT611A
SN74BCT2958	Q	QS74FCT2958AT	P74PCT611B
SN74BCT2959	Q	QS74FCT2959AT	P74PCT612A
SN74BCT2960	Q	QS74FCT2960AT	P74PCT612B
SN74BCT2961	Q	QS74FCT2961AT	P74PCT613A
SN74BCT2962	Q	QS74FCT2962AT	P74PCT613B
SN74BCT2963	Q	QS74FCT2963AT	P74PCT614A
SN74BCT2964	Q	QS74FCT2964AT	P74PCT614B
SN74BCT2965	Q	QS74FCT2965AT	P74PCT615A
SN74BCT2966	Q	QS74FCT2966AT	P74PCT615B
SN74BCT2967	Q	QS74FCT2967AT	P74PCT616A
SN74BCT2968	Q	QS74FCT2968AT	P74PCT616B
SN74BCT2969	Q	QS74FCT2969AT	P74PCT617A
SN74BCT2970	Q	QS74FCT2970AT	P74PCT617B
SN74BCT2971	Q	QS74FCT2971AT	P74PCT618A
SN74BCT2972	Q	QS74FCT2972AT	P74PCT618B
SN74BCT2973	Q	QS74FCT2973AT	P74PCT619A
SN74BCT2974	Q	QS74FCT2974AT	P74PCT619B
SN74BCT2975	Q	QS74FCT2975AT	P74PCT620A
SN74BCT2976	Q	QS74FCT2976AT	P74PCT620B
SN74BCT2977	Q	QS74FCT2977AT	P74PCT621A
SN74BCT2978	Q	QS74FCT2978AT	P74PCT621B
SN74BCT2979	Q	QS74FCT2979AT	P74PCT622A
SN74BCT2980	Q	QS74FCT2980AT	P74PCT622B
SN74BCT2981	Q	QS74FCT2981AT	P74PCT623A
SN74BCT2982	Q	QS74FCT2982AT	P74PCT623B
SN74BCT2983	Q	QS74FCT2983AT	P74PCT624A
SN74BCT2984	Q	QS74FCT2984AT	P74PCT624B
SN74BCT2985	Q	QS74FCT2985AT	P74PCT625A
SN74BCT2986	Q	QS74FCT2986AT	P74PCT625B
SN74BCT2987	Q	QS74FCT2987AT	P74PCT626A
SN74BCT2988	Q	QS74FCT2988AT	P74PCT626B
SN74BCT2989	Q	QS74FCT2989AT	P74PCT627A
SN74BCT2990	Q	QS74FCT2990AT	P74PCT627B
SN74BCT2991	Q	QS74FCT2991AT	P74PCT628A
SN74BCT2992	Q	QS74FCT2992AT	P74PCT628B
SN74BCT2993	Q	QS74FCT2993AT	P74PCT629A
SN74BCT2994	Q	QS74FCT2994AT	P74PCT629B
SN74BCT2995	Q	QS74FCT2995AT	P74PCT630A
SN74BCT2996	Q	QS74FCT2996AT	P74PCT630B
SN74BCT2997	Q	QS74FCT2997AT	P74PCT631A
SN74BCT2998	Q	QS74FCT2998AT	P74PCT631B
SN74BCT2999	Q	QS74FCT2999AT	P74PCT632A
SN74BCT3000	Q	QS74FCT3000AT	P74PCT632B

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1	General Information
2	Product Line
3	FIRO Memory Products
4	FCT-T Logic Products
5	QuickSwitch Products
6	Application Notes
7	Quality And Reliability
8	Package Information
9	Sales Offices

SRAM Table of Contents

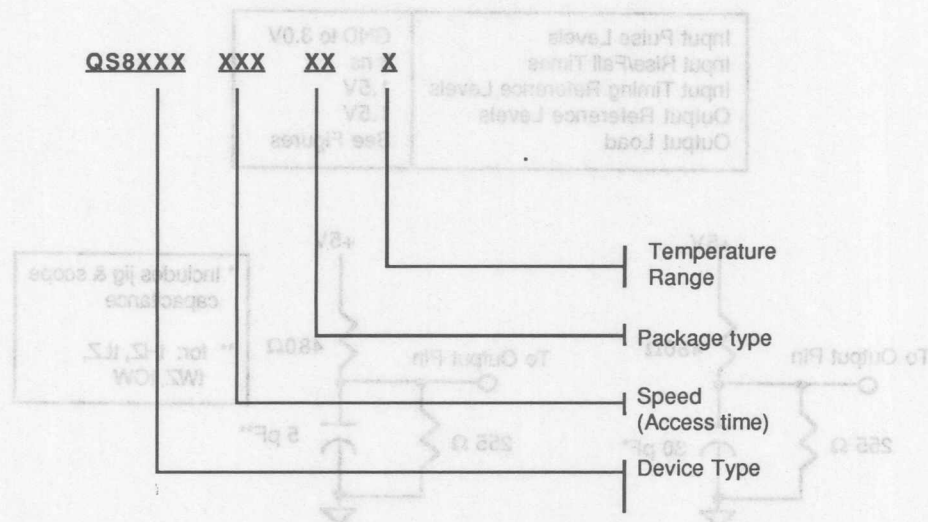
STATIC RAM DATA SHEETS

	Page
SRAM Ordering Information	2-3
SRAM Test Configuration	2-4
QS8768	4Kx4 SRAM in 20 pins
QS8769	4Kx4 SRAM in 20 pins with fast $\overline{CS}$
QS8780	4Kx4 Cache Tag RAM with Reset
QS8881/2	16Kx4 SRAM with Separate I/O
QS8883	16Kx4 Cache Tag SRAM
QS8885/6	16Kx4 SRAM with Output Enable
QS8888	16Kx4 SRAM in 22 pins
QS88180/60	8Kx18/16 SRAM
QS88181	8Kx18 Burst Mode SRAM
QS88182	8Kx18 Cache TAG SRAM
QS83280	32Kx8 SRAM
QS83283	32Kx8 SRAM with Fast Address bit
QS83285	32Kx8 Low Power SRAM
QS83289	32Kx8 SRAM with Fast Chip Select
QS83290	32Kx9 SRAM
QS83291	32Kx9 Burst Mode SRAM
QS86440	64Kx4 SRAM
QS86442	64Kx4 Cache TAG SRAM
QS86444/9	64Kx4 SRAM with Separate I/O
QS86446	64Kx4 SRAM with Output Enable
QS86447	64Kx4 SRAM with Address Latch
QS86448	64Kx4 SRAM with Address Register
QS81280	128Kx8 SRAM

SRAM Table of Contents

Page	STATIC RAM DATA SHEETS
2-3	SRAM Ordering Information
2-4	SRAM Test Configuration
2-5	4Kx4 SRAM in 20 pins
2-10	4Kx4 SRAM in 20 pins with fast CS
2-21	4Kx4 Cache Tag SRAM with Reset
2-31	16Kx4 SRAM with Separate VO
2-41	16Kx4 Cache Tag SRAM
2-51	16Kx4 SRAM with Output Enable
2-59	16Kx4 SRAM in 32 pins
2-67	64Kx4 SRAM
2-77	8Kx16 Burst Mode SRAM
2-79	8Kx16 Cache TAG SRAM
2-81	32Kx8 SRAM
2-89	32Kx8 SRAM with Fast Address bit
2-91	32Kx8 Low Power SRAM
2-99	32Kx8 SRAM with Fast Chip Select
2-101	32Kx8 SRAM
2-103	32Kx8 Burst Mode SRAM
2-105	64Kx4 SRAM
2-113	64Kx4 Cache TAG SRAM
2-115	64Kx4 SRAM with Separate VO
2-117	64Kx4 SRAM with Output Enable
2-125	64Kx4 SRAM with Address Latch
2-127	64Kx4 SRAM with Address Register
2-129	128Kx8 SRAM

SRAM Ordering Information



2

Processing:

Blank - Standard
B - MIL-STD 883

Package Type:

P - Plastic DIP, 300 mil
D - Ceramic DIP, 300 mil
L - Leadless Ceramic Chip Carrier
SO - Small Outline IC, 300 mil
S1 - Small Outline IC, 150 mil
Z - Plastic ZIP
Q - QSOP, Quarter Size Outline Package, 150 mil

Figure 2. Output test loads for 8Kx16 and 6Kx16 SRAMs

Figure 3. Output test loads for Low-Power 32Kx8 SRAMs

SRAM Test Configuration

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures

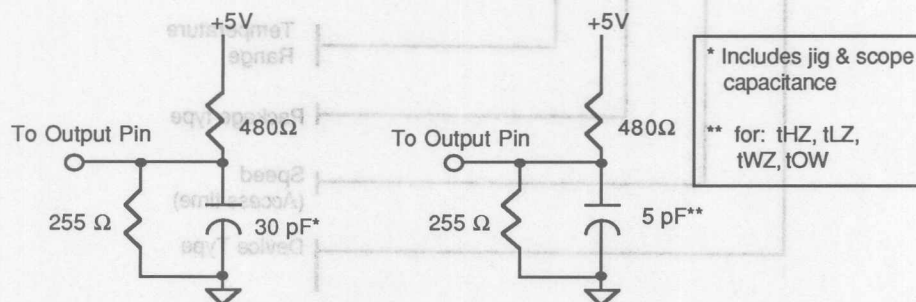


Figure 1. Output test loads for: 4Kx4, 16Kx4, 64Kx4, 32Kx8 & 128Kx8 SRAMs (Except Low-Power)

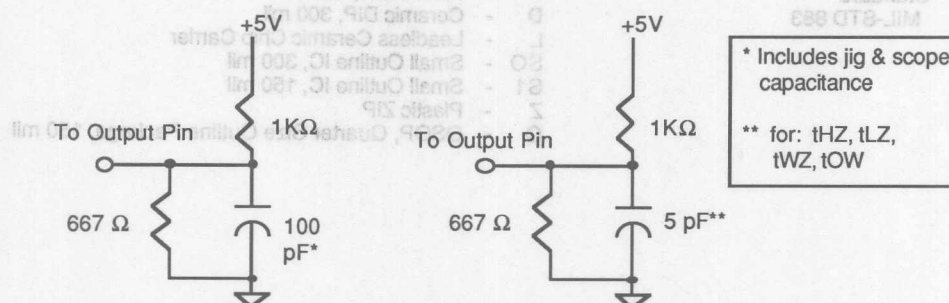


Figure 2. Output test loads for: 8Kx18 and 8Kx16 SRAMs

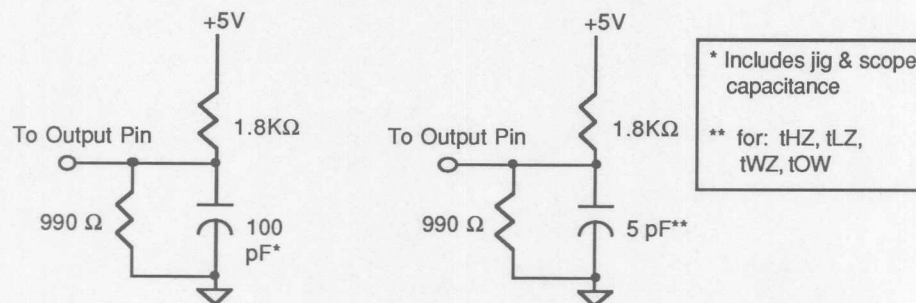


Figure 3. Output test loads for Low-Power 32Kx8 SRAMs



High-Speed CMOS 4Kx4 SRAM with Common I/O

QS8768

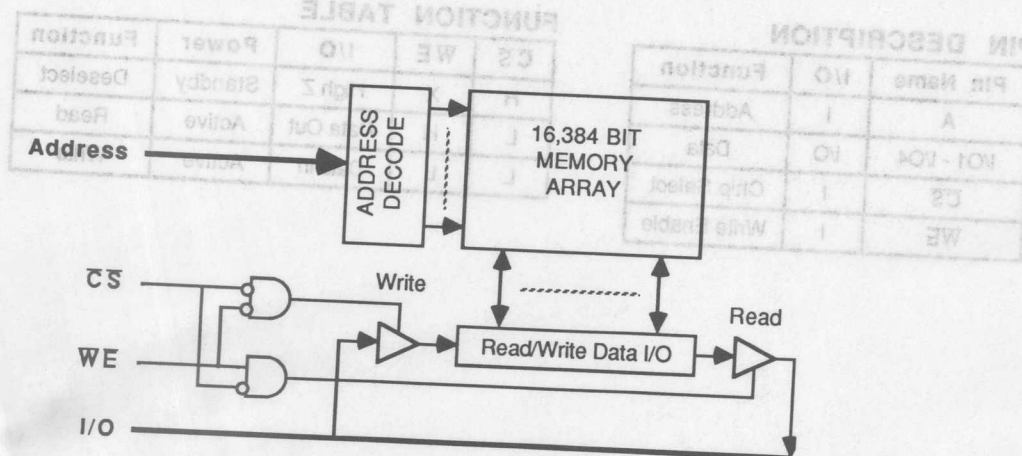
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 10ns/12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 20-pin DIP, 20-Pin ZIP
- 20-pin 300 mil SOJ & 20-pin LCC
- Low Standby current
- JEDEC standard pinout

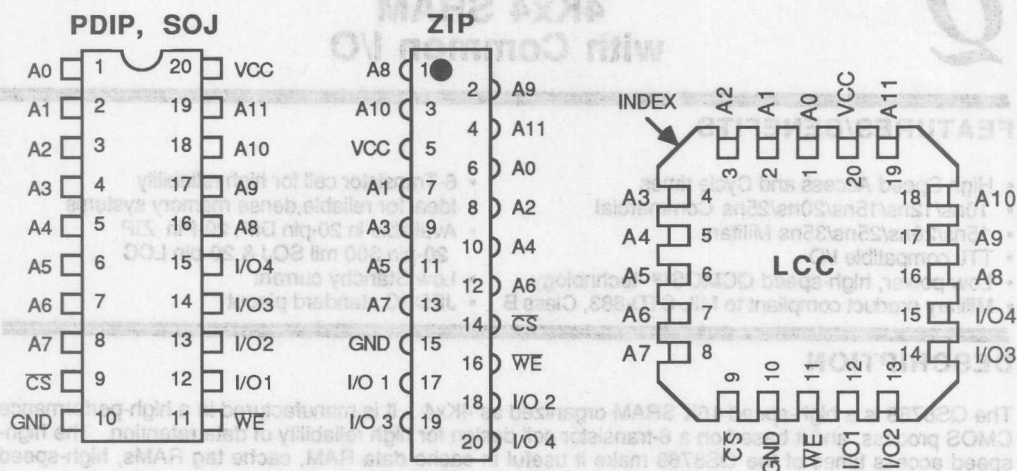
DESCRIPTION

The QS8768 is a high-speed 16K SRAM organized as 4Kx4. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS8768 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



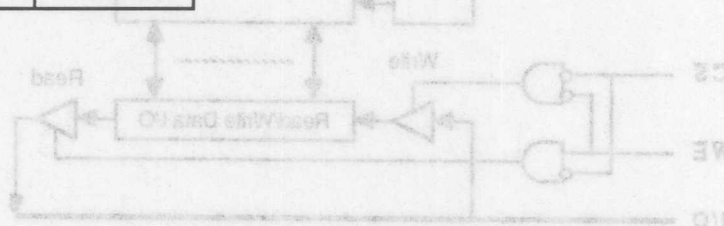
ALL PINS TOP VIEW

PIN DESCRIPTION

Pin	Name	I/O	Function
A		I	Address
I/O1 - I/O4		I/O	Data
CS		I	Chip Select
WE		I	Write Enable

FUNCTION TABLE

CS	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$		
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA		
DC Output Current Max. source current/pin.....	30 mA		
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C		
T_{STG} Storage Temperature, COM.....	-65° to +125°C		
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	165	135	155	125	145	120	140	110	130	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	60	70	60	70	60	70	60	70	60	70	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE													
t RC	Read Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	2	-	2	-	2	-	3	-	3	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-	3	-
t CHZ	Chip Select to Output in High Z (2)	-	4	-	5	-	7	-	8	-	10	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	-	10	-	12	-	15	-	19	-	25	-	35

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS8768

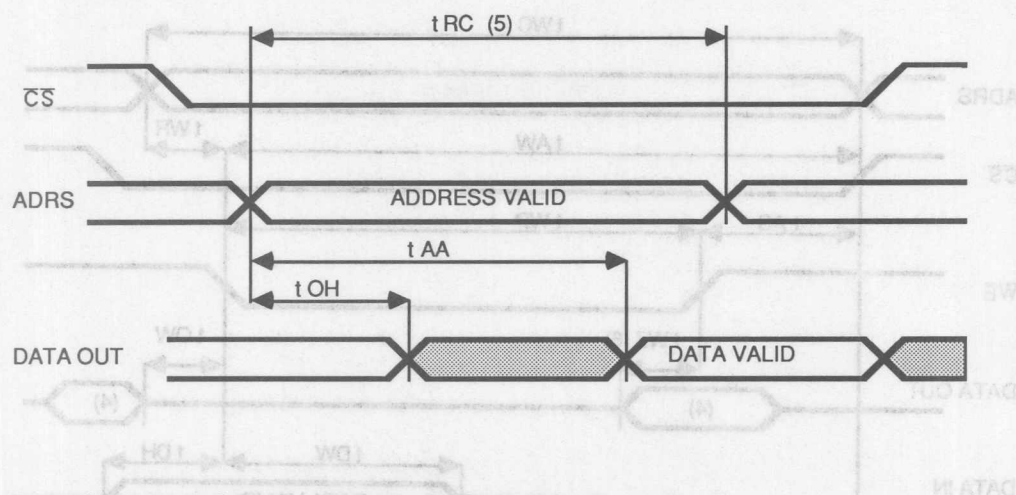
Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10 (3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE													
t WC	Write Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	8	-	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	5	-	7	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	4	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write (2)	2	-	2	-	2	-	2	-	2	-	3	-

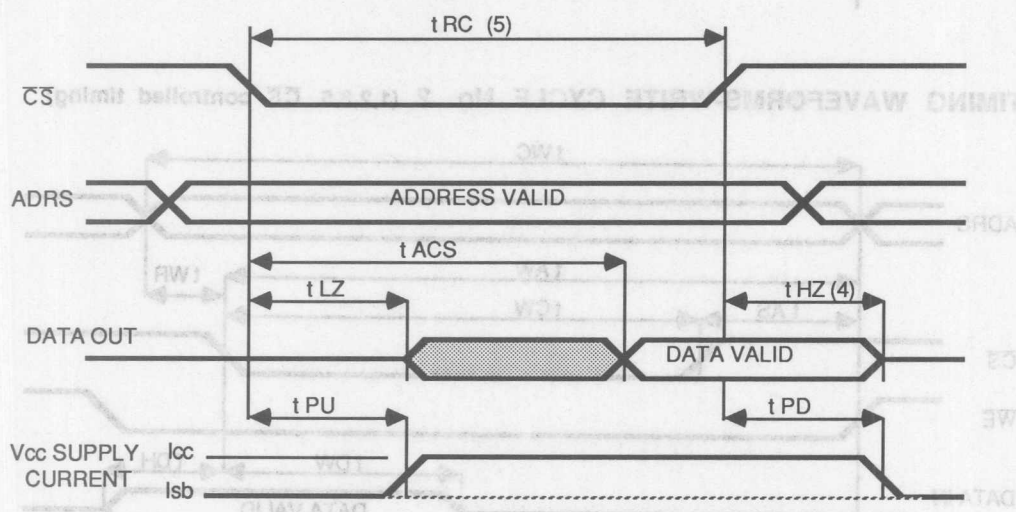
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



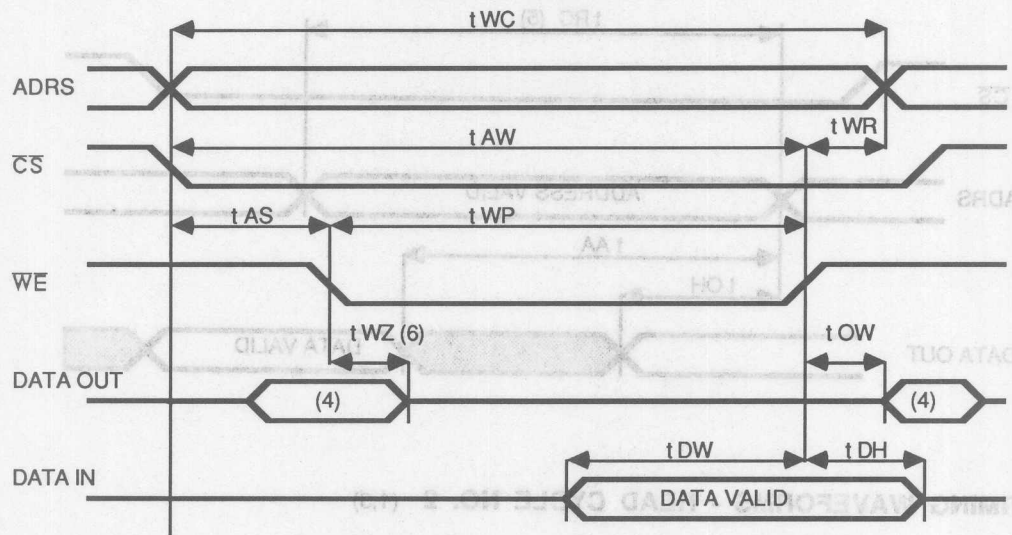
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



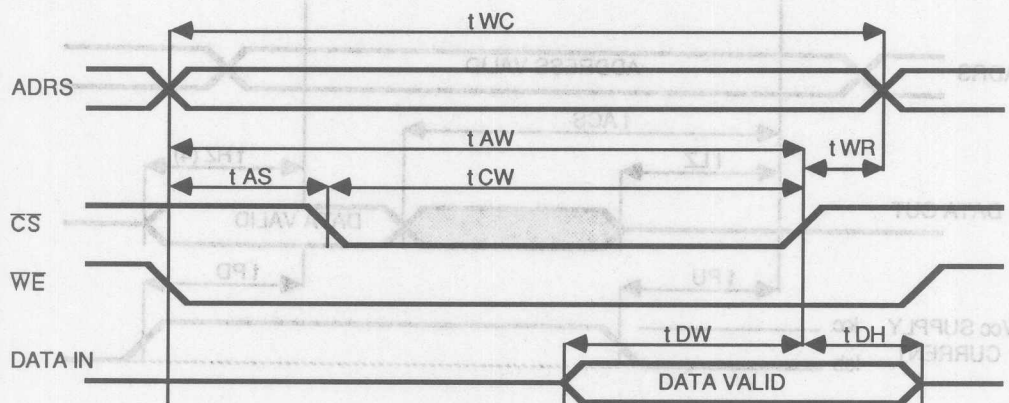
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. t WR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 4Kx4 SRAM with Fast Chip Select

QS8769

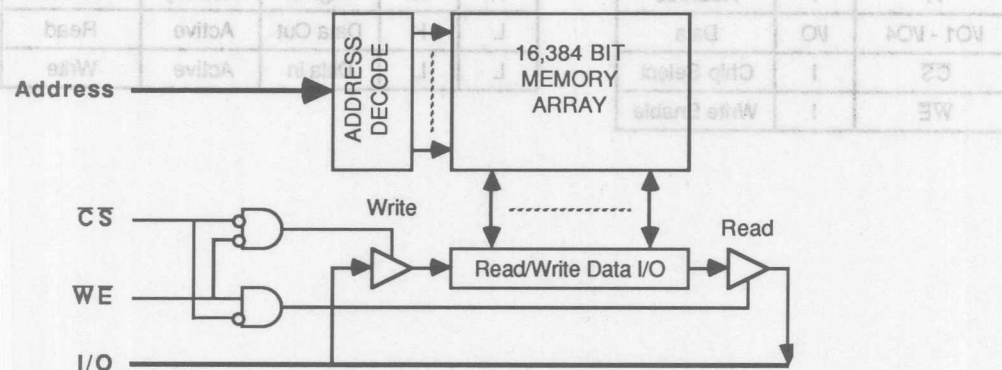
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 10ns/12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- Non power down for fast Chip select access
- 5ns/6ns/8ns/10ns/12ns chip select access times
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- TTL compatible I/O
- Available in 20-pin DIP, 20-Pin ZIP
- 20-pin 300 mil SOJ, 20-pin LCC
- JEDEC standard pinout

DESCRIPTION

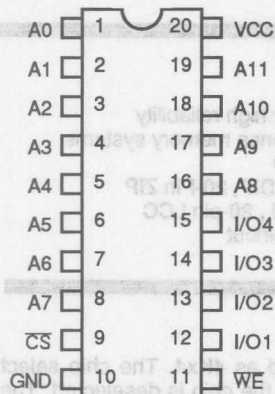
The QS8769 is a high-speed 16K SRAM with fast chip select organized as 4Kx4. The chip select access time is fast since it does not power down the memory array when the chip is deselected. The QS8769 is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS8769 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM

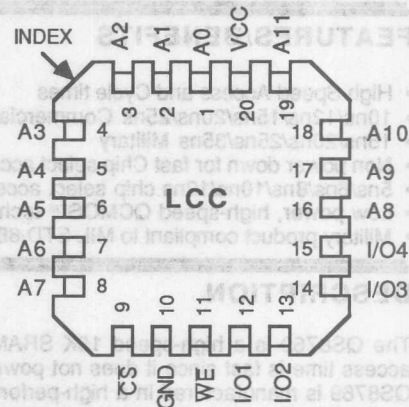
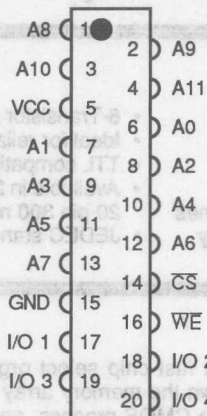


PIN CONFIGURATIONS

PDIP, SOJ



ZIP



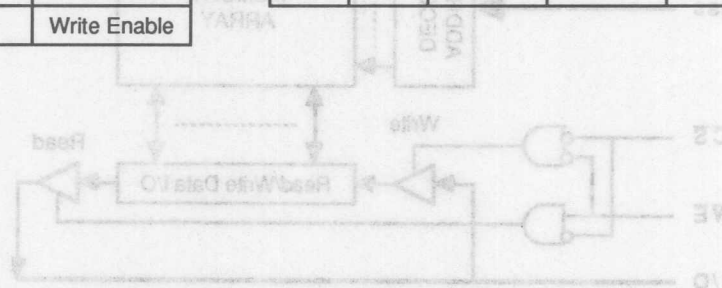
ALL PINS TOP VIEW

PIN DESCRIPTION

Pin	Name	I/O	Function
	A	I	Address
	I/O1 - I/O4	I/O	Data
	CS	I	Chip Select
	WE	I	Write Enable

FUNCTION TABLE

CS	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Output Current Max. sink current/pin.....	50 mA
DC Output Current Max. source current/pin.....	30 mA
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C
T_{STG} Storage Temperature, COM.....	-65° to +125°C
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C
T_{STG} Storage Temperature, MIL.....	-65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
C_{in}	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
C_{in}	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
C_{out}	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.	7	7	pF
C_{out}	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.	7	7	pF

Note: Capacitance is measured at characterization but not tested at final production.

Symbol	Test Conditions	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
t_{dL}	Static Operating Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IL}$, $t = 0$	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000
t_{dS}	Dynamic Operating Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IL}$, $t = 1 \text{ MAX}$	148	188	228	268	308	348	388	428	468	508	548	588	628	668	708	748	788	828	868

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes: 1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	165	135	155	125	145	120	140	110	130	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE													
t RC	Read Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	5	-	6	-	8	-	10	-	12	-	17
t OH	Output Hold from Address Change	2	-	2	-	2	-	3	-	3	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-	3	-
t CHZ	Chip Select to Output in High Z (2)	-	5	-	6	-	7	-	8	-	10	-	15

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS8769

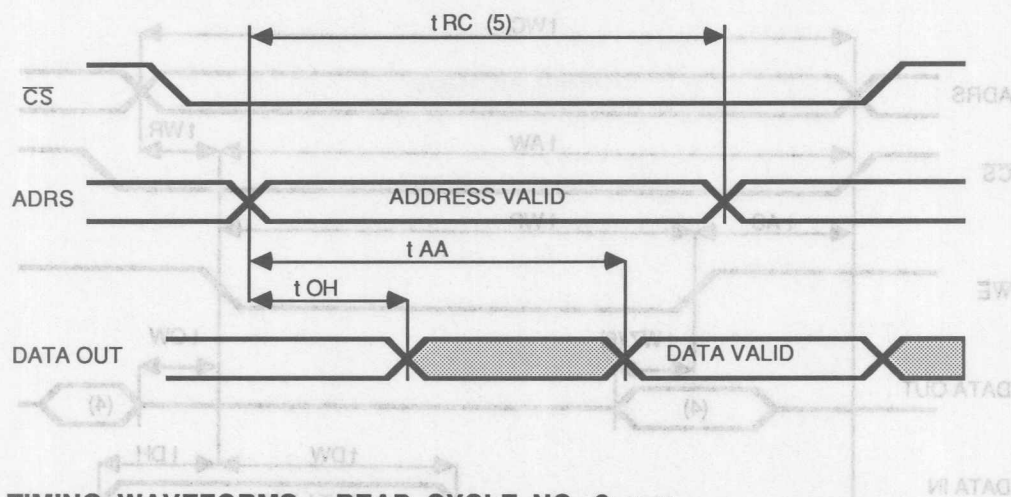
Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE													
t WC	Write Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	9	-	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	9	-	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	9	-	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	6	-	7	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	4	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write	2	-	2	-	2	-	2	-	2	-	3	-

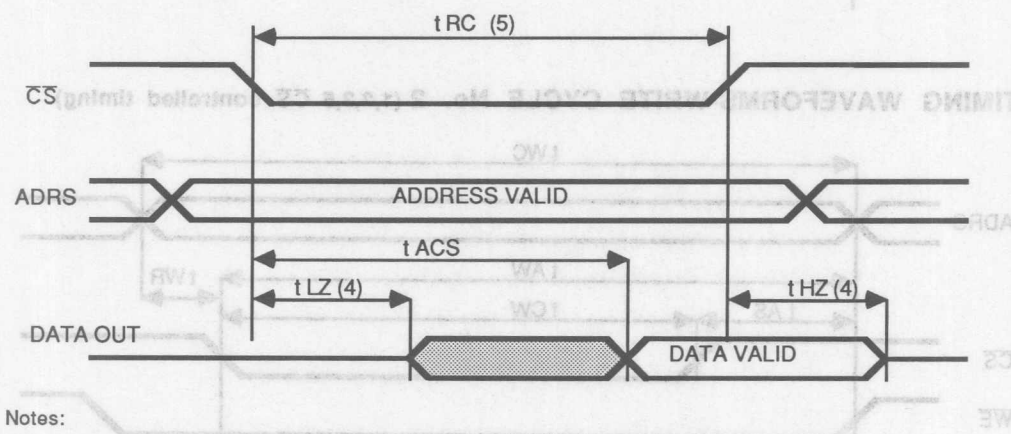
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



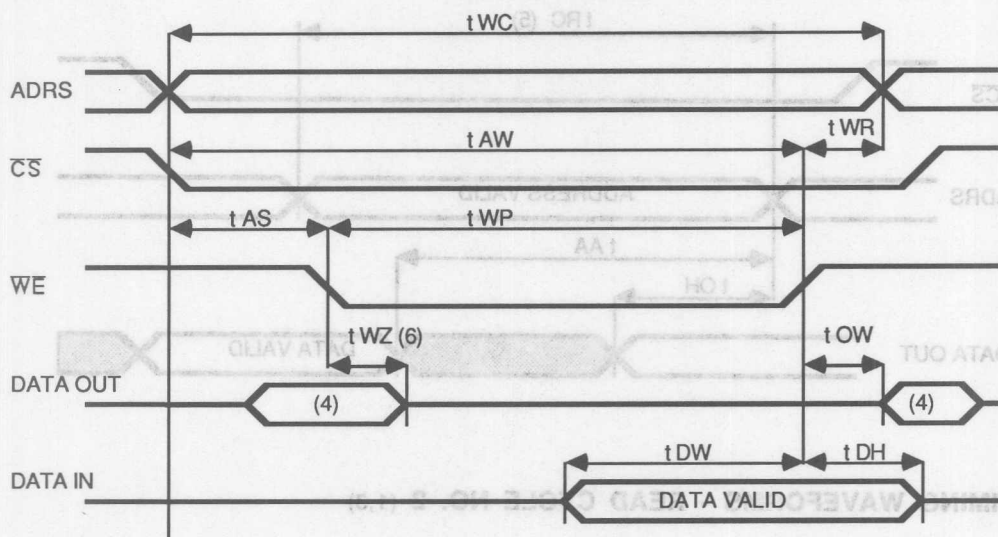
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



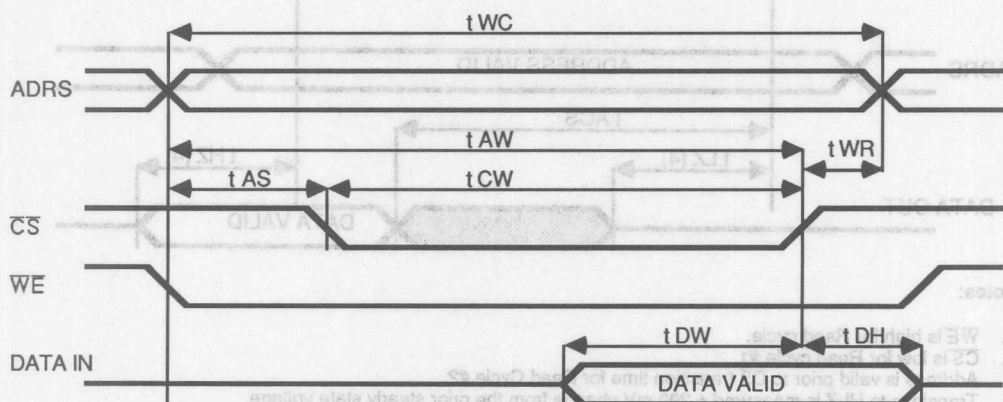
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid prior to CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 4Kx4 Cache Tag SRAM with Reset

QS8780
ADVANCE
INFORMATION

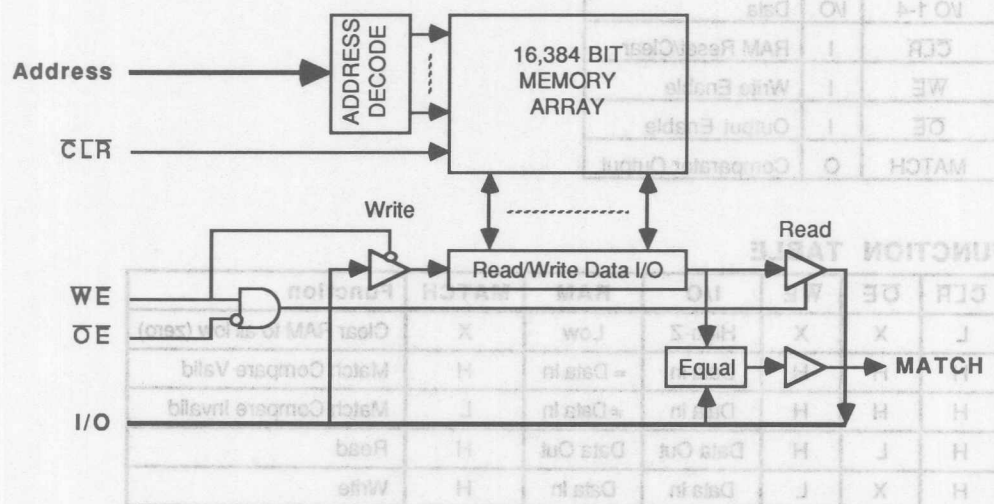
FEATURES/BENEFITS

- High Speed Match Access and Cycle times
- MATCH output goes high on match
- 12ns/15ns/20ns/25ns/35ns Commercial
- 15ns/20ns/25ns/35ns/45ns Military
- Low power, high-speed QCMOS™ technology
- Single reset pulse clears all RAM data to zero
- TTL level MATCH output
- Available in 22-pin DIP, 24-pin ZIP, & 24-pin 300 mil SOJ.
- 6-Transistor cell for high reliability

DESCRIPTION

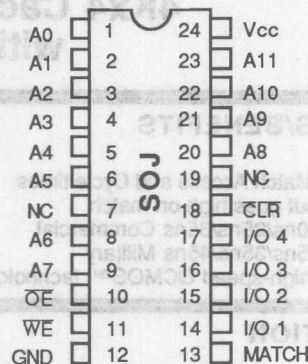
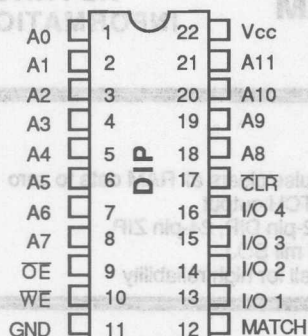
The QS8780 is a high-speed 16K Cache Tag SRAM with reset. It is organized as a 4Kx4 SRAM with a tag comparator between the data inputs and the RAM outputs. The match comparator output goes high on a match and has full TTL output drive. The RAM may be reset with a single pulse, which sets all bits of the RAM to logic zero. The fast address to match and data to match times provided by the 8780 allow design of high speed cache memory systems required for fast CISC and RISC processors. The reset feature allows fast cache flushing for task switching and logical cache designs. The 8780 is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. Excellent latch-up and ESD protection are also provided.

FUNCTIONAL BLOCK DIAGRAM



X = Don't Care for inputs, Undefined for MATCH output

PIN CONFIGURATIONS



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O 1-4	I/O	Data
CLR	I	RAM Reset/Clear
WE	I	Write Enable
OE	I	Output Enable
MATCH	O	Comparator Output

FUNCTION TABLE

CLR	OE	WE	I/O	RAM	MATCH	Function
L	X	X	High-Z	Low	X	Clear RAM to all low (zero)
H	H	H	Data In	= Data In	H	Match Compare Valid
H	H	H	Data In	≠ Data In	L	Match Compare Invalid
H	L	H	Data Out	Data Out	H	Read
H	X	L	Data In	Data In	H	Write

X = Don't Care for inputs, Undefined for MATCH output

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V				
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$				
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$				
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V				
DC Output Current Max. sink current/pin.....	50 mA				
DC Output Current Max. source current/pin.....	30 mA				
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C				
T_{STG} Storage Temperature, COM.....	-65° to +125°C				
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C				
T_{STG} Storage Temperature, MIL.....	-65° to +155°C				

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
C_{in}	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
C_{in}	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
C_{out}	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.		7	pF
C_{out}	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

- Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open f = f MAX	145	165	135	155	125	145	120	140	110	130	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10%
See Match Timing Diagrams.

Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter (1)	-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max
MATCH CYCLE									
t AM	Address to Match Time	-	12	-	15	-	20	-	25
t HAM	Match Valid Hold from Address	2	-	2	-	2	-	2	-
t DM	Data to Match Time	-	7.2	-	9	-	12	-	15
t HDM	Match Valid Hold from Data	1	-	1	-	1	-	1	-
t OM	$\overline{OE}$ high to Match valid	-	12	-	15	-	20	-	25
t HOM	Match hold from $\overline{OE}$	0	-	0	-	0	-	0	-
t WM	$\overline{WE}$ high to Match valid	-	12	-	15	-	20	-	25
t HWM	Match hold from $\overline{WE}$	0	-	0	-	0	-	0	-
CLEAR CYCLE									
t CLRW	$\overline{CLR}$ Pulse Width	-	50	-	50	-	50	-	50
t CLRR	$\overline{CLR}$ Recovery Time CLR High to $\overline{WE}$ Low	10	-	10	-	10	-	10	-

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

QS8780

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE									
t RC	Read Cycle Time	12	-	15	-	19	-	25	-
t AA	Address Access Time	-	12	-	15	-	19	-	25
t OH	Output Hold from Address Change	2	-	2	-	3	-	3	-
t OE	Output Enable to Data Valid	-	6	-	6	-	8	-	10
t OLZ	Output Enable to Output in Low Z (2)	2	-	2	-	2	-	2	-
t OHZ	Output Enable to Output in High Z (2)	-	4	-	5	-	7	-	8

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

QS8780

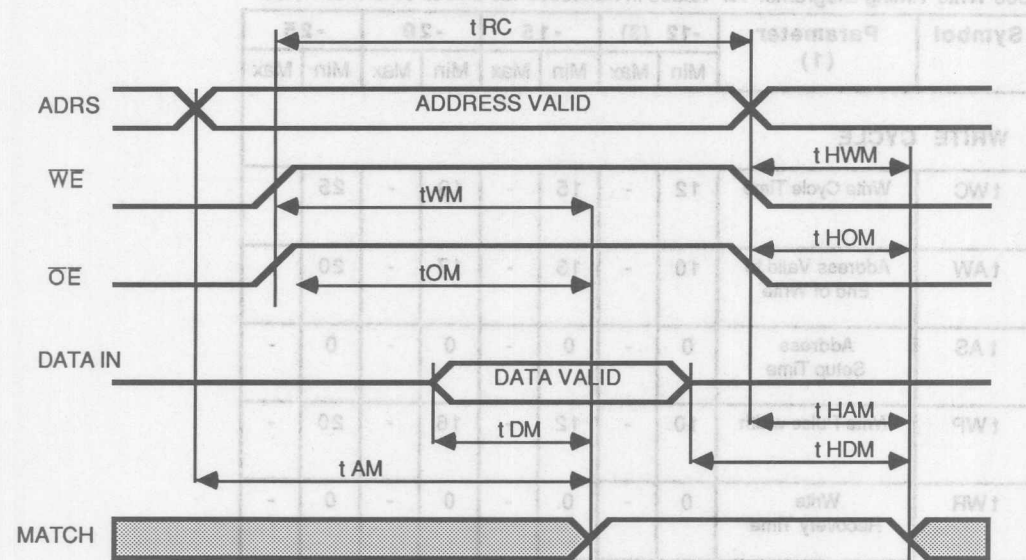
Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE									
t WC	Write Cycle Time	12	-	15	-	19	-	25	-
t AW	Address Valid to End of Write	10	-	13	-	17	-	20	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-
t WP	Write Pulse width	10	-	12	-	16	-	20	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	7	-	8	-	10	-	13	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	5	-	6	-	7	-	8
t OW	Output Active from End of Write (2)	2	-	2	-	2	-	2	-

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

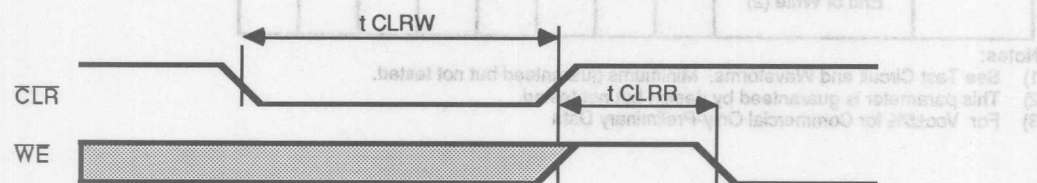
TIMING WAVEFORMS - MATCH CYCLE (1)



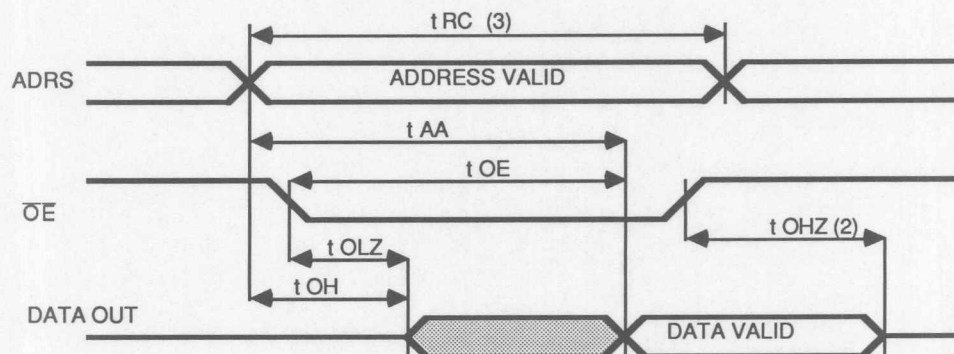
Notes:

1. WE, OE are high for Match cycle.

TIMING WAVEFORMS - CLEAR CYCLE



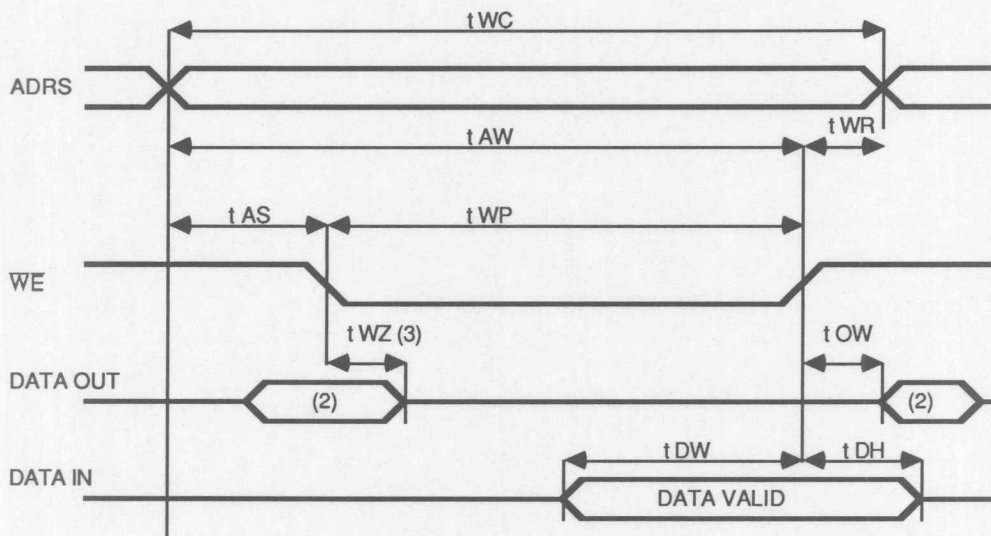
TIMING WAVEFORMS - READ CYCLE NO. 1 (1)



Notes:

1. WE is high for Read cycle.
2. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
3. All read timings are referenced from the last valid address to the first transitioning address.

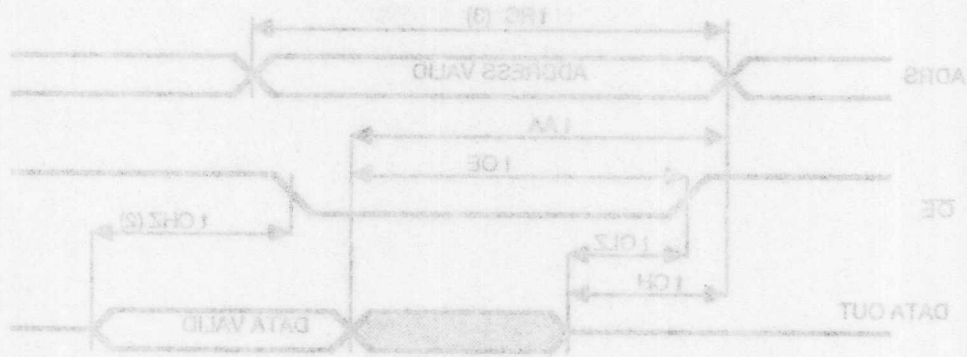
TIMING WAVEFORMS-WRITE CYCLE (1)



Notes:

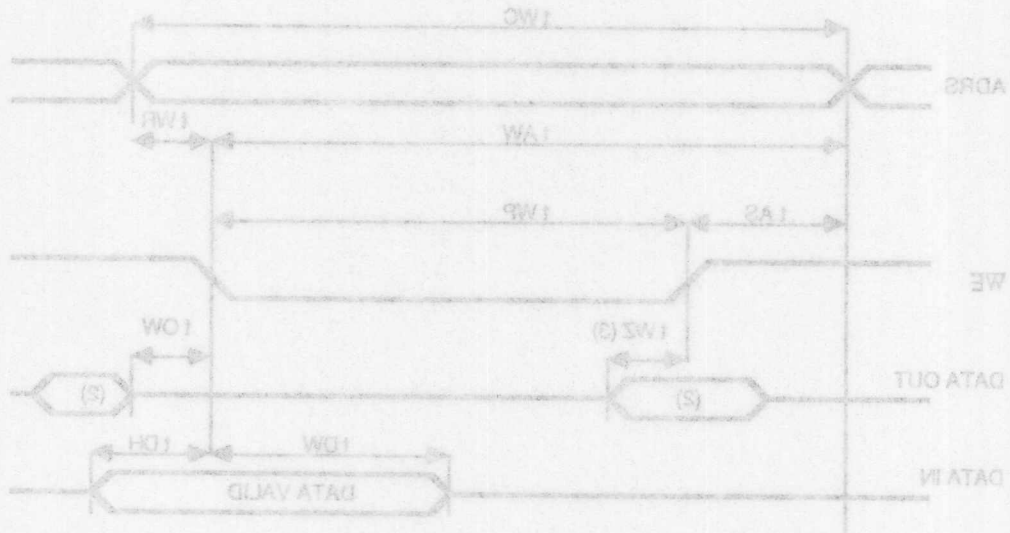
1. WE must be high during address transitions.
2. During this period the I/O pins are in the output state and input signals must not be applied.
3. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.

TIMING WAVEFORMS - READ CYCLE NO. 1 (t)



- Notes:
1. WE is high for Read cycle.
 2. Transition to HI-Z is measured ± 200 mV change from the previous steady state voltage.
 3. All read timings are referenced from the first valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE (t)



- Notes:
1. WE must be high during address transitions.
 2. During this period the I/O pins are in the output state and input signals must not be applied.
 3. Transition to HI-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 16Kx4 SRAM with Separate I/O

QS8881
QS8882

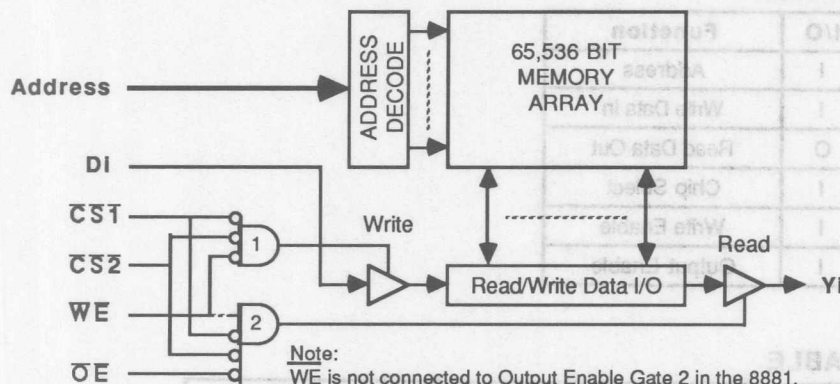
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 10ns/12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 28-pin DIPs, 28-pin 300 mil SOJ, 28-pin LCC
- Low Standby current
- JEDEC standard pinout

DESCRIPTION

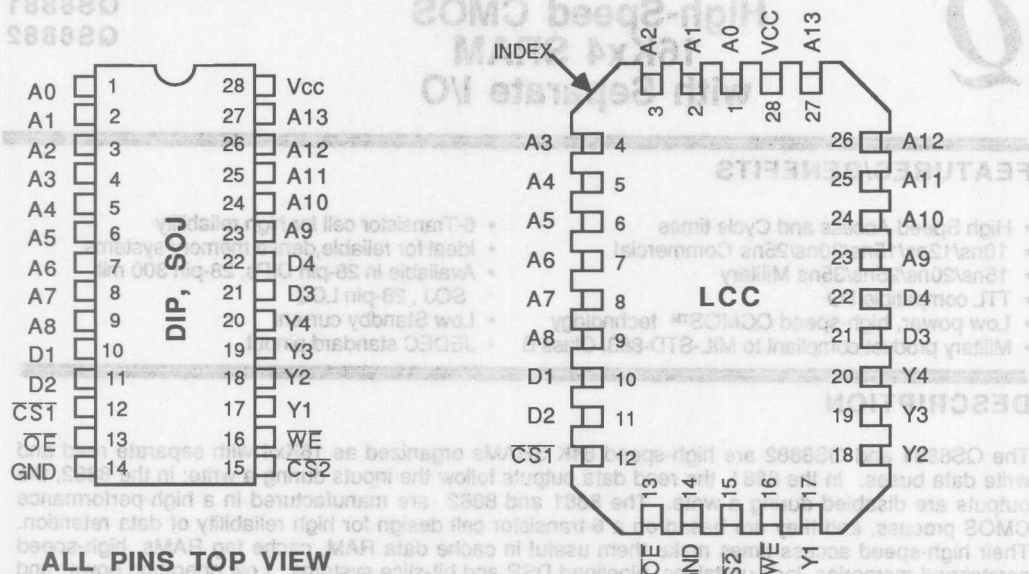
The QS8881 and QS8882 are high-speed 64K SRAMs organized as 16Kx4 with separate read and write data buses. In the 8881, the read data outputs follow the inputs during a write; in the 8882, the outputs are disabled during a write. The 8881 and 8882 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



	8881	8882				
Standby	High Z	High Z	X	X	H	
Standby	High Z	High Z	X	H	X	
Read	Active	Data Out	H	L	L	
Write	Active	Data In	L	L	L	

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin	Name	I/O	Function
A	I		Address
D	I		Write Data In
Y	O		Read Data Out
CS	I		Chip Select
WE	I		Write Enable
OE	I		Output Enable

FUNCTION TABLE

CS1	CS2	WE	Y Outputs		Power	Function
			8881	8882		
H	X	X	High Z	High Z	Standby	Deselect
X	H	X	High Z	High Z	Standby	Deselect
L	L	H	Data Out	Data Out	Active	Read
L	L	L	Data In	High Z	Active	Write

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$	Parameter	Symbol
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA	Input HIGH Voltage	V_{IH}
DC Output Current Max. source current/pin.....	30 mA	Input LOW Voltage (1)	V_{IL}
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C	Output HIGH Voltage	V_{OH}
T_{STG} Storage Temperature, COM.....	-65° to +125°C	Output LOW Voltage	V_{OL}
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Capacitance is guaranteed by design but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	165	135	155	125	145	120	140	110	130	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	60	70	60	70	60	70	60	70	60	70	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10 (3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE													
t _{RC}	Read Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t _{AA}	Address Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t _{ACS}	Chip Select Access Time	-	10	-	12	-	15	-	19	-	25	-	35
t _{OH}	Output Hold from Address Change	2	-	2	-	2	-	3	-	3	-	3	-
t _{CLZ}	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-	3	-
t _{CHZ}	Chip Select to Output in High Z (2)	-	5	-	5	-	7	-	8	-	10	-	15
t _{OE}	Output Enable to Data Valid	-	5	-	6	-	6	-	8	-	10	-	18
t _{OLZ}	Output Enable to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-	3	-
t _{OHZ}	Output Enable to Output in High Z (2)	-	4	-	4	-	5	-	7	-	8	-	15
t _{PU}	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-	0	-
t _{PD}	Chip Select to Power Down Time (2)	10	-	12	-	15	-	19	-	25	-	35	-

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

QS8881, QS8882

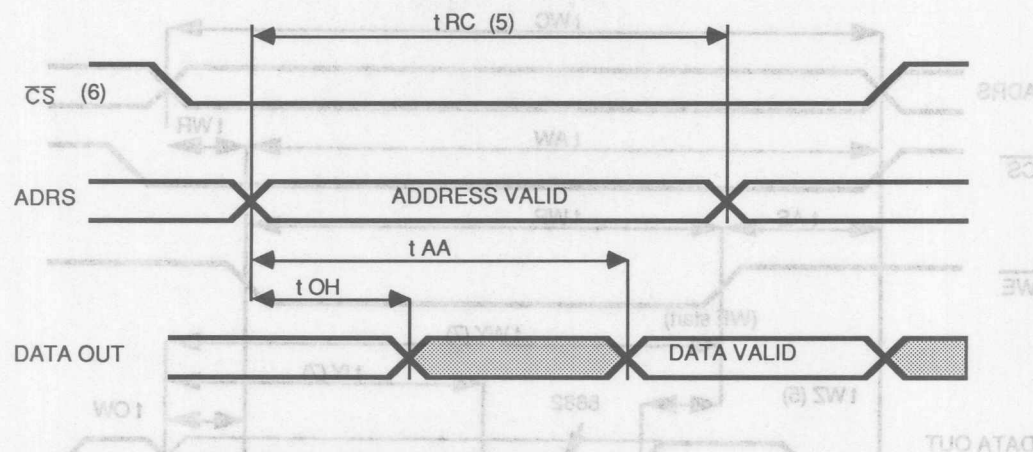
Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10 (3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE													
t WC	Write Cycle Time	10	-	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	8	-	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	8	-	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	5	-	6	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in Hi Z (2,4)	-	4	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write (4)(2)	2	-	2	-	2	-	2	-	2	-	3	-
t IY	Data to Output Delay (5)	-	8	-	10	-	12	-	15	-	20	-	25
t WY	Write Enable to Output Delay (5)	-	8	-	10	-	12	-	15	-	20	-	25

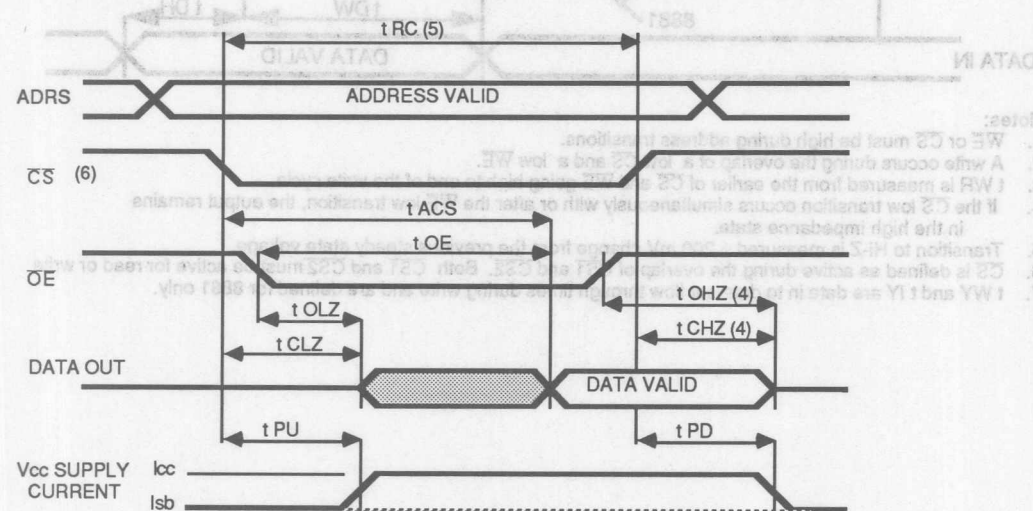
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data
- 4) 8882 Only. (8881 outputs remain on during write.)
- 5) 8881 Only. (8882 outputs go to Hi-Z during write.)

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,6)



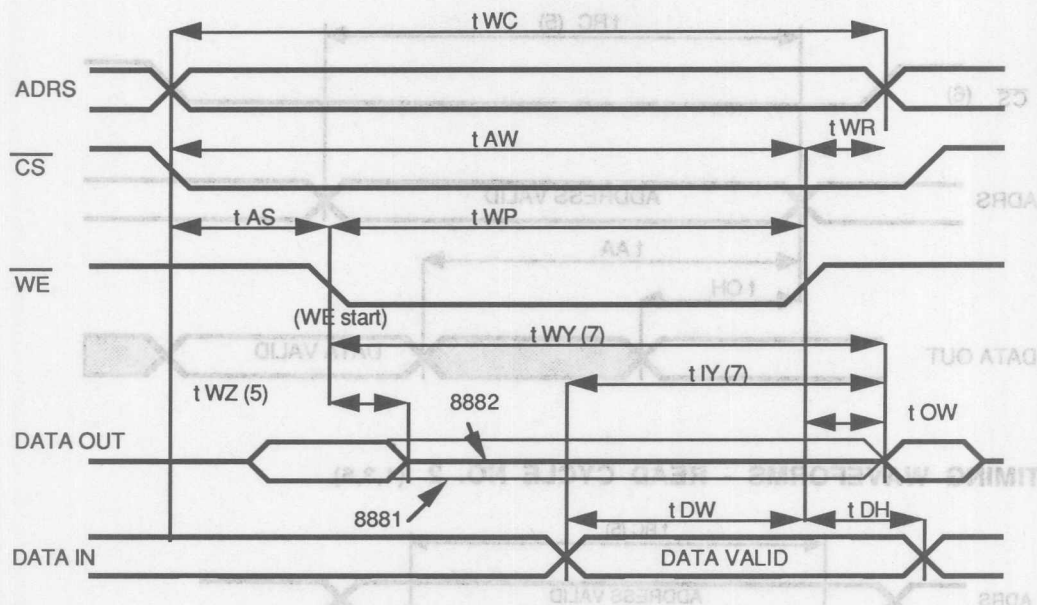
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3,6)



Notes:

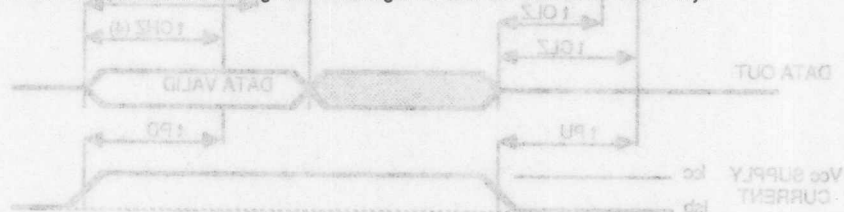
1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.
6. CS is defined as active during the overlap of CS1 and CS2. Both CS1 and CS2 must be active for read or write.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3,6 WE controlled timing)

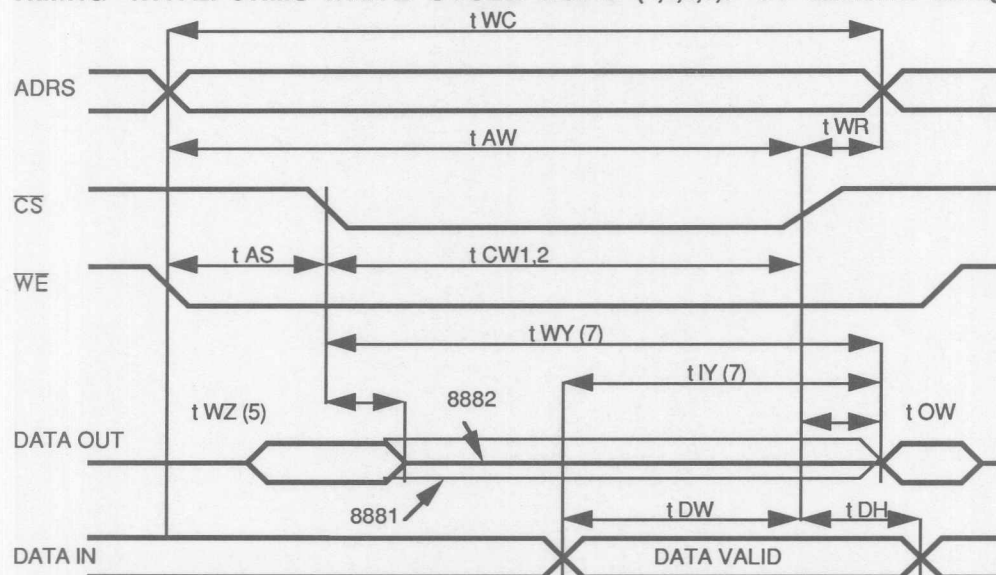


Notes:

1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.
6. $\overline{CS}$ is defined as active during the overlap of $\overline{CS1}$ and $\overline{CS2}$. Both $\overline{CS1}$ and $\overline{CS2}$ must be active for read or write.
7. t_{WY} and t_{IY} are data in to data out flow through times during write and are defined for 8881 only.



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,4,6 $\overline{CS}$ controlled timing)



Notes:

1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.
6. $\overline{CS}$ is defined as active during the overlap of $\overline{CS1}$ and $\overline{CS2}$. Both $\overline{CS1}$ and $\overline{CS2}$ must be active for read or write.
7. t_{WY} and t_{IY} are data in to data out flow through times during write and are defined for 8881 only.



High-Speed CMOS 16Kx4 Cache Tag SRAM

QS8883

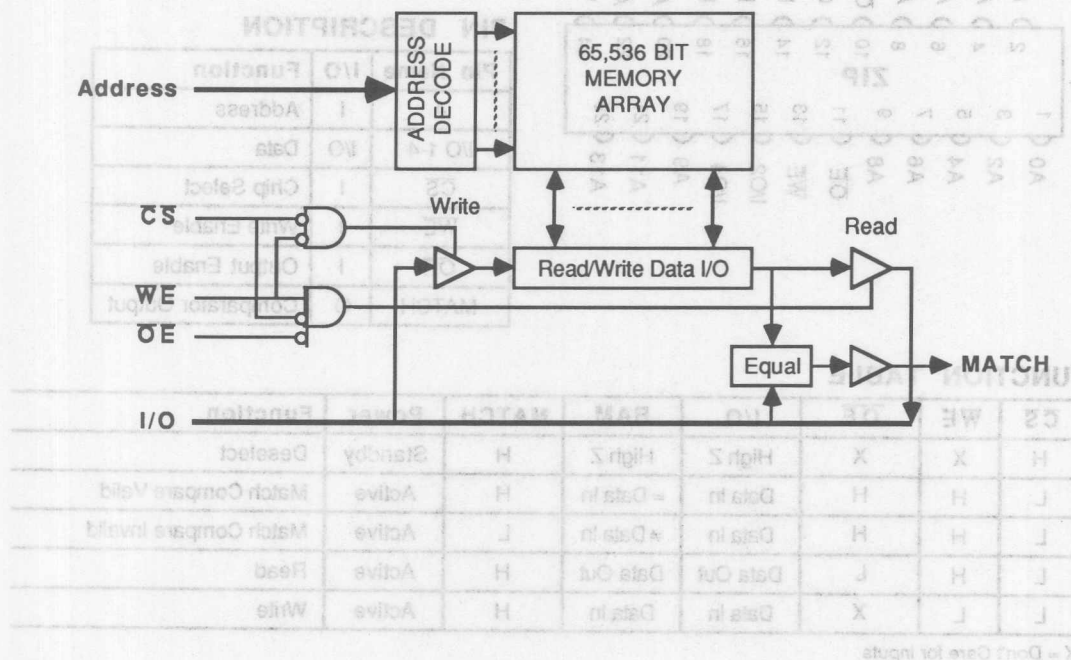
FEATURES/BENEFITS

- High Speed Match Access and Cycle times
- 10ns, 12ns/15ns/20ns/25ns/35ns Commercial
- 15ns/20ns/25ns/35ns/45ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS® technology
- MATCH output goes high on match
- TTL level MATCH output
- Available in 24-pin DIPs, 24-pin ZIP
- 24-pin 300 mil, SOJ, 28-pin LCC, QSOP
- 6-Transistor cell for high reliability

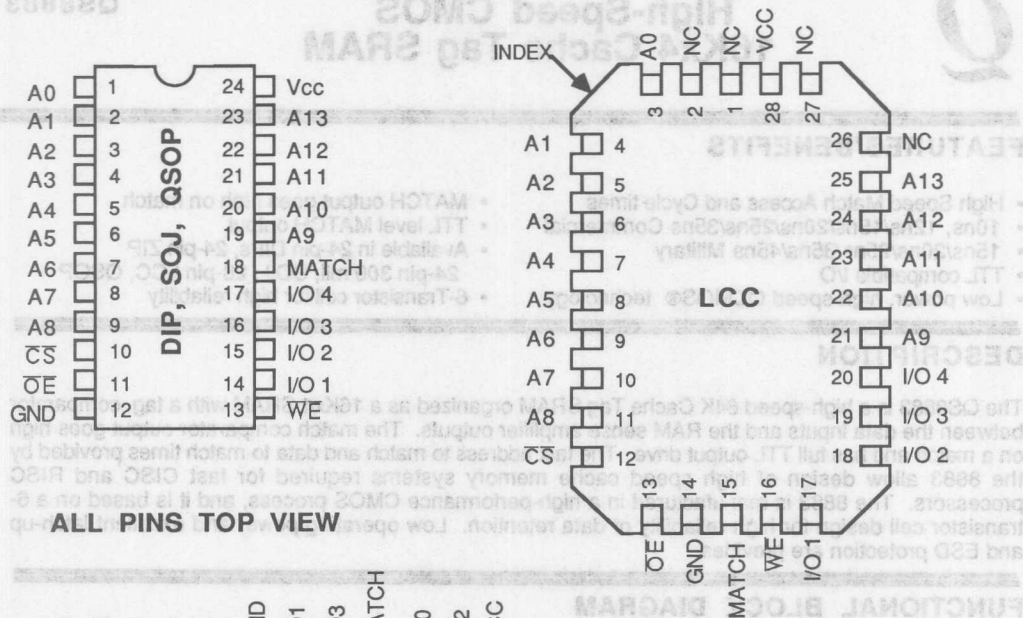
DESCRIPTION

The QS8883 is a high-speed 64K Cache Tag SRAM organized as a 16Kx4 SRAM with a tag comparator between the data inputs and the RAM sense amplifier outputs. The match comparator output goes high on a match and has full TTL output drive. The fast address to match and data to match times provided by the 8883 allow design of high speed cache memory systems required for fast CISC and RISC processors. The 8883 is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. Low operating power and excellent latch-up and ESD protection are provided.

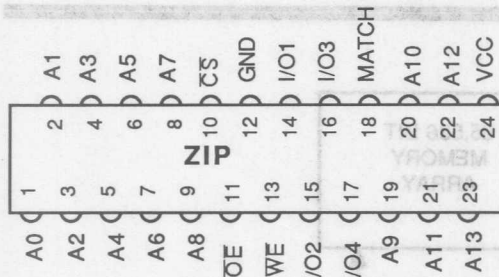
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW



PIN DESCRIPTION

Pin	Name	I/O	Function
A	A	I	Address
I/O 1-4	I/O 1-4	I/O	Data
$\overline{CS}$	$\overline{CS}$	I	Chip Select
WE	WE	I	Write Enable
$\overline{OE}$	$\overline{OE}$	I	Output Enable
MATCH	MATCH	O	Comparator Output

FUNCTION TABLE

$\overline{CS}$	WE	$\overline{OE}$	I/O	RAM	MATCH	Power	Function
H	X	X	High Z	High Z	H	Standby	Deselect
L	H	H	Data In	= Data In	H	Active	Match Compare Valid
L	H	H	Data In	≠ Data In	L	Active	Match Compare Invalid
L	H	L	Data Out	Data Out	H	Active	Read
L	L	X	Data In	Data In	H	Active	Write

X = Don't Care for inputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to V_{CC} + 0.5V
DC Input Voltage V_I	-0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Output Current Max. sink current/pin.....	50 mA
DC Output Current Max. source current/pin.....	30 mA
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C
T_{STG} Storage Temperature, COM.....	-65° to +125°C
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C
T_{STG} Storage Temperature, MIL.....	-65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10		-12		-15		-20		-25		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	165	135	155	125	145	120	140	115	135	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	60	70	60	70	60	70	60	70	60	70	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%

See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10(3)		-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
MATCH CYCLE											
t AM	Address to Match Time	-	10	-	12	-	15	-	20	-	25
t HAM	Match Valid Hold from Address	2	-	2	-	3	-	3	-	3	-
t DM	Data to Match Time	-	6	-	7.2	-	9	-	12	-	15
t HDM	Match Valid Hold from Data	1	-	1	-	1	-	1	-	1	-
t CM	Chip Select to MATCH Valid	-	10	-	12	-	15	-	20	-	25
t HCM	Match Valid Hold from Chip Select	2		2		2		2		2	
t OM	$\overline{OE}$ High to Match Valid		8		10		12		15		20
t HOM	Match Valid Hold from Output Enable	0		0		0		0		0	
t WM	$\overline{WE}$ High to Match Valid		10		12		15		20		25
t HWM	Match Valid Hold from Write Enable	0		0		0		0		0	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

QS8883

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter	-10 (3)		-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE											
t RC	Read Cycle Time	10	-	12	-	15	-	19	-	25	-
t AA	Address Access Time	-	10	-	12	-	15	-	19	-	25
t ACS	Chip Select Access Time	-	10	-	12	-	15	-	19	-	25
t OH	Output Hold from Address Change	2	-	2	-	2	-	3	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-
t CHZ	Chip Select to Output in High Z (2)	-	4	-	5	-	7	-	8	-	10
t OE	Output Enable to Data Valid	-	5	-	6	-	6	-	8	-	10
t OLZ	Output Enable to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-
t OHZ	Output Enable to Output in High Z (2)	-	4	-	4	-	5	-	7	-	8
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	10	-	12	-	15	-	19	-	25	-

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only.

QS8883

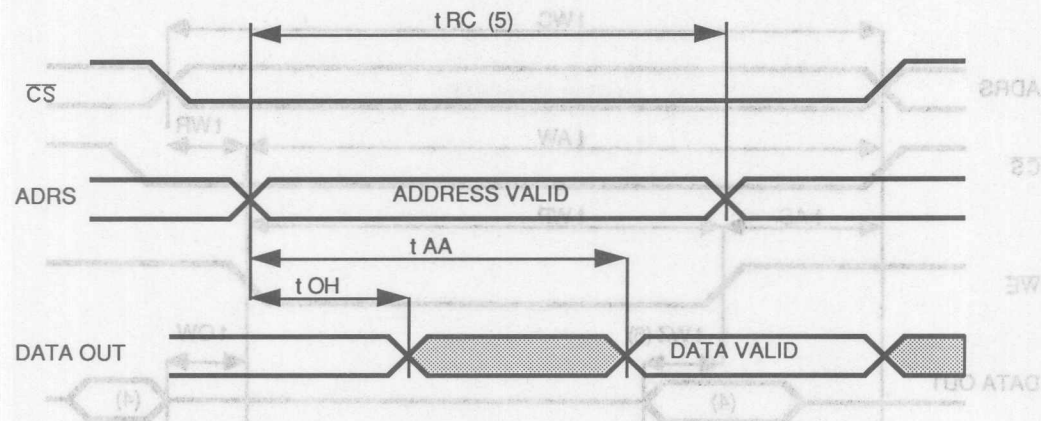
Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-10 (3)		-12 (3)		-15		-20		-25	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	10	-	12	-	15	-	19	-	25	-
t CW	Chip Select Valid to End of Write	8	-	10	-	13	-	17	-	20	-
t AW	Address Valid to End of Write	8	-	10	-	13	-	17	-	20	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width		-	10	-	12	-	16	-	20	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write		-	6	-	8	-	10	-	13	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-		-	5	-	6	-	7	-	8
t OW	Output Active from End of Write (2)		-	2	-	2	-	2	-	2	-

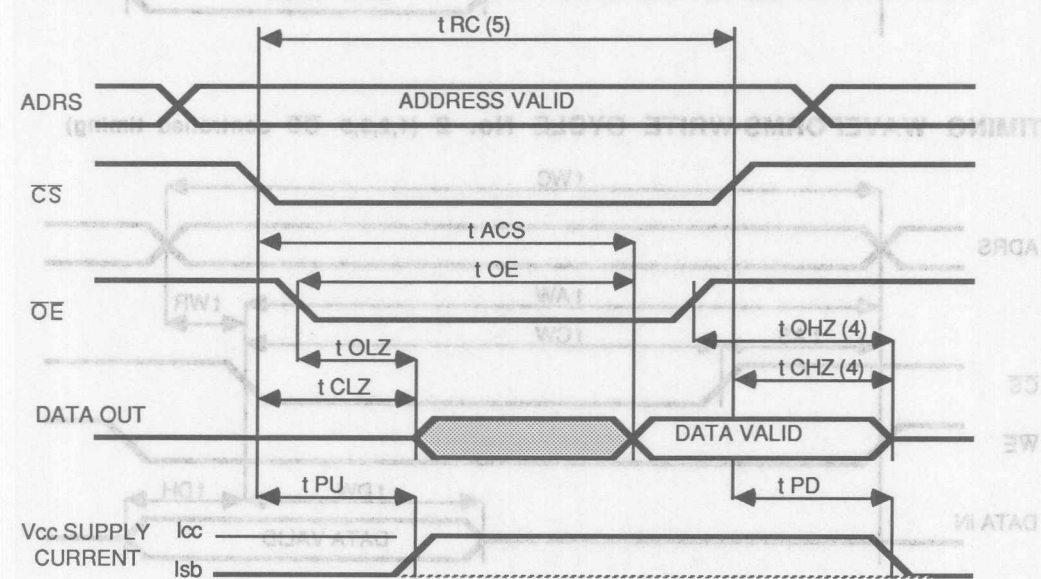
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% for Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



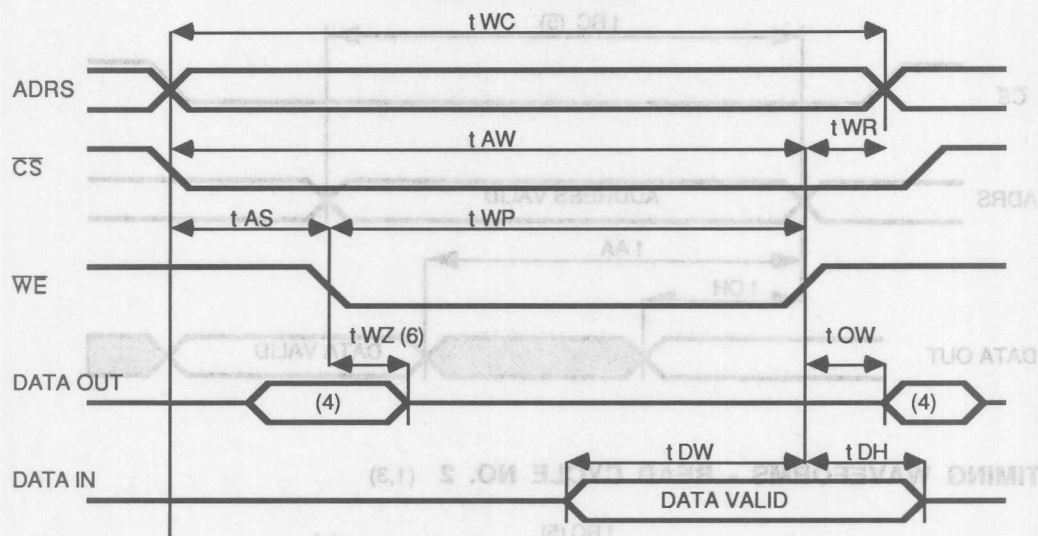
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



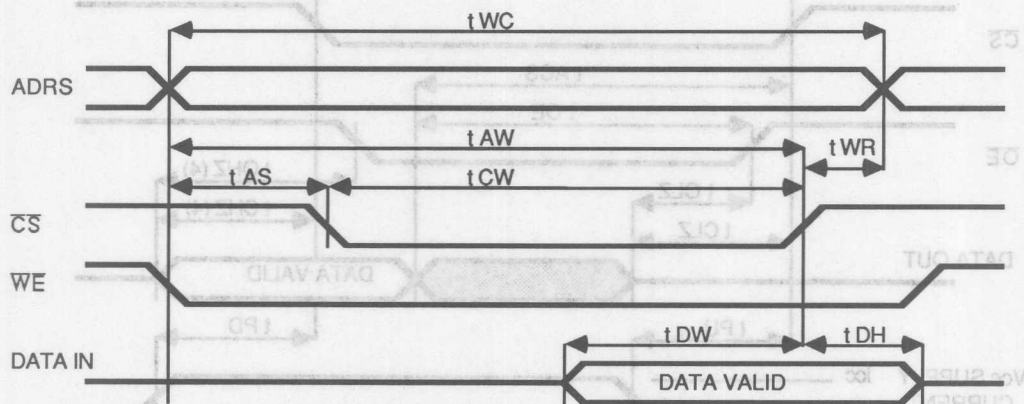
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.

Q

High-Speed CMOS 16Kx4 SRAM with Output Enable

QS8885
QS8886

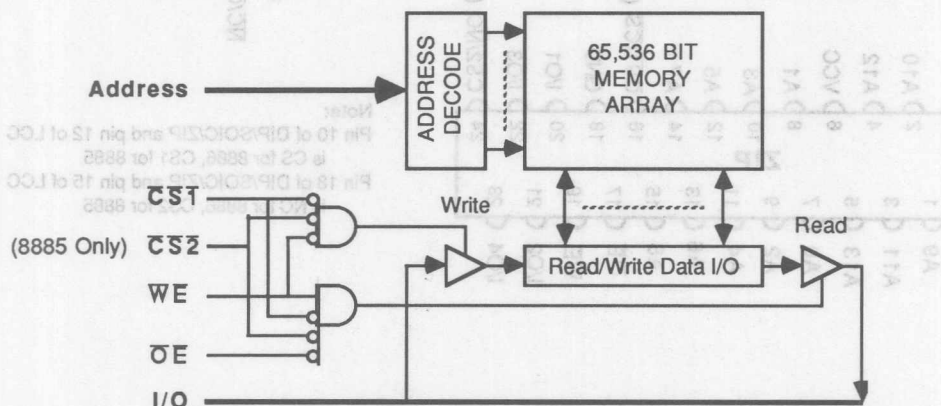
- High Speed Access and Cycle times
- 8ns/10ns/12ns/15ns/20ns/25ns Commercial
- 12ns/15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 24-pin DIPs, 24-pin ZIP, 24-pin 300 mil SOJ, 28-pin LCC & QSOP
- Low Standby current
- JEDEC standard pinout

DESCRIPTION

The QS8885 and QS8886 are high-speed 64K SRAMs organized as 16Kx4. The 8885 has two chip selects, and both have output enable. The 8885 and 8886 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

2

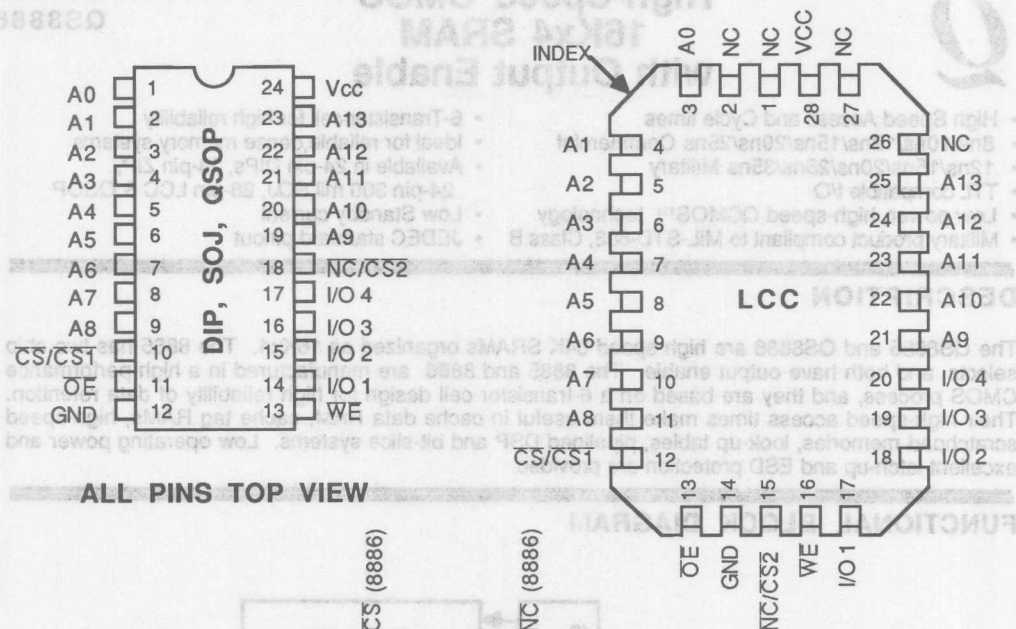
FUNCTIONAL BLOCK DIAGRAM



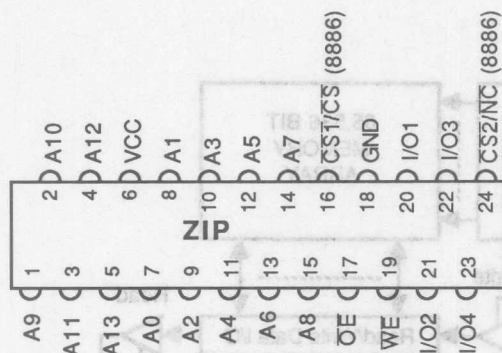
Function	Power	I/O	WE	CS1	CS2
Standby	High Z	High Z	X	X	H
Standby	High Z	High Z	X	H	X
Read	Active	Data Out	H	L	L
Write	Active	Data In	L	L	L

Pin Name	I/O	Function
A	I	Address
VO 1-4	NO	Data
CS1, CS2	I	Chip Select
WE	I	Write Enable
OE	I	Output Enable

PIN CONFIGURATIONS



ALL PINS TOP VIEW



Note:
Pin 10 of DIP/SOIC/ZIP and pin 12 of LCC is CS for 8886, CS1 for 8885
Pin 18 of DIP/SOIC/ZIP and pin 15 of LCC is NC for 8886, CS2 for 8885

PIN DESCRIPTION

Pin	Name	I/O	Function
A		I	Address
I/O 1-4		I/O	Data
CS, CS1/2		I	Chip Select
WE		I	Write Enable
OE		I	Output Enable

FUNCTION TABLE

CS1	CS2	WE	I/O	Power	Function
H	X	X	High Z	Standby	Deselect
X	H	X	High Z	Standby	Deselect
L	L	H	Data Out	Active	Read
L	L	L	Data In	Active	Write

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to V_{CC} + 0.5V DC		
Input Voltage V_I	-0.5V to V_{CC} + 0.5V		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA		
DC Output Current Max. source current/pin.....	30 mA		
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C		
T_{STG} Storage Temperature, COM.....	-65° to +125°C		
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	- 8		- 10		- 12		15		-20		-25/-35		Unit
		C	C	M	C	M	C	M	C	M	C	M		
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	110	100	120	100	120	100	120	100	120	100	120	mA	
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	160	145	165	135	155	125	145	120	140	110	130		
I _{sb}	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	70	60	70	60	70	60	70	60	70	60	70		
I _{sb1}	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	20	15	20	15	20	15	20	15	20	15	20		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-8(3)		-10(3)		-12		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE															
t RC	Read Cycle Time	8	-	10	-	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	8	-	10	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	8	-	10	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	1.5	-	2	-	2	-	2	-	3	-	3	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	1.5	-	2	-	2	-	2	-	2	-	2	-	3	-
t CHZ	Chip Select to Output in High Z (2)	-	4	-	4	-	5	-	7	-	8	-	10	-	15
t OE	Output Enable to Data Valid (2)	-	4	-	5	-	6	-	6	-	8	-	10	-	18
t OLZ	Output Enable to Output in Low Z (2)	1.5	-	2	-	2	-	2	-	2	-	2	-	3	-
t OHZ	Output Enable to Output in High Z (2)	-	4	-	4	-	4	-	5	-	7	-	8	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	8	-	10	-	12	-	15	-	19	-	25	-	35	-

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data.

QS8885, QS8886

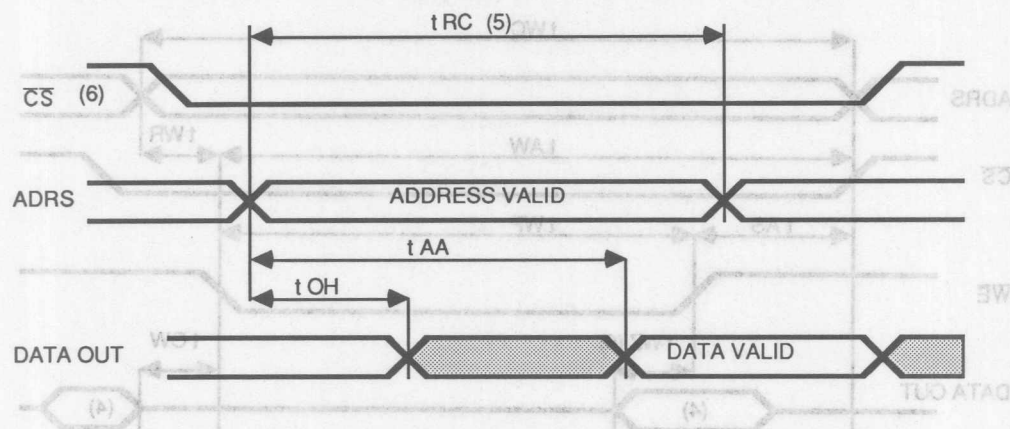
Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-8(3)		-10 (3)		-12		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE															
tWC	Write Cycle Time	8	-	10	-	12	-	15	-	19	-	25	-	35	-
tCW	Chip Select Valid to End of Write	7	-	8	-	10	-	13	-	17	-	20	-	30	-
tAW	Address Valid to End of Write	7	-	8	-	10	-	13	-	17	-	20	-	30	-
tAS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
tWP	Write Pulse width	7	-	8	-	10	-	12	-	16	-	20	-	30	-
tWR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
tDW	Data Valid to End of Write	4	-	5	-	6	-	8	-	10	-	13	-	18	-
tDH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
tWZ	Write Enable to Output in High Z (2)	-	4	-	4	-	5	-	6	-	7	-	8	-	12
tOW	Output Active from End of Write	1.5	-	2	-	2	-	2	-	2	-	2	-	3	-

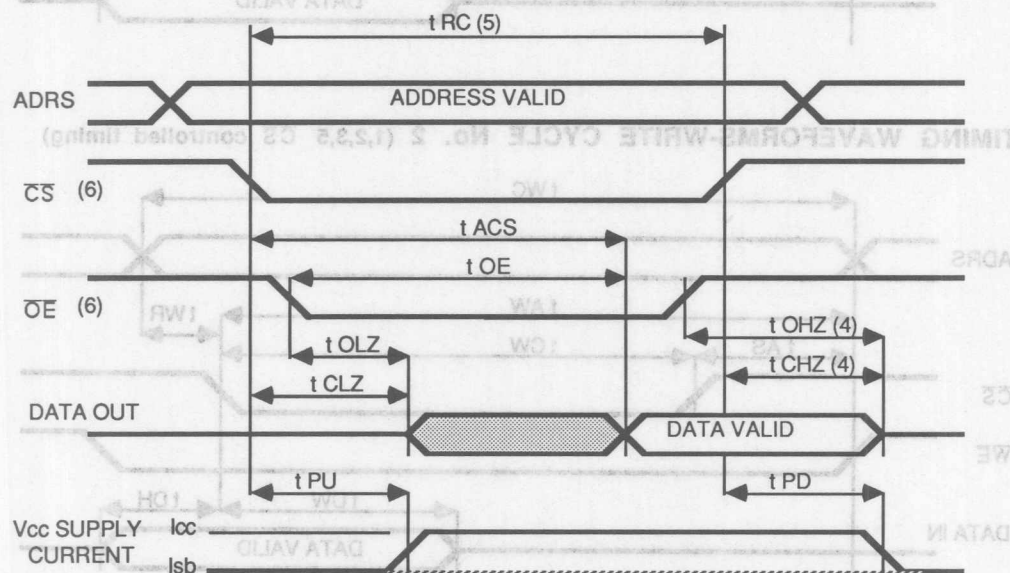
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data.

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,6)



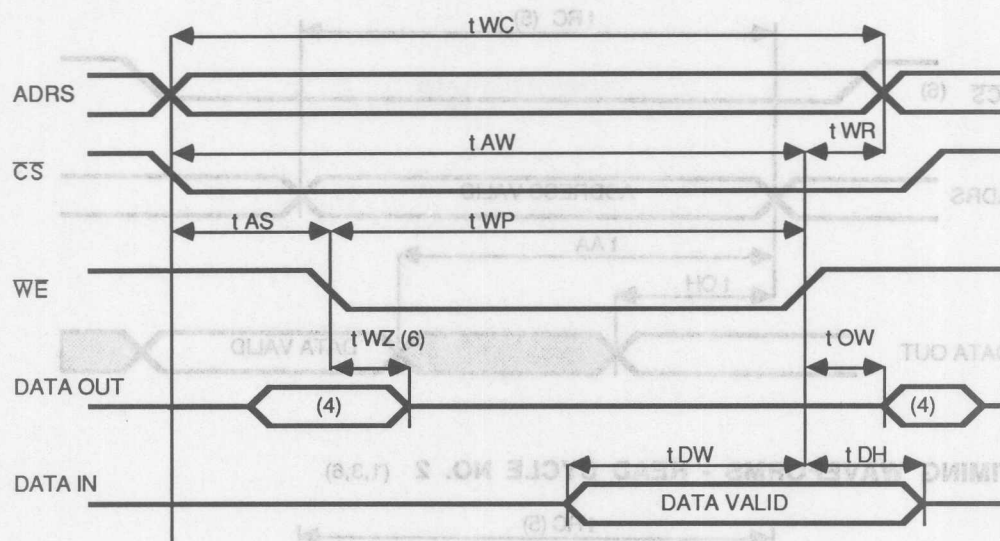
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3,6)



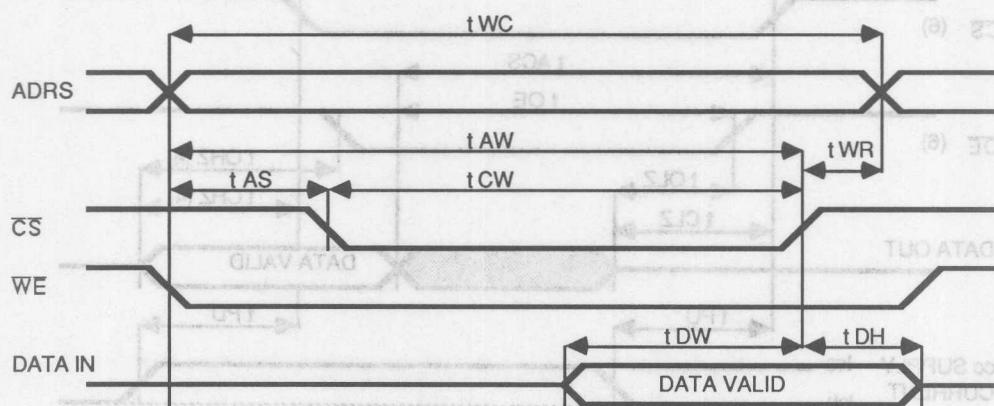
Notes:

1. WE is high for Read cycle.
2. 8886 CS is low for Read cycle #1. Both CS1 and CS2 are low for 8885.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.
6. CS applies to CS on the 8886 and the combination of CS1 and CS2 on the 8885.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.

Q

High-Speed CMOS 16Kx4 SRAM with Common I/O

QS8888

FEATURES/BENEFITS

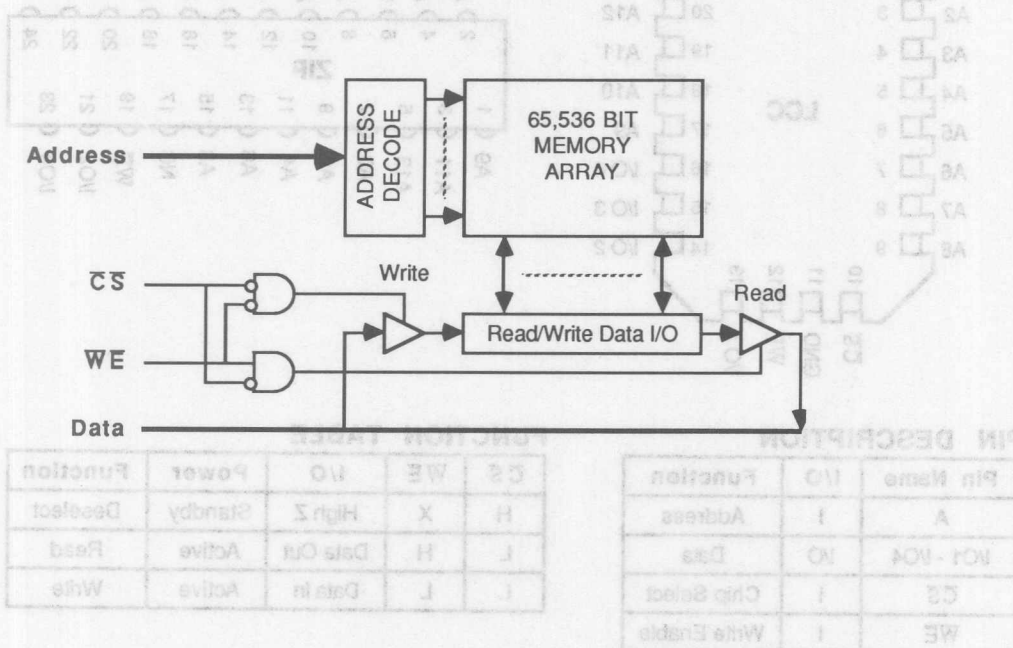
- High Speed Access and Cycle times
- 8ns/10ns/12ns/15ns/20ns/25ns Commercial
- 12ns/15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 22-pin DIPs, 24-pin ZIP, 24-pin 300 mil SOJ, 22-pin LCC, QSOP
- Low Standby current
- JEDEC standard pinout

2

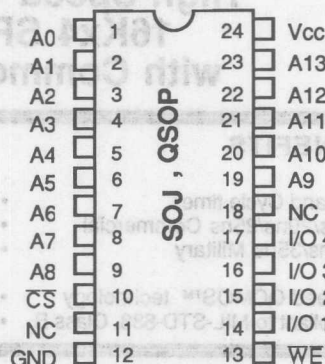
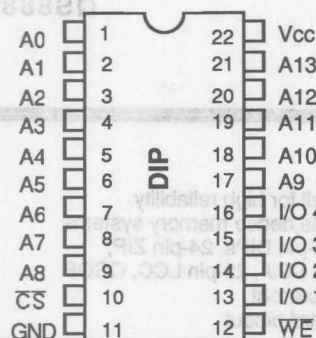
DESCRIPTION

The QS8888 is a high-speed 64K SRAM organized as 16Kx4 . It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS8888 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

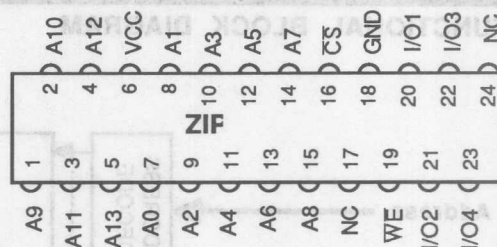
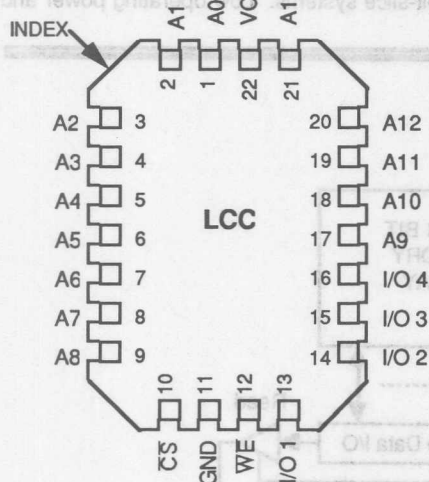
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW



PIN DESCRIPTION

Pin	Name	I/O	Function
A		I	Address
I/O1 - I/O4		I/O	Data
CS		I	Chip Select
WE		I	Write Enable

FUNCTION TABLE

CS	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$	Parameter	Symbol
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA	Input HIGH Voltage	V_{IH}
DC Output Current Max. source current/pin.....	30 mA	Input LOW Voltage (1)	V_{IL}
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C	Output HIGH Voltage	V_{OH}
T_{STG} Storage Temperature, COM.....	-65° to +125°C	Output LOW Voltage	V_{OL}
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
I _{II}	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
I _{lo}	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-8		-10		-12		15		20		25/-35		Unit
		C	C	M	C	M	C	M	C	M	C	M		
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	110	100	120	100	120	100	120	100	120	100	120	mA	
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	160	145	165	135	155	125	145	120	140	110	130		
I _{sb}	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	70	60	70	60	70	60	70	60	70	60	70		
I _{sb1}	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	20	15	20	15	20	15	20	15	20	15	20		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-8(3)		-10(3)		-12 (3)		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE															
t RC	Read Cycle Time	8	-	10	-	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	8	-	10	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	8	-	10	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	1.5	-	2	-	2	-	2	-	3	-	3	-	3	-
t LZ	Chip Select to Output in Low Z (2)	1.5	-	2	-	2	-	2	-	2	-	2	-	3	-
t HZ	Chip Select to Output in High Z (2)	-	4	-	5	-	5	-	7	-	8	-	10	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	-	8	-	10	-	12	-	15	-	19	-	25	-	35

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS8888

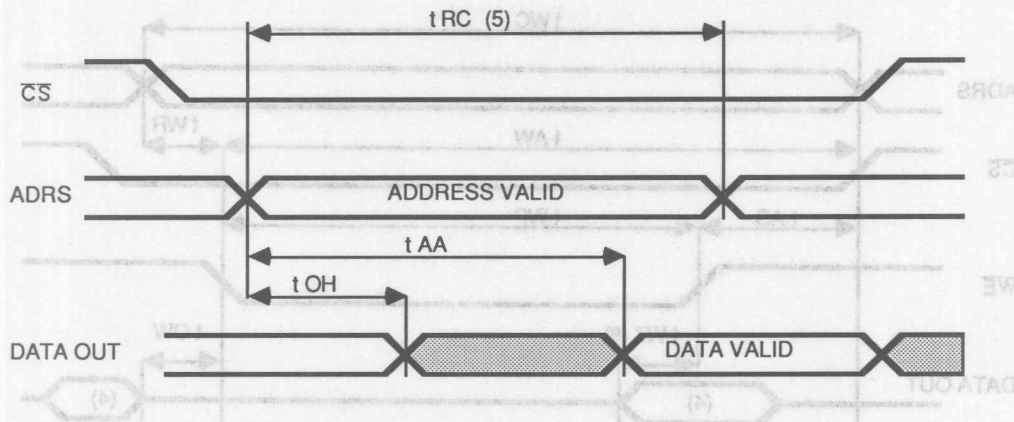
Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	8 (3)		-10 (3)		-12		-15		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE															
t WC	Write Cycle Time	8	-	10	-	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	7	-	8	-	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	7	-	8	-	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	7	-	8	-	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	4	-	5	-	6	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	4	-	4	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write (2)	1.5	-	2	-	2	-	2	-	2	-	2	-	3	-

Notes:

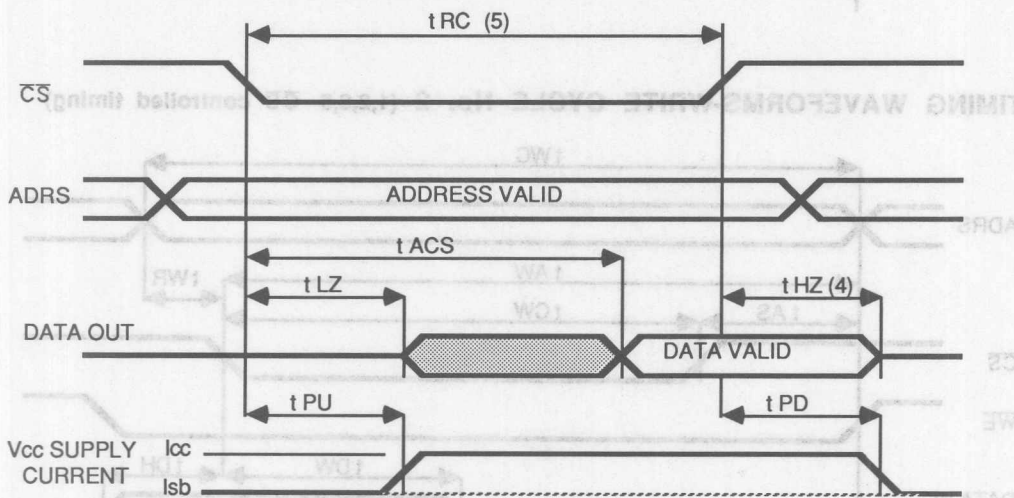
- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



2

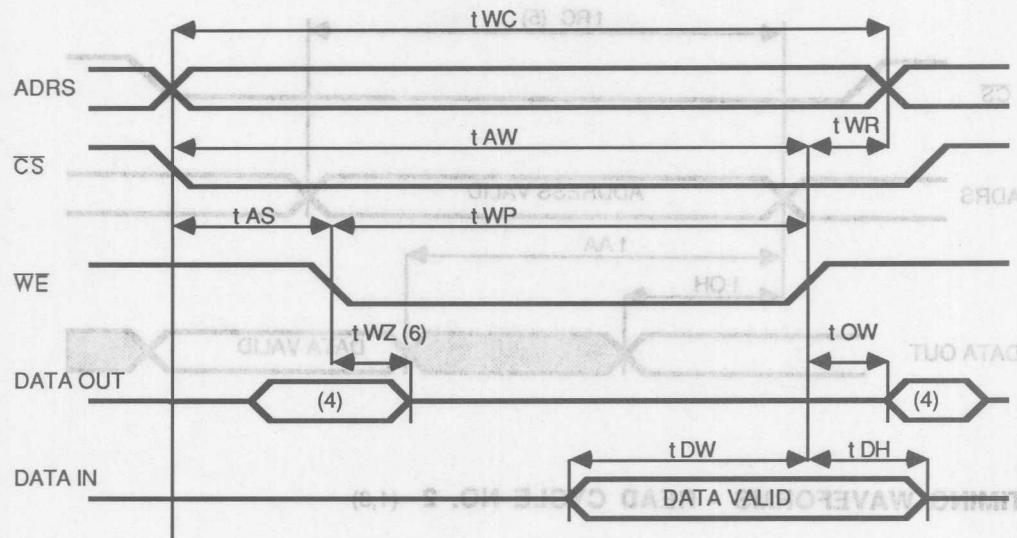
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



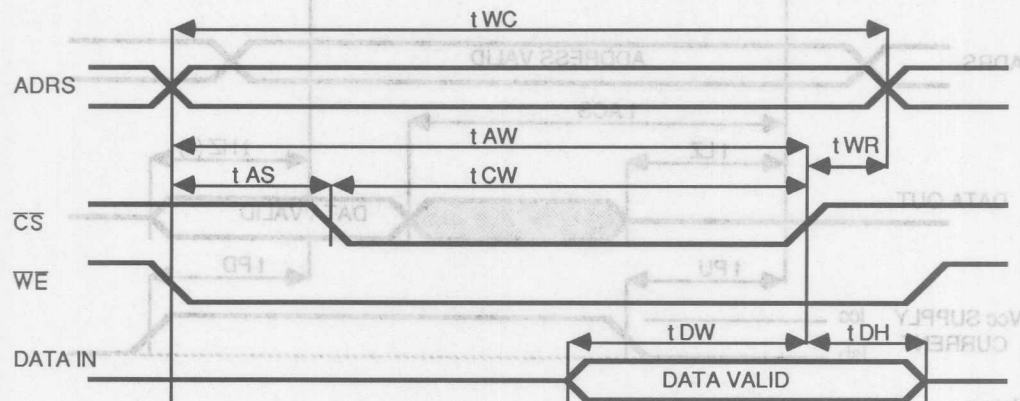
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS Dual 4Kx16/18 SRAM with Latched Addresses

QS88180
QS88160
Preliminary

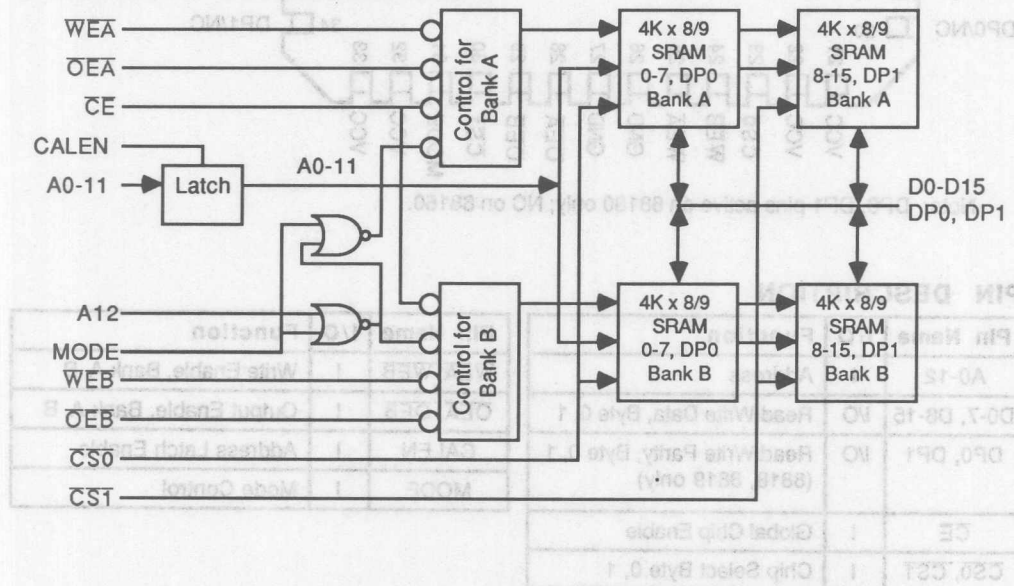
FEATURES/BENEFITS

- Dual 4Kx18/16 allows 2-way set associative cache
- Byte enables for byte/word read/write
- 20ns/25 ns/30ns/35 ns Taa commercial
- 25 ns/30ns/35/45 ns Taa military
- Military product compliant to MIL-STD-883, Class B
- 386/486 compatible
- 6-Transistor cell for high reliability
- Low power, high-speed QCMOS™ technology
- Available in 52-pin PLCC

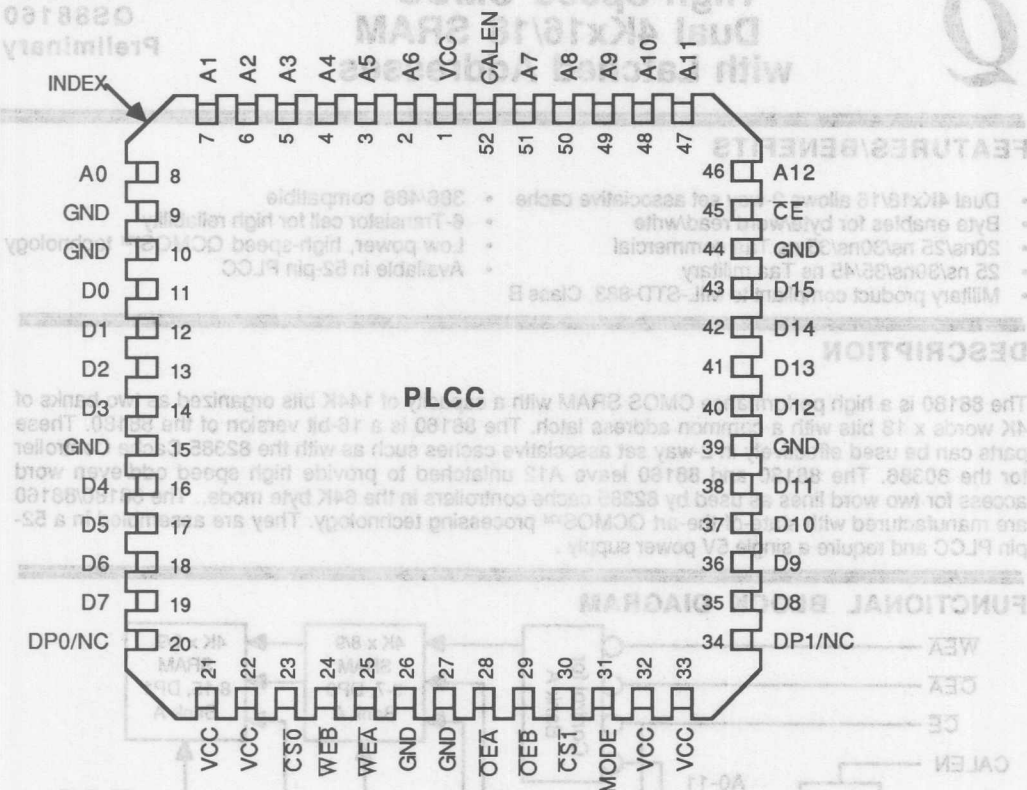
DESCRIPTION

The 88180 is a high performance CMOS SRAM with a capacity of 144K bits organized as two banks of 4K words x 18 bits with a common address latch. The 88160 is a 16-bit version of the 88180. These parts can be used effectively in 2-way set associative caches such as with the 82385 Cache Controller for the 80386. The 88180 and 88160 leave A12 unlatched to provide high speed odd/even word access for two word lines as used by 82385 cache controllers in the 64K byte mode.. The 88180/88160 are manufactured with state-of-the-art QCMOS™ processing technology. They are assembled in a 52-pin PLCC and require a single 5V power supply .

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Note: DP0, DP1 pins active on 88180 only; NC on 88160.

PIN DESCRIPTION

Pin Name	I/O	Function
A0-12	I	Address
D0-7, D8-15	I/O	Read/Write Data, Byte 0, 1
DP0, DP1	I/O	Read/Write Parity, Byte 0, 1 (8818, 8819 only)
$\overline{CE}$	I	Global Chip Enable
$\overline{CS0}$, $\overline{CS1}$	I	Chip Select Byte 0, 1

Pin Name	I/O	Function
$\overline{WEA}$, $\overline{WEB}$	I	Write Enable, Bank A, B
$\overline{OEA}$, $\overline{OEB}$	I	Output Enable, Bank A, B
CALEN	I	Address Latch Enable
MODE	I	Mode Control

FUNCTION TABLE

OPERATION	CONTROL SIGNALS Dual 4K Mode: MODE = H							DATA BUS	
	CE	CS0	CS1	OEA	OEB	WEA	WEB	D0-7, DP0	D8-15, DP1
Chip Disabled	H	X	X	X	X	X	X	Hi - Z	Hi - Z
Bytes Disabled	X	H	H	X	X	X	X	Hi - Z	Hi - Z
Outputs Disabled	X	X	X	H	H	X	X	Hi - Z	Hi - Z
Outputs Disabled	X	X	X	L	L	X	X	Hi - Z	Hi - Z
Read D0-7, DP0 Bank A	L	L	H	L	H	H	H	Data Out	Hi - Z
Read D0-7, DP0 Bank B	L	L	H	H	L	H	H	Data Out	Hi - Z
Read D8-15, DP1 Bank A	L	H	L	L	H	H	H	Hi - Z	Data Out
Read D8-15, DP1 Bank B	L	H	L	H	L	H	H	Hi - Z	Data Out
Read D0-15, DP0 Bank A	L	L	L	L	H	H	H	Data Out	Data Out
Read D0-15, DP0 Bank B	L	L	L	H	L	H	H	Data Out	Data Out
Write D0-7, DP0 Bank A	L	L	H	X	X	L	H	Data In	Hi - Z
Write D0-7, DP0 Bank B	L	L	H	X	X	H	L	Data In	Hi - Z
Write D8-15, DP1 Bank A	L	H	L	X	X	L	H	Hi - Z	Data In
Write D8-15, DP1 Bank B	L	H	L	X	X	H	L	Hi - Z	Data In
Write D0-15, DP1 Bank A	L	L	L	X	X	L	H	Data In	Data In
Write D0-15, DP1 Bank B	L	L	L	X	X	H	L	Data In	Data In
Write D0-7 Banks A&B	L	L	H	X	X	L	L	Data In	Hi - Z
Write D8-15 Banks A&B	L	H	L	X	X	L	L	Hi - Z	Data In
Write D0-15 Banks A&B	L	L	L	X	X	L	L	Data In	Data In

OPERATION	CONTROL SIGNALS 8K Mode: MODE = L							DATA BUS	
	CE	CS0	CS1	OEA	OEB	WEA	WEB	D0-7, DP0	D8-15, DP1
Chip Disabled	H	X	X	X	X	X	X	Hi - Z	Hi - Z
Bytes Disabled	X	H	H	X	X	X	X	Hi - Z	Hi - Z
Outputs Disabled	X	X	X	H	H	X	X	Hi - Z	Hi - Z
Read D0-7, DP0	L	L	H	L	L	H	H	Data Out	Hi - Z
Read D8-15, DP1	L	H	L	L	L	H	H	Hi - Z	Data Out
Read D0-15, DP0, DP1	L	L	L	L	L	H	H	Data Out	Data Out
Write D0-7, DP0	L	L	H	X	X	L	L	Data In	Hi - Z
Write D8-15, DP1	L	H	L	X	X	L	L	Hi - Z	Data In
Write D0-15, DP0, DP1	L	L	L	X	X	L	L	Data In	Data In

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$		
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA		
DC Output Current Max. source current/pin.....	30 mA		
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C		
T_{STG} Storage Temperature, COM.....	-65° to +125°C		
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V		7	pF
Cout	Output Capacitance	Vout = 0 V		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -1 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 4 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter		-20	-25	-30	-35	Unit
Icc2	Standby Current, Addresses Latched Vcc = MAX, Outputs open CE ≥ Vih, CALEN ≤ Vil, f = 0	COM	60	60	60	60	mA
		MIL					
Icc3	Dynamic Operating Current, Addresses Unlatched Vcc = MAX, Outputs open CE ≤ Vil, CALEN ≥ Vih, f = 1/t RC	COM	240	230	230	225	
		MIL					

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted.

Symbol	Parameter	Note (1)	20 ns		25 ns		30 ns		35 ns		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Address Latch Parameters											
t ASL	Address Setup to Latch Low		4		4		4		6		ns
t AHL	Address Hold to Latch Low		5		5		5		5		ns
t CALEN	Latch Enable Pulse width		8		8		8		10		ns
Read Cycle Parameters											
t RC	Read cycle time		20		25		30		35		ns
t AA	Address Access	4	20		25		30		35		ns
t A12A	A12 Address Access		15		17		20		25		ns
t CS t CE	Chip Select Access		20		25		30		35		ns
t OE	Output Enable		8		10		12		14		ns
t OH	Output Hold from Addr	3	3		3		3		3		ns
t OLZ	Output Enable to Low Z	2	2		2		2		2		ns
t LZ	Chip Enable to Low Z	2	3		3		3		3		ns
t OHZ	Output Disable to High Z	2	10		12		15		15		ns
t HZ	Chip Disable to High Z	2	15		17		17		25		ns

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Preliminary Data (Commercial only)
- 4) Measured from address transition when CALEN high or from the low-to-high transition of CALEN.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted.

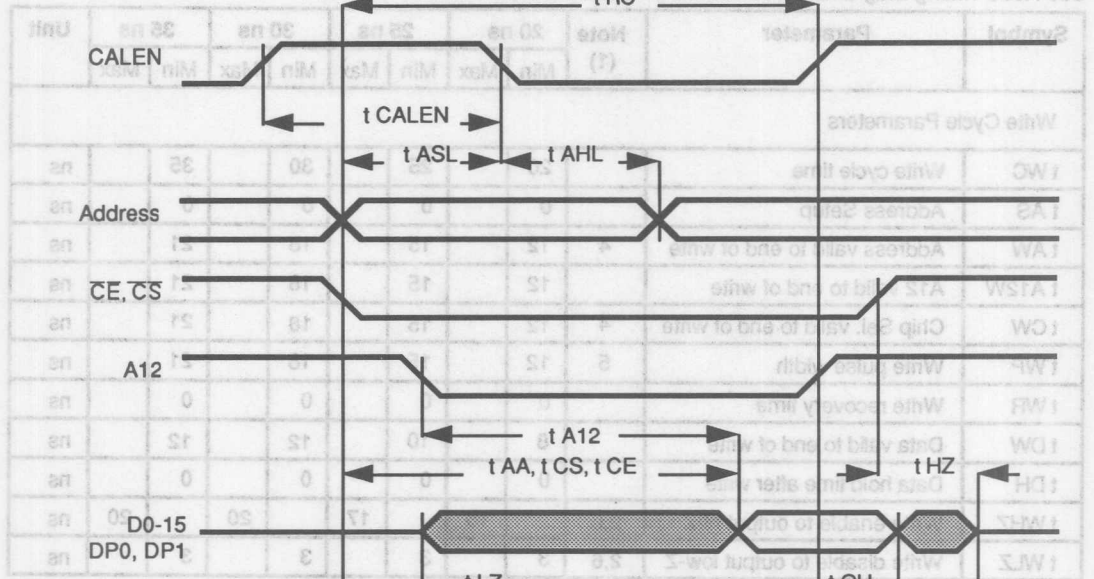
Symbol	Parameter	Note (1)	20 ns		25 ns		30 ns		35 ns		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Parameters											
t WC	Write cycle time		20		25		30		35		ns
t AS	Address Setup		0		0		0		0		ns
t AW	Address valid to end of write	4	12		15		18		21		ns
t A12W	A12 valid to end of write		12		15		18		21		ns
t CW	Chip Sel. valid to end of write	4	12		15		18		21		ns
t WP	Write pulse width	5	12		15		18		21		ns
t WR	Write recovery time		0		0		0		0		ns
t DW	Data valid to end of write		8		10		12		12		ns
t DH	Data hold time after write		0		0		0		0		ns
t WHZ	Write enable to output hi-Z	2,6		15		17		20		20	ns
t WLZ	Write disable to output low-Z	2,6	3		3		3		3		ns

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Preliminary Data (Commercial only)
- 4) Measured from address transition when CALEN high or from the low-to-high transition of CALEN.
- 5) Write occurs during the overlap of WE, CE, and CS. Measurements are made from this overlap.
- 6) If CE, CS, and WE go low simultaneously, the output remains in the Hi-Z state

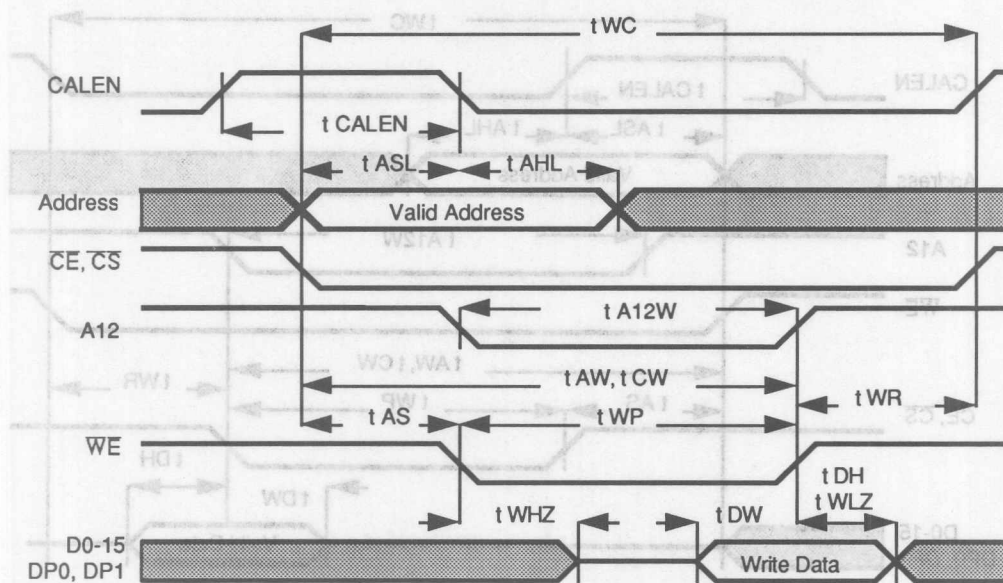
SWITCHING CHARACTERISTICS Read Timing Diagram

Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted.

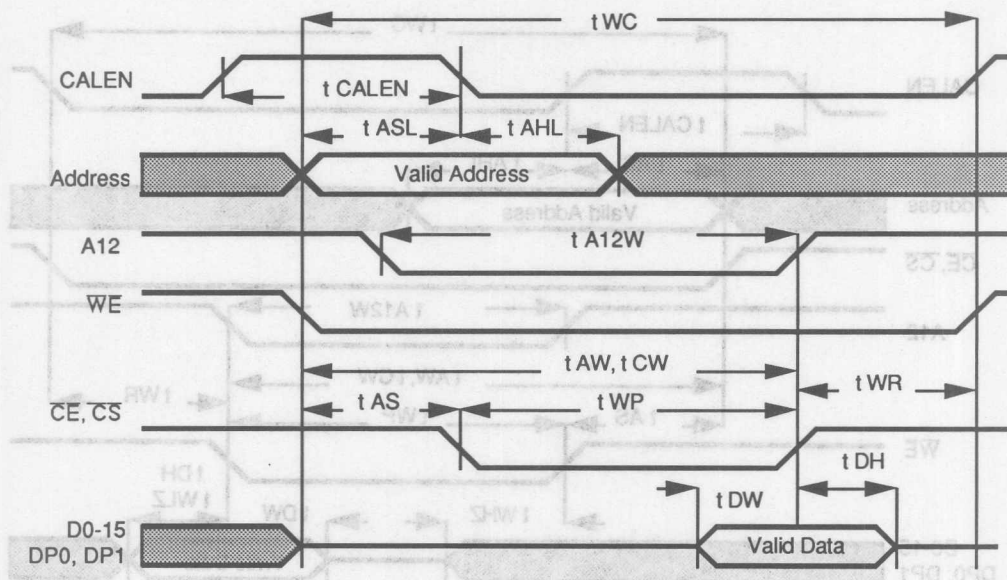


- Notes:
- (1) See circuit and timing diagram for minimum guarantees.
 - (2) The parameter is guaranteed by design but not tested.
 - (3) Preliminary Data (Commercial only).
 - (4) Measured from address transition with CE and CS high to first valid data on D0-15.
 - (5) White occurs during the overlap of WE, CE, and CS. Measurements are made from this overlap.
 - (6) If CE, CS, and WE go low simultaneously, the output remains in the Hi-Z state.

Write Cycle 1 Timing Diagram - WE Controlled Write



Write Cycle 2 Timing Diagram - CE Controlled Write





High-Speed CMOS 8Kx18 Burst Mode SRAM with Address Counter

**QS88181
ADVANCE
INFORMATION**

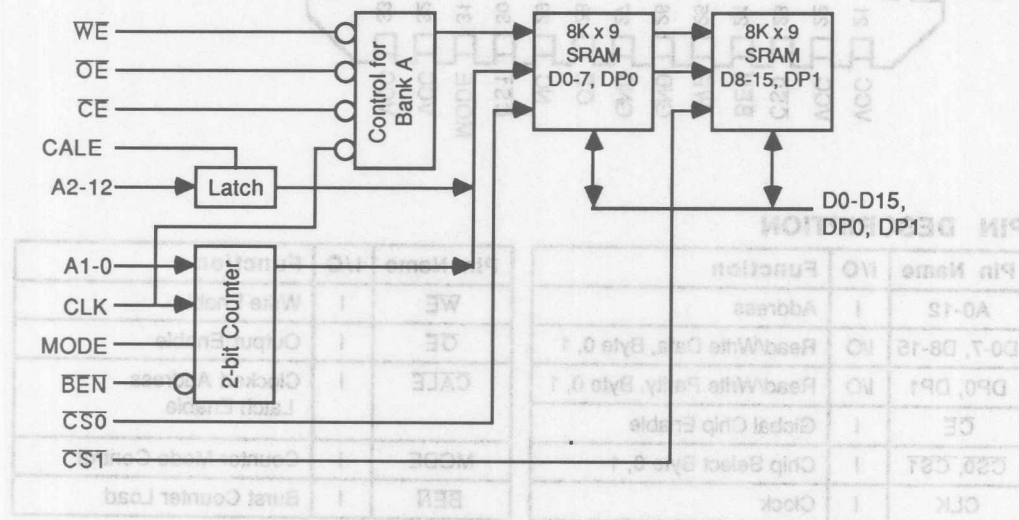
FEATURES/BENEFITS

- 8Kx18 with burst mode for secondary cache
- 1 clock initial access + 1 clock/word
- 40, 33, 25 MHz clock frequency
- Low power, high-speed QCMOS™ technology
- Selectable Binary and 486 type address counter
- Byte enables for byte/word read/write
- 6-Transistor cell for high reliability
- Available in 52-pin PLCC

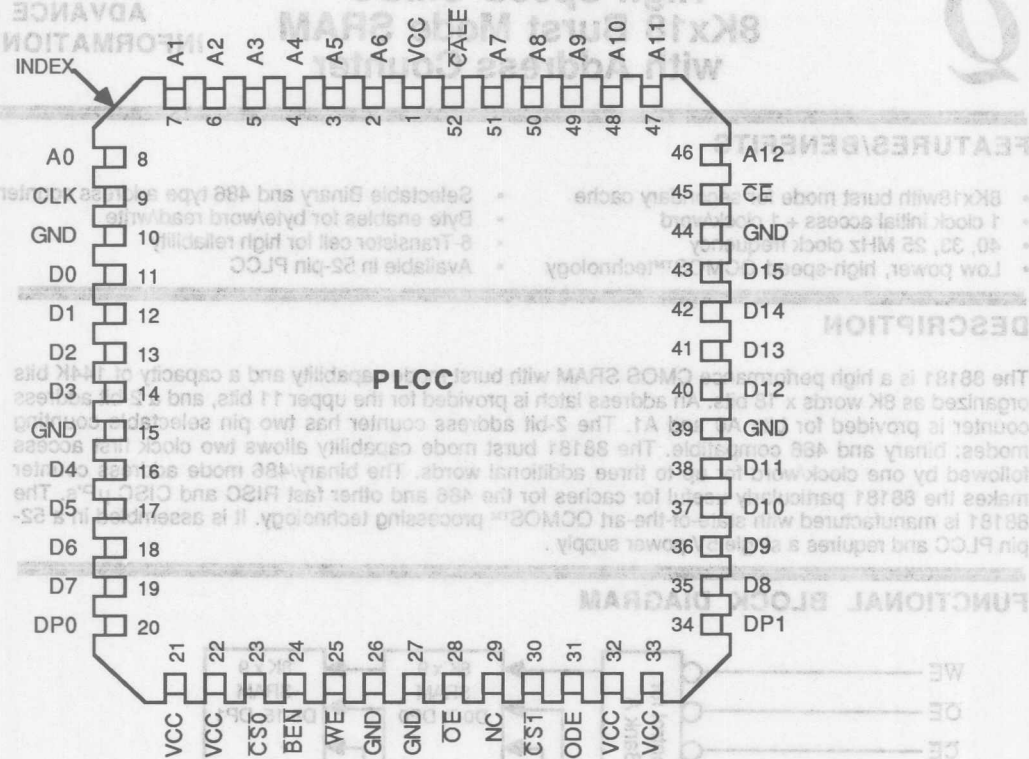
DESCRIPTION

The 88181 is a high performance CMOS SRAM with burst mode capability and a capacity of 144K bits organized as 8K words x 18 bits. An address latch is provided for the upper 11 bits, and a 2-bit address counter is provided for bits A0 and A1. The 2-bit address counter has two pin selectable counting modes: binary and 486 compatible. The 88181 burst mode capability allows two clock first access followed by one clock/word for up to three additional words. The binary/486 mode address counter makes the 88181 particularly useful for caches for the 486 and other fast RISC and CISC μ P's. The 88181 is manufactured with state-of-the-art QCMOS™ processing technology. It is assembled in a 52-pin PLCC and requires a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Name	I/O	Function
A0-12	I	Address
D0-7, D8-15	I/O	Read/Write Data, Byte 0, 1
DP0, DP1	I/O	Read/Write Parity, Byte 0, 1
CE	I	Global Chip Enable
CS0, CS1	I	Chip Select Byte 0, 1
CLK	I	Clock

Pin Name	I/O	Function
WE	I	Write Enable
OE	I	Output Enable
CALE	I	Clocked Address Latch Enable
MODE	I	Counter Mode Control
BEN	I	Burst Counter Load



High-Speed CMOS Dual 4Kx18 Cache Tag SRAM

QS88182

ADVANCE
INFORMATION

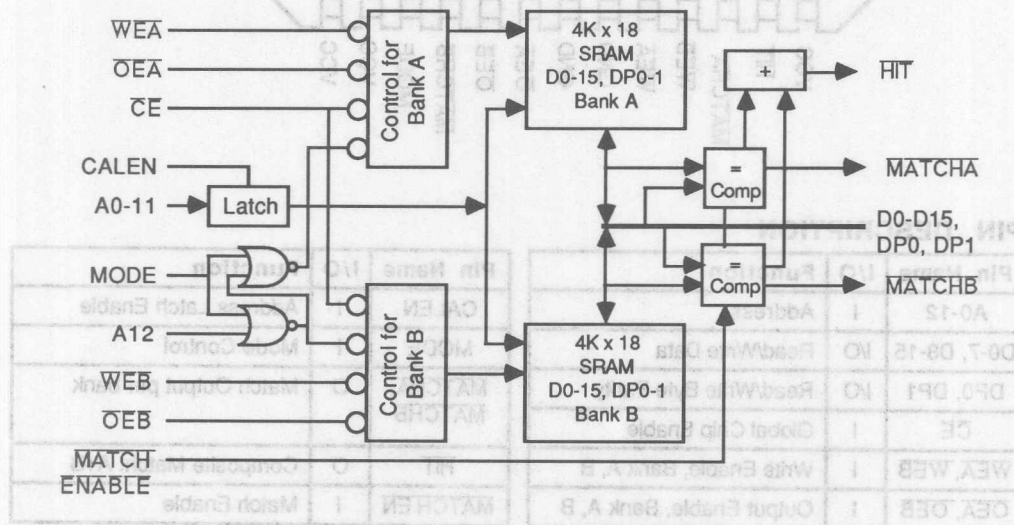
FEATURES/BENEFITS

- Dual 4Kx18 allows 2-way set associative cache tag
- MATCH lines per bank allow direct bank OE drive
- MATCH enable controls MATCH outputs for speed
- 20ns/25 ns/30 ns Taa Commercial
- 25ns/30ns Taa military
- Military product compliant to MIL-STD-883, Class B
- Independent tag comparator/bank
- Comptible with 88180 Cache Data SRAM
- HIT line provides ORed match output for control
- 6-Transistor cell for high reliability
- Low power, high-speed QCMOS™ technology
- Available in 52-pin PLCC

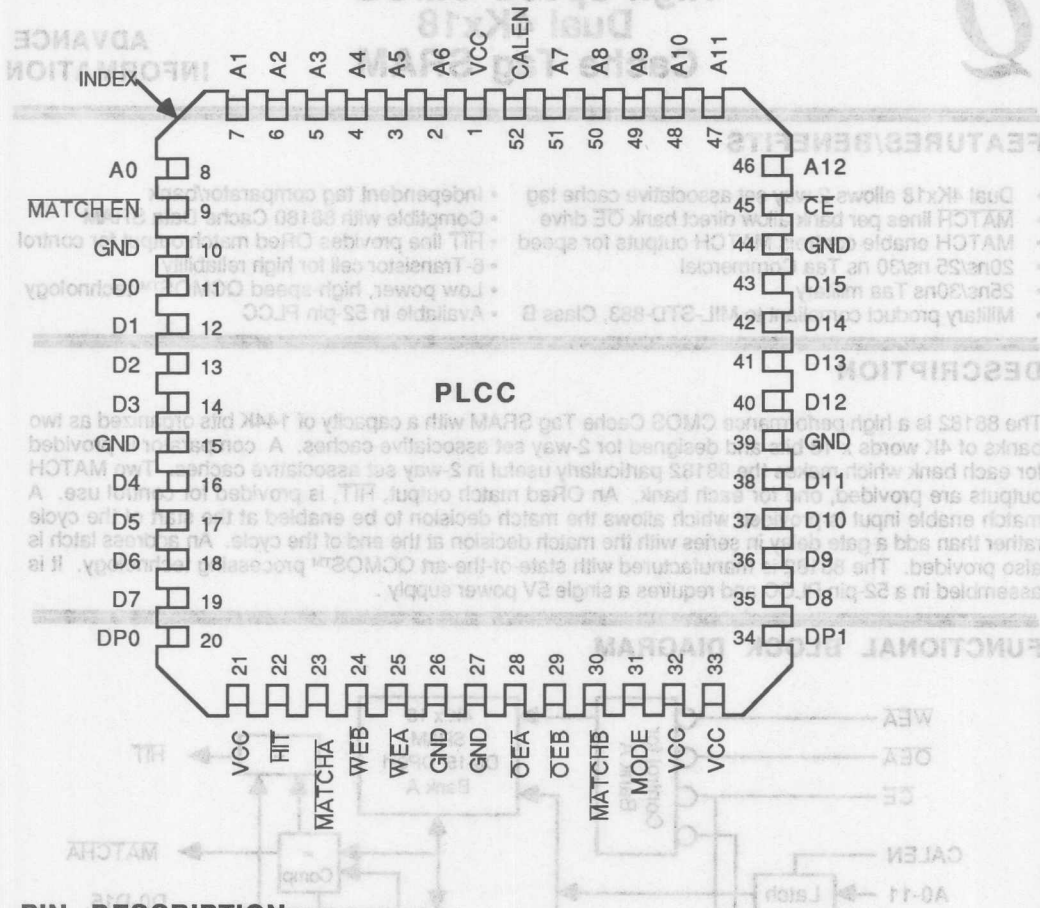
DESCRIPTION

The 88182 is a high performance CMOS Cache Tag SRAM with a capacity of 144K bits organized as two banks of 4K words x 18 bits and designed for 2-way set associative caches. A comparator is provided for each bank which makes the 88182 particularly useful in 2-way set associative caches. Two MATCH outputs are provided, one for each bank. An ORed match output, HIT, is provided for control use. A match enable input is provided which allows the match decision to be enabled at the start of the cycle rather than add a gate delay in series with the match decision at the end of the cycle. An address latch is also provided. The 88182 is manufactured with state-of-the-art QCMOS™ processing technology. It is assembled in a 52-pin PLCC and requires a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Name	I/O	Function	Pin Name	I/O	Function
A0-12	I	Address	CALEN	I	Address Latch Enable
D0-7, D8-15	I/O	Read/Write Data	MODE	I	Mode Control
DP0, DP1	I/O	Read/Write Byte Parity	MATCHA, MATCHB	O	Match Output per bank
$\overline{CE}$	I	Global Chip Enable	HIT	O	Composite Match: A+B
WEA, WEB	I	Write Enable, Bank A, B	MATCHEN	I	Match Enable
$\overline{OEA}$, $\overline{OEB}$	I	Output Enable, Bank A, B			

**QS83280
ADVANCE
INFORMATION**

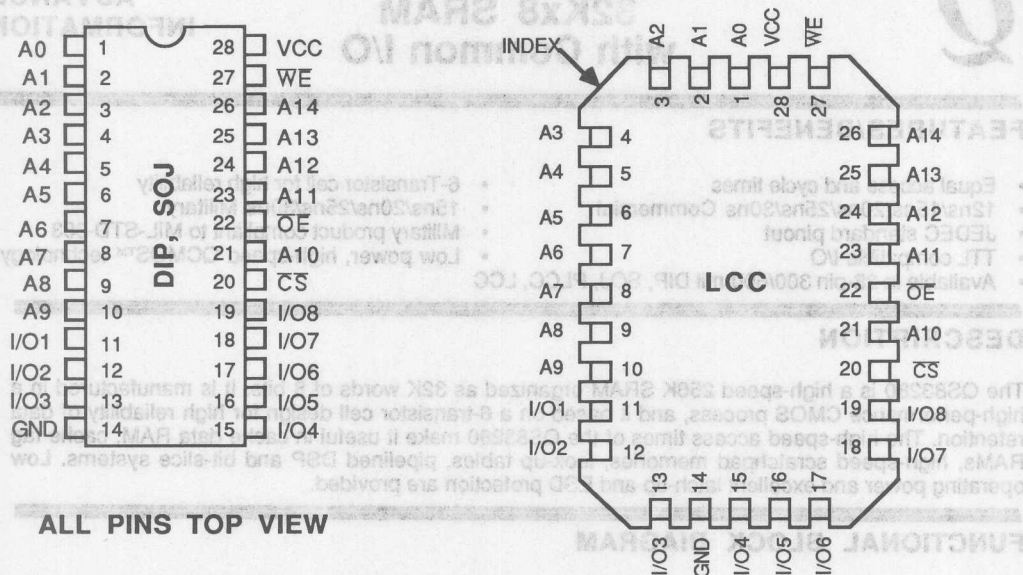
- Equal access and cycle times
- 12ns/15ns/20ns/25ns/30ns Commercial
- JEDEC standard pinout
- TTL compatible I/O
- Available in 28-pin 300/600-mil DIP, SOJ, PLCC, LCC
- 6-Transistor cell for high reliability
- 15ns/20ns/25ns/30ns Military
- Military product compliant to MIL-STD-883
- Low power, high-speed QCMOS™ technology

The QS83280 is a high-speed 256K SRAM organized as 32K words of 8 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83280 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

The diagram shows a memory array system with the following components and connections:

- Address Decoder:** Receives an **Address** input and outputs an **Address** signal to the memory array.
- 262,144 BIT MEMORY ARRAY:** The central memory component, connected to the address decoder and the Read/Write Data I/O block.
- Read/Write Data I/O:** A block that handles data transfer between the memory array and the external **I/O** bus. It is controlled by **Write** and **Read** signals.
- Control Logic:**
 - The **CS** (Chip Select) signal is connected to the **Write** signal.
 - The **WE** (Write Enable) and **OE** (Output Enable) signals are connected to the **Read** signal.
 - The **I/O** bus is connected to the **Read/Write Data I/O** block.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O8	I/O	Data
CS	I	Chip Select
WE	I	Write Enable
OE	I	Output Enable

FUNCTION TABLE

Function	CS	WE	OE	I/O	Power
Deselect	H	X	X	High Z	Standby
Read	L	H	L	Data out	Active
Write	L	L	X	Data In	Active
Output Disable	L	H	H	High Z	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Output Current Max. sink current/pin.....	50 mA
DC Output Current Max. source current/pin.....	30 mA
TBIAS Temperature Under Bias, COM.....	-65° to +125°C
TSTG Storage Temperature, COM.....	-65° to +125°C
TBIAS Temperature Under Bias, MIL.....	-65° to +135°C
TSTG Storage Temperature, MIL.....	-65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.		7	pF
Cout	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

Symbol	Parameter	-12		-15		-20		-25		-30		-35		-40		-45		-50		-55		-60		-65		-70		-75		-80		-85		-90		-95		-100		-105		-110		-115		-120		-125		-130		-135		-140		-145		-150		-155		-160		-165		-170		-175		-180		-185		-190		-195		-200		-205		-210		-215		-220		-225		-230		-235		-240		-245		-250		-255		-260		-265		-270		-275		-280		-285		-290		-295		-300		-305		-310		-315		-320		-325		-330		-335		-340		-345		-350		-355		-360		-365		-370		-375		-380		-385		-390		-395		-400		-405		-410		-415		-420		-425		-430		-435		-440		-445		-450		-455		-460		-465		-470		-475		-480		-485		-490		-495		-500		-505		-510		-515		-520		-525		-530		-535		-540		-545		-550		-555		-560		-565		-570		-575		-580		-585		-590		-595		-600		-605		-610		-615		-620		-625		-630		-635		-640		-645		-650		-655		-660		-665		-670		-675		-680		-685		-690		-695		-700		-705		-710		-715		-720		-725		-730		-735		-740		-745		-750		-755		-760		-765		-770		-775		-780		-785		-790		-795		-800		-805		-810		-815		-820		-825		-830		-835		-840		-845		-850		-855		-860		-865		-870		-875		-880		-885		-890		-895		-900		-905		-910		-915		-920		-925		-930		-935		-940		-945		-950		-955		-960		-965		-970		-975		-980		-985		-990		-995		-1000		-1005		-1010		-1015		-1020		-1025		-1030		-1035		-1040		-1045		-1050		-1055		-1060		-1065		-1070		-1075		-1080		-1085		-1090		-1095		-1100		-1105		-1110		-1115		-1120		-1125		-1130		-1135		-1140		-1145		-1150		-1155		-1160		-1165		-1170		-1175		-1180		-1185		-1190		-1195		-1200		-1205		-1210		-1215		-1220		-1225		-1230		-1235		-1240		-1245		-1250		-1255		-1260		-1265		-1270		-1275		-1280		-1285		-1290		-1295		-1300		-1305		-1310		-1315		-1320		-1325		-1330		-1335		-1340		-1345		-1350		-1355		-1360		-1365		-1370		-1375		-1380		-1385		-1390		-1395		-1400		-1405		-1410		-1415		-1420		-1425		-1430		-1435		-1440		-1445		-1450		-1455		-1460		-1465		-1470		-1475		-1480		-1485		-1490		-1495		-1500		-1505		-1510		-1515		-1520		-1525		-1530		-1535		-1540		-1545		-1550		-1555		-1560		-1565		-1570		-1575		-1580		-1585		-1590		-1595		-1600		-1605		-1610		-1615		-1620		-1625		-1630		-1635		-1640		-1645		-1650		-1655		-1660		-1665		-1670		-1675		-1680		-1685		-1690		-1695		-1700		-1705		-1710		-1715		-1720		-1725		-1730		-1735		-1740		-1745		-1750		-1755		-1760		-1765		-1770		-1775		-1780		-1785		-1790		-1795		-1800		-1805		-1810		-1815		-1820		-1825		-1830		-1835		-1840		-1845		-1850		-1855		-1860		-1865		-1870		-1875		-1880		-1885		-1890		-1895		-1900		-1905		-1910		-1915		-1920		-1925		-1930		-1935		-1940		-1945		-1950		-1955		-1960		-1965		-1970		-1975		-1980		-1985		-1990		-1995		-2000		-2005		-2010		-2015		-2020		-2025		-2030		-2035		-2040		-2045		-2050		-2055		-2060		-2065		-2070		-2075		-2080		-2085		-2090		-2095		-2100		-2105		-2110		-2115		-2120		-2125		-2130		-2135		-2140		-2145		-2150		-2155		-2160		-2165		-2170		-2175		-2180		-2185		-2190		-2195		-2200		-2205		-2210		-2215		-2220		-2225		-2230		-2235		-2240		-2245		-2250		-2255		-2260		-2265		-2270		-2275		-2280		-2285		-2290		-2295		-2300		-2305		-2310		-2315		-2320		-2325		-2330		-2335		-2340		-2345		-2350		-2355		-2360		-2365		-2370		-2375		-2380		-2385		-2390		-2395		-2400		-2405		-2410		-2415		-2420		-2425		-2430		-2435		-2440		-2445		-2450		-2455		-2460		-2465		-2470		-2475		-2480		-2485		-2490		-2495		-2500		-2505		-2510		-2515		-2520		-2525		-2530		-2535		-2540		-2545		-2550		-2555		-2560		-2565		-2570		-2575		-2580		-2585		-2590		-2595		-2600		-2605		-2610		-2615		-2620		-2625		-2630		-2635		-2640		-2645		-2650		-2655		-2660		-2665		-2670		-2675		-2680		-2685		-2690		-2695		-2700		-2705		-2710		-2715		-2720		-2725		-2730		-2735		-2740		-2745		-2750		-2755		-2760		-2765		-2770		-2775		-2780		-2785		-2790		-2795		-2800		-2805		-2810		-2815		-2820		-2825		-2830		-2835		-2840		-2845		-2850		-2855		-2860		-2865		-2870		-2875		-2880		-2885		-2890		-2895		-2900		-2905		-2910		-2915		-2920		-2925		-2930		-2935		-2940		-2945		-2950		-2955		-2960		-2965		-2970		-2975		-2980		-2985		-2990		-2995		-3000		-3005		-3010		-3015		-3020		-3025		-3030		-3035		-3040		-3045		-3050		-3055		-3060		-3065		-3070		-3075		-3080		-3085		-3090		-3095		-3100		-3105		-3110		-3115		-3120		-3125		-3130		-3135		-3140		-3145		-3150		-3155		-3160		-3165		-3170		-3175		-3180		-3185		-3190		-3195		-3200		-3205		-3210		-3215		-3220		-3225		-3230		-3235		-3240		-3245		-3250		-3255		-3260		-3265		-3270		-3275		-3280		-3285		-3290		-3295		-3300		-3305		-3310		-3315		-3320		-3325		-3330		-3335		-3340		-3345		-3350		-3355		-3360		-3365		-3370		-3375		-3380		-3385		-3390		-3395		-3400		-3405		-3410		-3415		-3420		-3425		-3430		-3435		-3440		-3445		-3450		-3455		-3460		-3465		-3470		-3475		-3480		-3485		-3490		-3495		-3500		-3505		-3510		-3515		-3520		-3525		-3530		-3535		-3540		-3545		-3550		-3555		-3560		-3565		-3570		-3575		-3580		-3585		-3590		-3595		-3600		-3605		-3610		-3615		-3620		-3625		-3630		-3635		-3640		-3645		-3650		-3655		-3660		-3665		-3670		-3675		-3680		-3685		-3690		-3695		-3700		-3705		-3710		-3715		-3720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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc Chip deselected		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1/t RC

Symbol	Parameter	-12		-15		-20		-25/-30		Unit
		C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	180	190	170	180	160	170	150	160	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	90	100	90	100	90	100	90	100	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	12ns(3)		15ns(3)		20ns		25ns		30ns	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE											
t RC	Read Cycle Time	12	-	15	-	20	-	25	-	30	-
t AA	Address Access Time	-	12	-	15	-	20	-	25	-	30
t ACS	Chip Select Access Time	-	12	-	15	-	20	-	25	-	30
t OH	Output Hold from Address Change	2	-	2	-	2	-	2	-	2	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	2	-
tCHZ	Chip Select to Output in High Z (2)	-	6	-	7	-	8	-	10	-	12
tOE	Output Enable Access Time	-	7	-	8	-	10	-	12	-	15
tOHZ	Output enable to output in High Z (2)	-	6	-	7	-	8	-	10	-	12
tOLZ	Output enable to output in Low Z (2)	0	-	0	-	0	-	0	-	0	-
tPU	Chip select to Power-Up time(2)	0	-	0	-	0	-	0	-	0	-
tPD	Chip select to Power-Down time	-	12	-	15	-	20	-	25	-	30

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

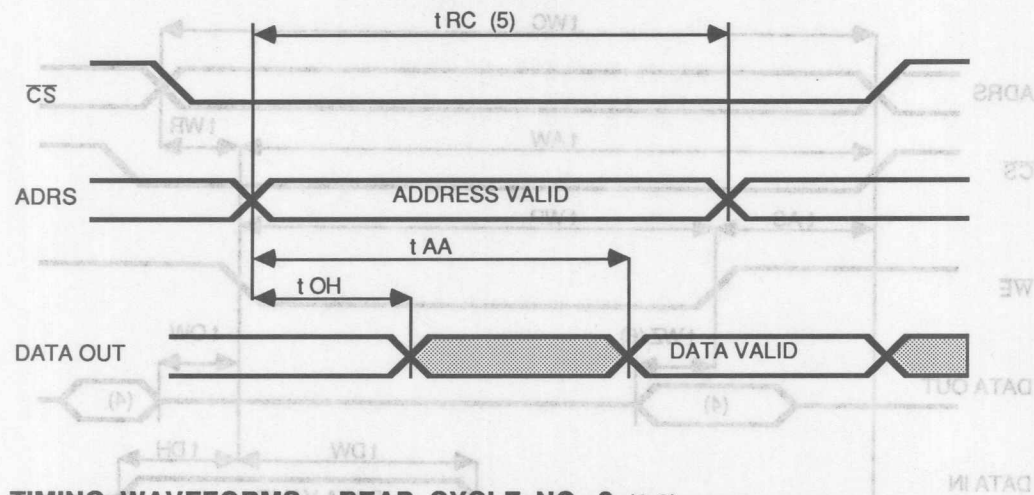
Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12ns (3)		-15ns(3)		-20ns		-25ns		-30ns	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	12	-	15	-	20	-	25	-	30	-
t CW	Chip Select Valid to End of Write	10	-	13	-	17	-	20	-	25	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	10	-	12	-	16	-	20	-	25	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	7	-	8	-	10	-	15	-	20	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	6	-	7	-	8	-	10	-	12
t OW	Output Active from End of Write (2)	0	-	0	-	0	-	0	-	0	-
t AW	Address Valid to End of Write	10	-	13	-	17	-	20	-	25	-

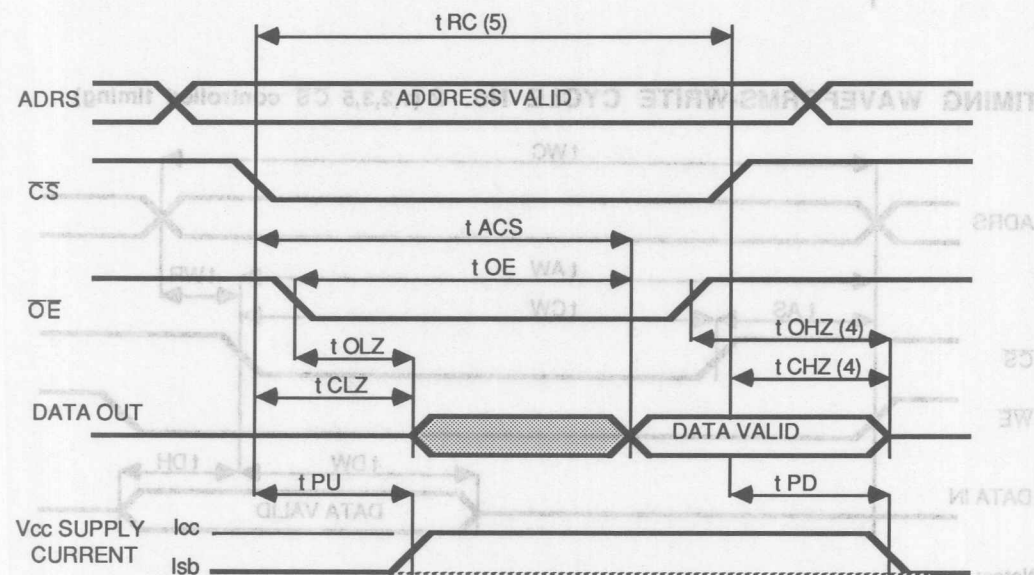
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,3)



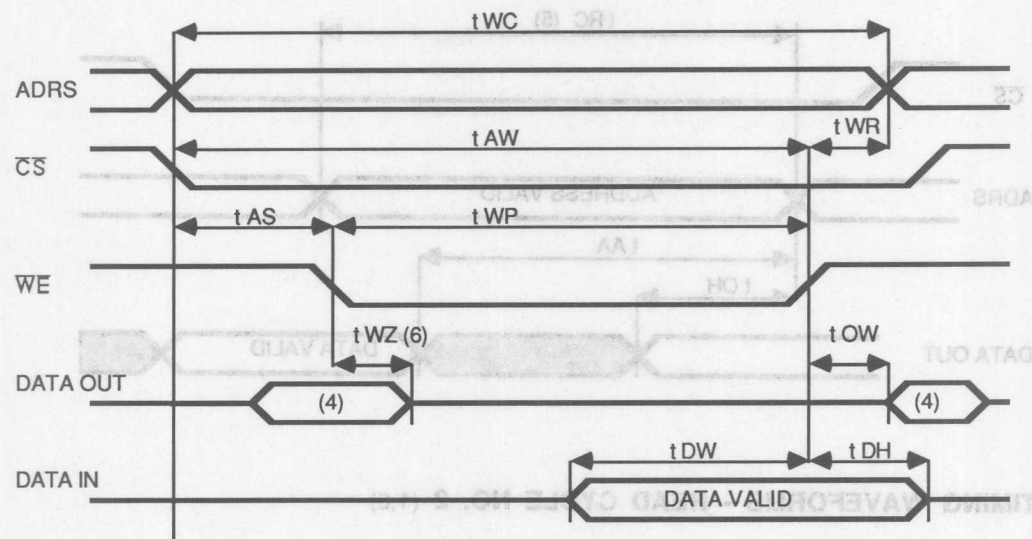
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



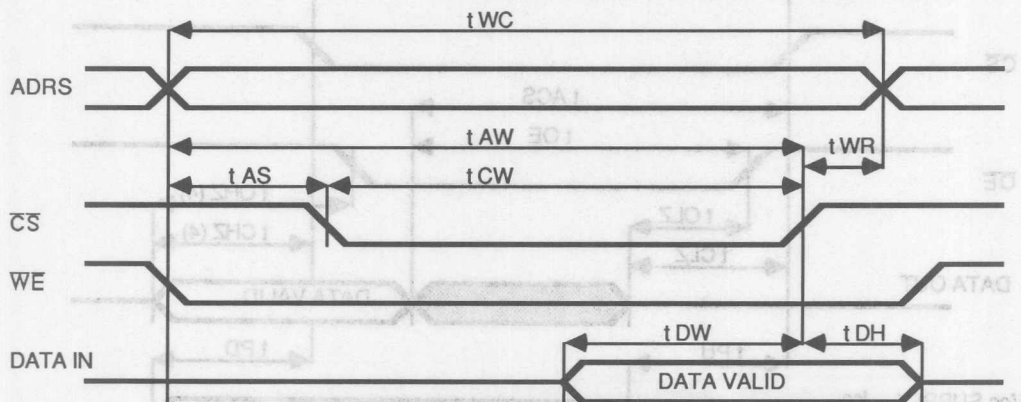
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. t_{WR} is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 32Kx8 SRAM with Fast Address Bit

**QS83283
ADVANCE
INFORMATION**

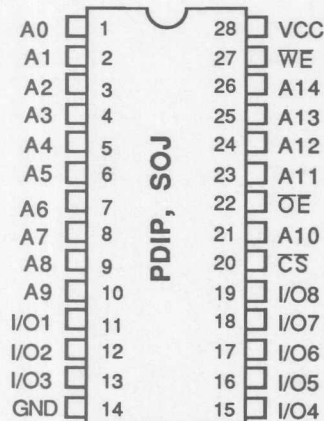
FEATURES/BENEFITS

- Equal access and cycle times
- 15ns/20ns/25/30 ns Commercial
- 20ns/25/30 ns Military
- Available in 28-pin 300/600-mil DIP, SOJ
- Military product compliant to MIL-STD-883
- Fast access on one address bit for MIPS R4000
- 6-Transistor cell for high reliability
- TTL compatible I/O
- High performance QCMOS™ technology

DESCRIPTION

The QS83283 is a high-speed 256K SRAM organized as 32K words of 8 bits. It has a fast access address pin (A10) which allows access to a second word in approximately half the access time for the first word. This is useful in MIPS R4000 RISC CPU secondary cache applications. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83283 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATION



ALL PINS TOP VIEW

Q883283
ADVANCE
INFORMATION

High-Speed CMOS 32Kx8 SRAM with Fast Address Bit



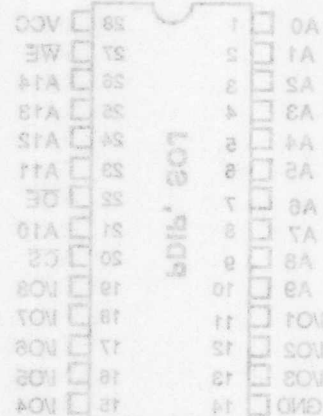
FEATURES/BENEFITS

- Equal access and cycle times
- 15ns/20ns/25ns as Commercial
- 20ns/25ns as Military
- Available in 28-pin 300µm-mil DIP, SOJ
- Military product compliant to MIL-STD-883
- High performance CMOS technology
- TTL compatible I/O
- 8-Transistor cell for high reliability
- Fast access on one address bit for MIPS R4000

DESCRIPTION

The Q883283 is a high-speed 32K SRAM organized as 32K words of 8 bits. It has a fast access address pin (A10) which allows access to a second word in approximately half the access time for the first word. This is useful in MIPS R4000 RISC CPU secondary cache applications. It is manufactured in a high-performance CMOS process, and is based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the Q883283 make it useful in cache data RAM, cache tag RAM, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATION



ALL PINS TOP VIEW



Low Power CMOS 32Kx8 SRAM with Common I/O

QS83285
PRELIMINARY

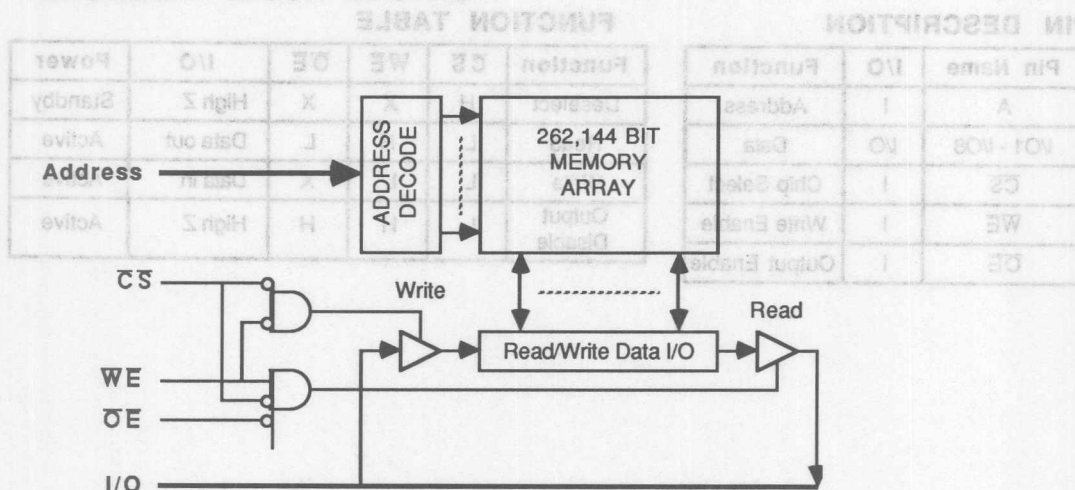
FEATURES/BENEFITS

- Ultra low stby. power for battery backup applications
- 70ns/85ns/100ns/120ns Commercial
- 85ns/100ns/120ns Military
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- TTL compatible I/O
- JEDEC standard pinout
- Available in 28-pin 300/600-mil PDIP

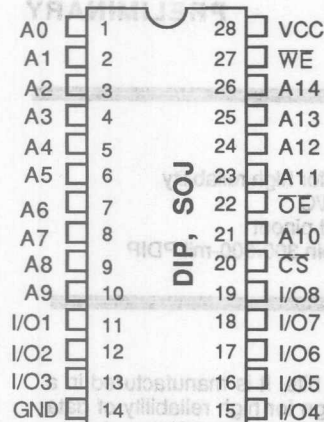
DESCRIPTION

The QS83285 is a high-speed 256K SRAM organized as 32K words of 8 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83285 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



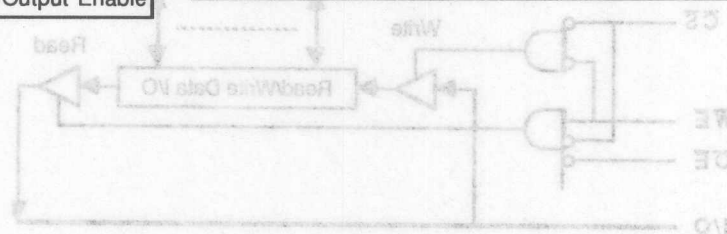
ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O8	I/O	Data
CS	I	Chip Select
WE	I	Write Enable
OE	I	Output Enable

FUNCTION TABLE

Function	CS	WE	OE	I/O	Power
Deselect	H	X	X	High Z	Standby
Read	L	H	L	Data out	Active
Write	L	L	X	Data In	Active
Output Disable	L	H	H	High Z	Active



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Output Current Max. sink current/pin.....	50 mA
DC Output Current Max. source current/pin.....	30 mA
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C
T_{STG} Storage Temperature, COM.....	-65° to +125°C
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C
T_{STG} Storage Temperature, MIL.....	-65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.	7	7	pF
Cout	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.	7	7	pF

Note: Capacitance is measured at characterization but not tested at final production.

Icc1	mA	80	55	Operating Current, $C_S = V_I, V_E = V_{IH}$, Other inputs = V_{IH}/V_{IL} $V_{CC} = \text{MAX}$ Outputs open $t = \text{max. } 700\text{ns}$
				Standby Current, $V_{CC} = 5.0\text{V}$ $C_S \geq V_{CC} - 0.2\text{V}$ $V_{in} \leq 0.2\text{V}$ or $V_{in} \leq V_{CC} - 0.2\text{V}$
Icc2	mA	50	45	Operating Current, $C_S = V_I, V_E = V_{IH}$, Other inputs = V_{IH}/V_{IL} $V_{CC} = \text{MAX}$ Outputs open $t = \text{max. } 100\text{--}150$ ns
				Standby Current, $V_{CC} = 5.0\text{V}$ $C_S \geq V_{CC} - 0.2\text{V}$ $V_{in} \leq 0.2\text{V}$ or $V_{in} \leq V_{CC} - 0.2\text{V}$
Icc3	mA	4.0	3.0	Operating Current, $C_S = V_I, V_E = V_{IH}$, Other inputs = V_{IH}/V_{IL} $V_{CC} = \text{MAX}$ Outputs open $t = \text{max. } 100\text{--}150$ ns
				Standby Current, $V_{CC} = 5.0\text{V}$ $C_S \geq V_{CC} - 0.2\text{V}$ $V_{in} \leq 0.2\text{V}$ or $V_{in} \leq V_{CC} - 0.2\text{V}$

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -1 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 2.1 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		2		4	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc Chip deselected		2		4	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	Max COM.	Max MIL.	Unit	Symbol	Parameter	Max COM.	Max MIL.	Unit
Icc1	Operating Current, CS = Vil, WE = Vih, Other inputs = Vih/Vil Vcc = MAX Outputs open f = max, 70/85ns	55	60	mA	Ib2	Standby Current, Vcc = 2.0-5.5V CS ≥ Vcc-0.2V Vin ≤ 0.2V or Vin ≥ Vcc -0.2V	1.0	5.0	uA
Icc2	Operating Current, CS = Vil, WE = Vih, Other inputs = Vih/Vil Vcc = MAX Outputs open f = max, 100-150 ns	45	50		Ib3	Standby Current, Vcc = 2.0V CS ≥ Vcc-0.2V Vin ≤ 0.2V or Vin ≥ Vcc -0.2V	0.5	3.0	
Ib1	Standby Current, Vcc = MAX Outputs open CS ≥ Vih	3.0	4.0						

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	70ns		85ns		100ns		120ns	
		Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE									
t RC	Read Cycle Time	70	-	85	-	100	-	120	-
t AA	Address Access Time	-	70	-	85	-	100	-	120
t ACS	Chip Select Access Time	-	70	-	85	-	100	-	120
t OH	Output Hold from Address	5	-	5	-	5	-	5	-
t CLZ	Chip Select to Output in Low Z (2)	10	-	10	-	10	-	10	-
t CHZ	Chip Select to Output in High Z (2)	-	30	-	30	-	35	-	40
t OE	Output Enable Access Time	-	35	-	45	-	50	-	60
t OHZ	Output enable to output in High Z	-	30	-	30	-	35	-	40
t OLZ	Output enable to output in Low Z	5	-	5	-	5	-	5	-
t PU	Chip select to Power-Up Time (2)	0	-	0	-	0	-	0	-
t PD	Chip select to Power-Down Time	-	70	-	85	-	100	-	120

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QS83285

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

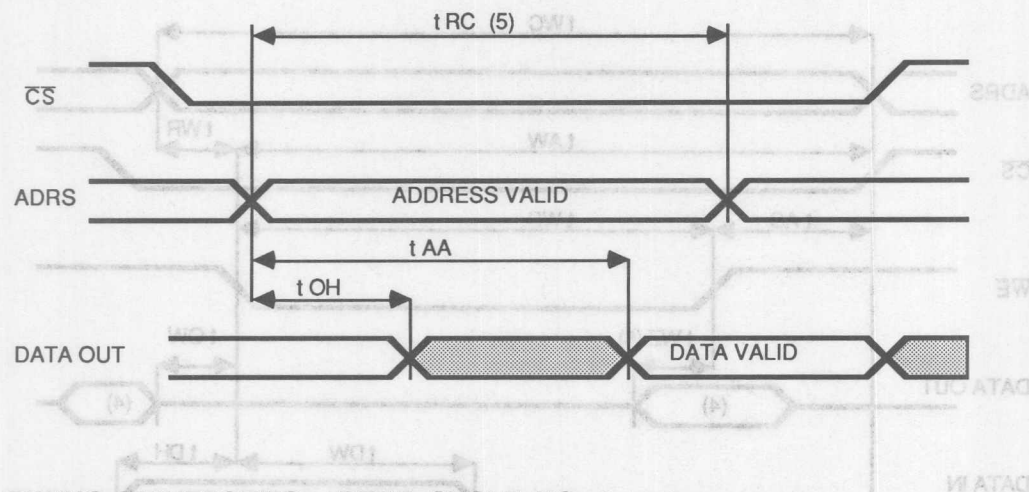
Symbol	Parameter (1)	70ns		85ns		100ns		120ns	
		Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE									
tWC	Write Cycle Time	70		85		100			120
tCW	Chip Select Valid to End of Write	65		75		90		100	
tAS	Address Setup Time	0		0		0		0	
tWP	Write Pulse width	55		65		70		80	
tWR	Write Recovery Time	0		0		0		0	
tDW	Data Valid to End of Write	35		40		45		50	
tDH	Data Hold Time	0		0		0		0	
tWZ	Write Enable to Output in High Z (2)	-	30	-	30	-	35	-	40
tOW	Output Active from End of Write (2)	5		5		5		5	
tAW	Address Valid to End of Write	65		75		90		100	

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.

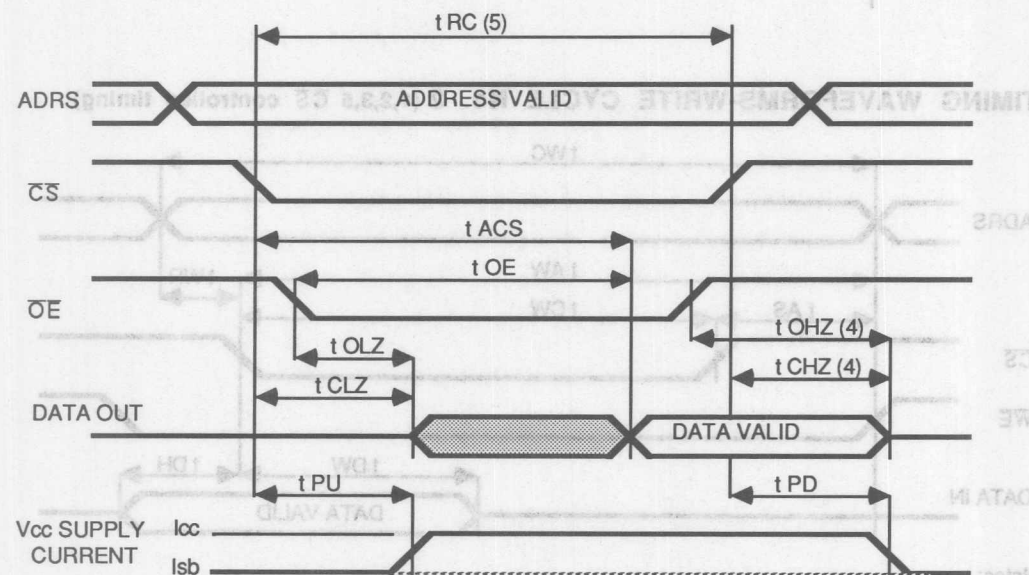
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,3)



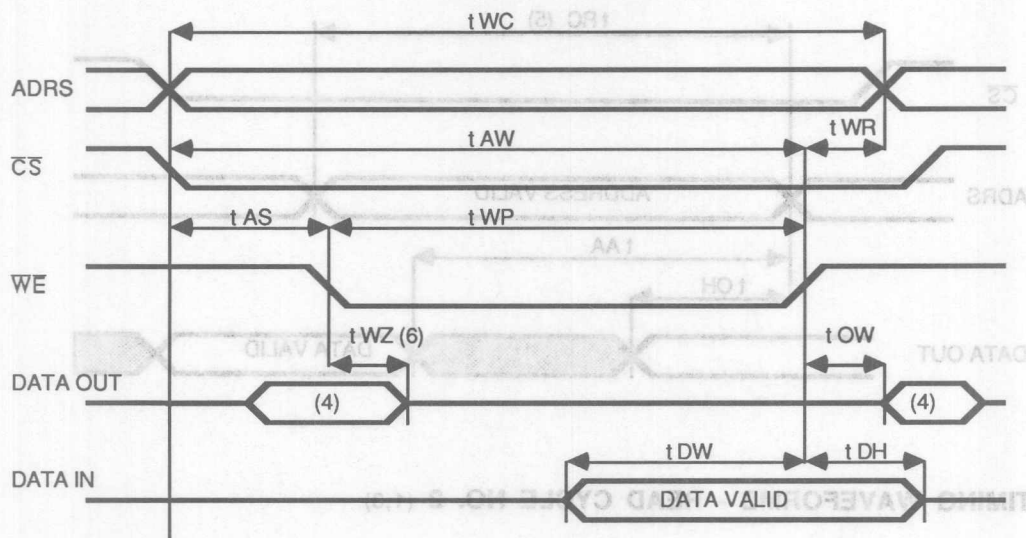
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



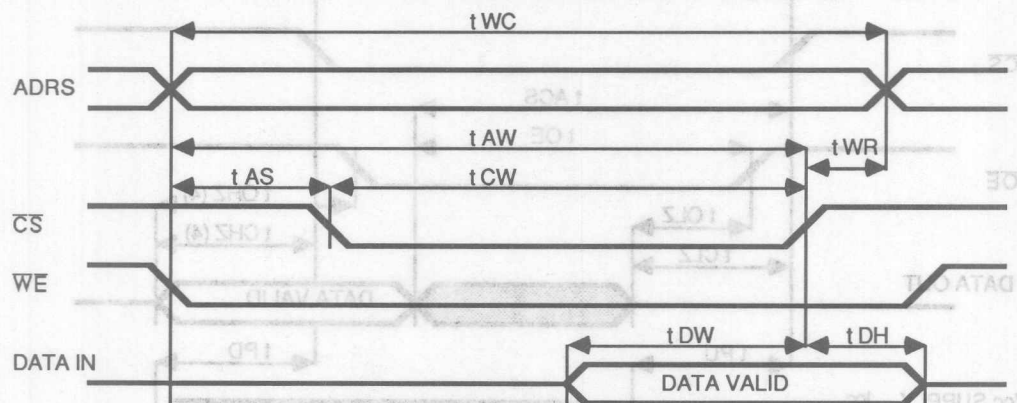
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 32Kx8 SRAM with Fast Chip Select

**QS83289
ADVANCE
INFORMATION**

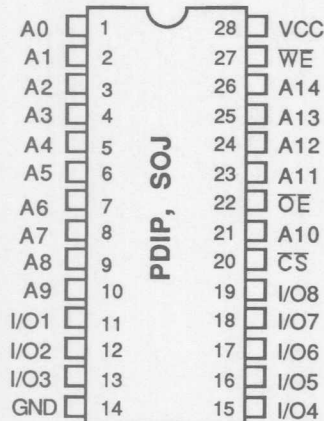
FEATURES/BENEFITS

- Equal access and cycle times
- 12ns/15ns/20ns/25/30ns Commercial
- 15ns/20ns/25/30ns Military
- Available in 28-pin 300/600-mil DIP, SOJ
- Military product compliant to MIL-STD-883
- Fast chip select access
- 6-Transistor cell for high reliability
- TTL compatible I/O
- High performance QCMOS™ technology

DESCRIPTION

The QS83289 is a high-speed 256K SRAM organized as 32K words of 8 bits. It achieves a fast chip select access time by not powering down the array when the chip is disabled. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83289 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATION



ALL PINS TOP VIEW

Q883289
ADVANCE
INFORMATION

High-Speed CMOS 32Kx8 SRAM with Fast Chip Select



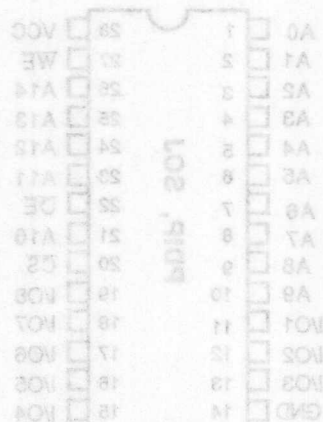
FEATURES/BENEFITS

- Equal access and cycle times
- 12ns/5ns/20ns/25/30ns Commercial
- 18ns/20ns/25/30ns Military
- Available in 28-pin 300µm DIP, SOJ
- Military product compliant to MIL-STD-883C
- Fast chip select access
- 8-Transistor cell for high reliability
- TTL compatible I/O
- High performance CMOS technology

DESCRIPTION

The Q883289 is a high-speed 32K SRAM organized as 32K words of 8 bits. It achieves a fast chip select access time by not powering down the array when the chip is disabled. It is manufactured in a high-performance CMOS process, and is based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the Q883289 make it useful in cache data RAM, cache tag RAM, high-speed secreted memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATION





High Speed CMOS 32Kx9 SRAM with Common I/O

QS83290
ADVANCE
INFORMATION

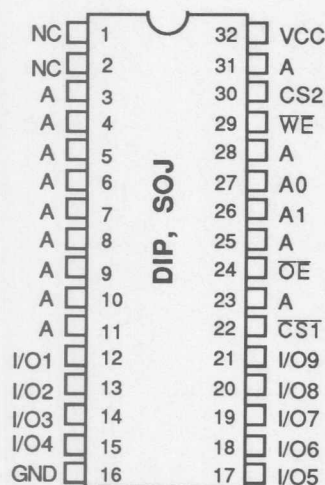
FEATURES/BENEFITS

- 15/20/25/30ns Commercial
- 20/25/30ns Military
- TTL compatible I/O
- Available in 32-pin 300/600-mil DIP, SOJ
- Equal access and cycle times
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- JEDEC standard pinout

DESCRIPTION

The QS83290 is a high-speed 288K SRAM organized as 32K words of 9 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83290 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

High Speed CMOS
32Kx8 SRAM
With Common I/O

High Speed CMOS
32Kx8 SRAM
With Common I/O



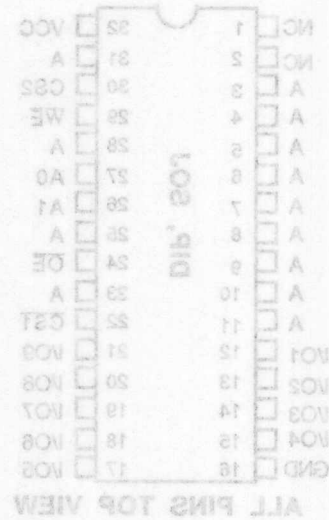
FEATURES/BENEFITS

- Available in 32-pin 300/600-mil DIP, SOJ
- TTL compatible I/O
- 30V/30ns Military
- 15V/25/30ns Commercial
- JEDEC standard pinout
- 8-Transistor cell for high reliability
- Military product compliant to MIL-STD-883
- Equal access and cycle times

DESCRIPTION

The QS83290 is a high-speed 32K SRAM organized as 32K words of 8 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS83290 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS





High Speed CMOS 32Kx9 SRAM with Burst Mode

**QS83291
ADVANCE
INFORMATION**

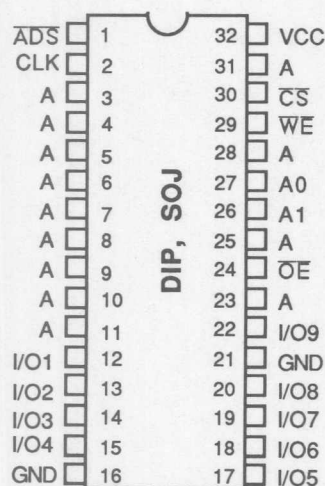
FEATURES/BENEFITS

- 32Kx9 Burst Mode SRAM
- 20/25/30/40ns Commercial
- 25/30/40ns Military
- TTL compatible I/O
- Available in 32-pin 300/600-mil DIP, SOJ
- Optimized for 80486 secondary cache
- 20 ns clock cycle time for 50 MHz systems
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- JEDEC standard pinout

DESCRIPTION

The QS83291 is a high-speed 288K SRAM with burst mode operation organized as 32K words of 9 bits. It is a clocked device with a 80486 CPU compatible 4-word burst counter and is optimized for performance in 80486 secondary cache systems. Clock cycle times down to 20 ns allow use in 50 MHz systems. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

High Speed CMOS
32Kx9 SRAM
with Burst Mode

High Speed CMOS
32Kx9 SRAM
with Burst Mode



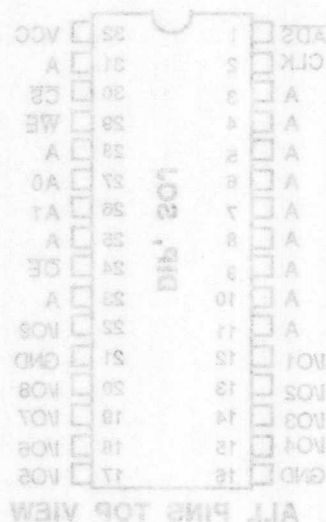
FEATURES/BENEFITS

- 32Kx9 Burst Mode SRAM
- 20/25/30/40ns Commercial
- 25/30/40ns Military
- TTL compatible I/O
- Available in 32-pin 300/600-mil DIP, SOJ
- Optimized for 80486 secondary cache
- 50 ns clock cycle time for 50 MHz systems
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- JEDEC standard pinout

DESCRIPTION

The QS83291 is a high-speed 32K SRAM with burst mode operation organized as 32K words of 9 bits. It is a clocked device with a 80486 CPU compatible 4-word burst counter and is optimized for performance in 80486 secondary cache systems. Clock cycle times down to 50 ns allow use in 50 MHz systems. It is manufactured in a high-performance CMOS process, and is based on a 6-transistor cell design for high reliability of data retention. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS





High-Speed CMOS 64Kx4 SRAM with Common I/O

QS86440
ADVANCE
INFORMATION

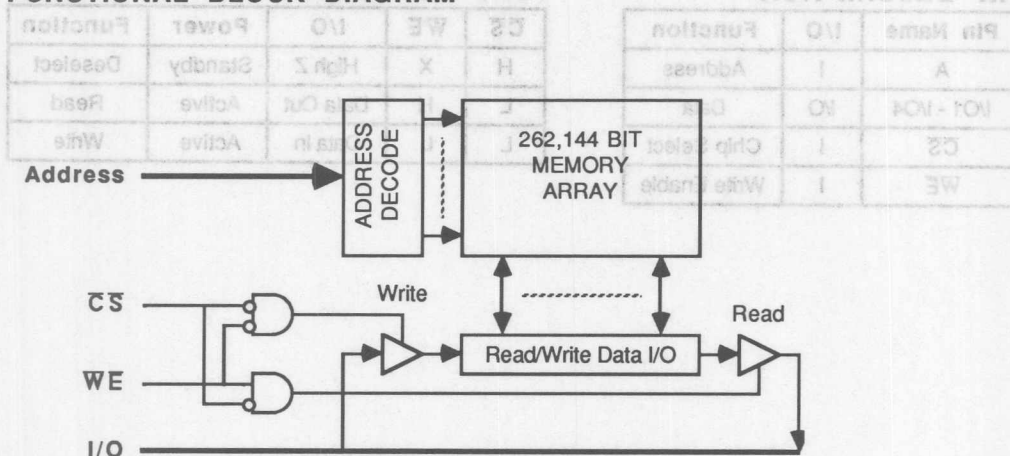
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 24-pin DIP, 24-pin ZIP, 24-pin 300 mil SOJ & 28-pin LCC
- Low Standby current
- JEDEC standard pinout

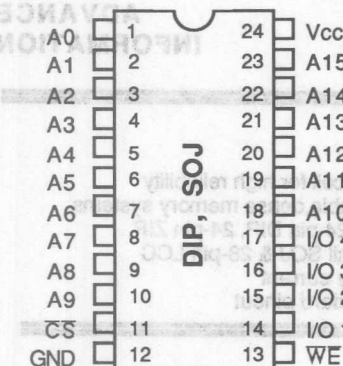
DESCRIPTION

The QS86440 is a high-speed 256K SRAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS86440 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW

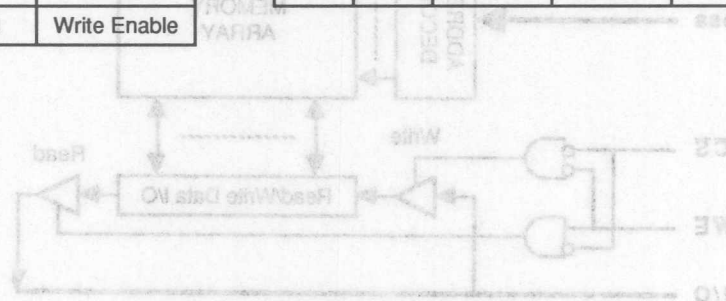
* For ZIP, LCC pinouts contact factory

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O4	I/O	Data
CS	I	Chip Select
WE	I	Write Enable

FUNCTION TABLE

CS	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$		
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA		
DC Output Current Max. source current/pin.....	30 mA		
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C		
T_{STG} Storage Temperature, COM.....	-65° to +125°C		
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

Symbol	Parameter	C	M	C	M	C	M	C	M	C	M
10c1	Static Operating Current, $V_{CC} = \text{MAX}$ Outputs open $C_S \leq V_{IL}, I = 0$	100	150	100	150	100	150	100	150	100	150
10c2	Dynamic Operating Current, $V_{CC} = \text{MAX}$ Outputs open $C_S \leq V_{IL}, I = \text{MAX}$	170	-	185	175	155	165	145	155		
10b	TTL Standby Current, $V_{CC} = \text{MAX}$ Outputs open $C_S \geq V_{IL}, I = \text{MAX}$	90	100	80	100	90	100	90	100		
10d1	Full Standby Current, $V_{CC} = \text{MAX}$ Outputs open $C_S \leq V_{IL}, I = 0$ $V_{IL} \leq V_{IC}$ or $V_{IL} \geq V_{IC}$	15	20	15	20	15	20	15	20		

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	170	-	165	175	155	165	145	155	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	90	100	90	100	90	100	90	100	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15(3)		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE											
t RC	Read Cycle Time	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	2	-	2	-	3	-	3	-	3	-
t LZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	3	-
t HZ	Chip Select to Output in High Z (2)	-	5	-	7	-	8	-	10	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	-	12	-	15	-	19	-	25	-	35

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS86440

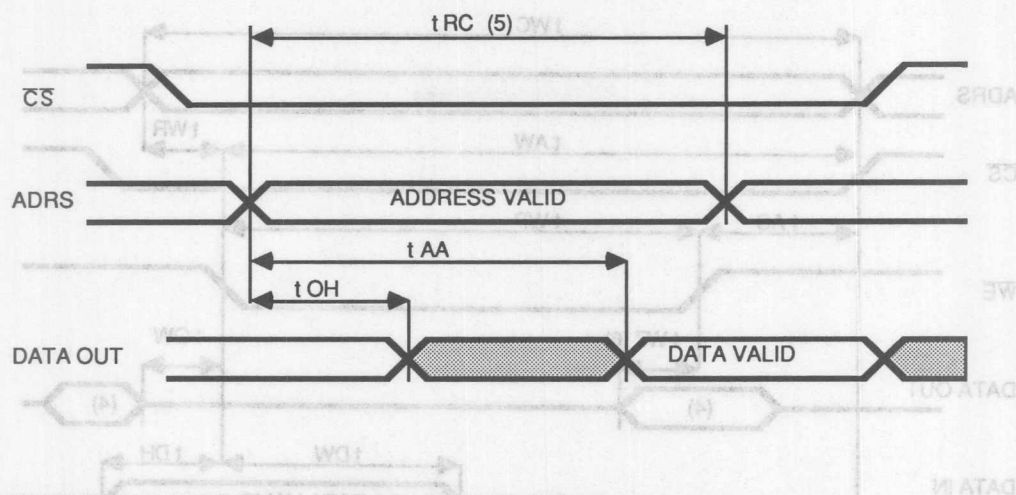
Commercial TA = 0°C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15(3)		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	6	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write(2)	2	-	2	-	2	-	2	-	3	-

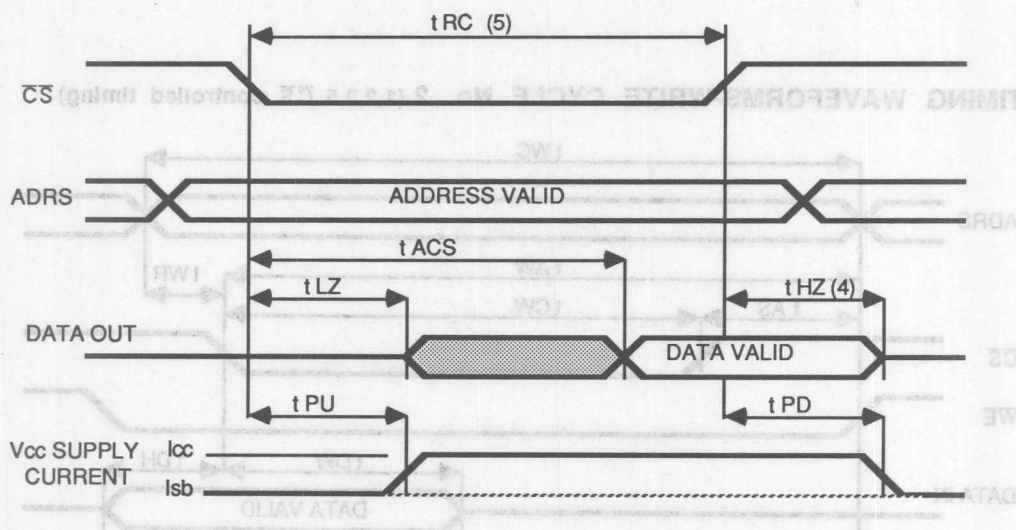
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



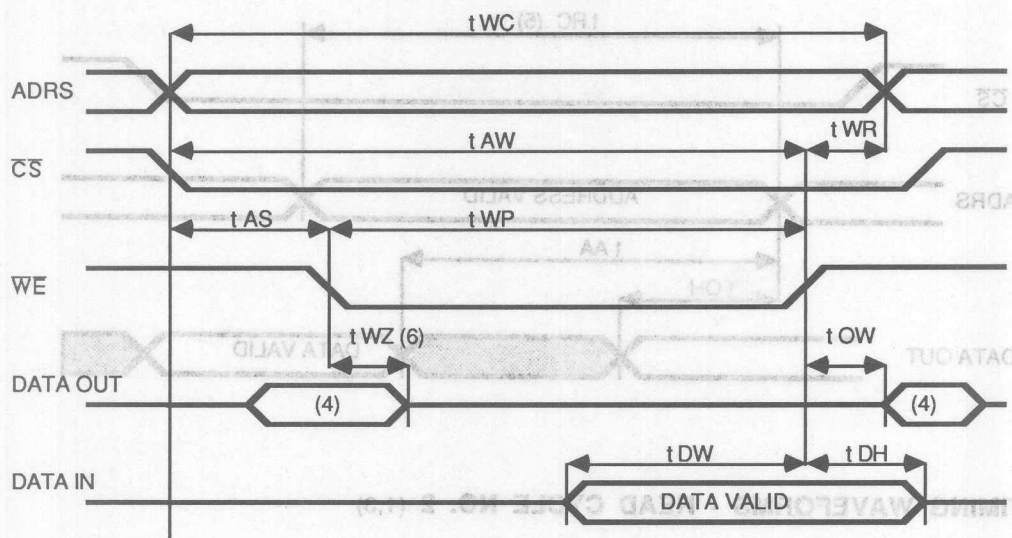
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



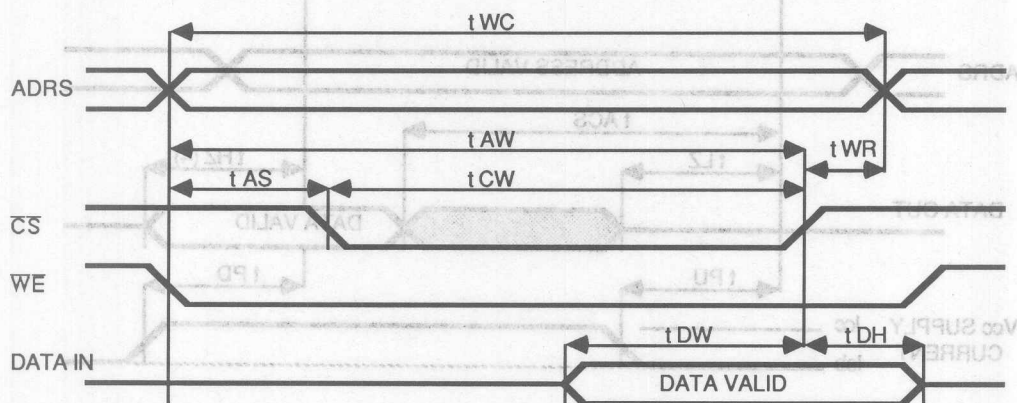
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or CS must be high during address transitions.
2. A write occurs during the overlap of a low CS and a low WE.
3. tWR is measured from the earlier of CS and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 64Kx4 Cache TAG RAM

QS86442
ADVANCE
INFORMATION

FEATURES/BENEFITS

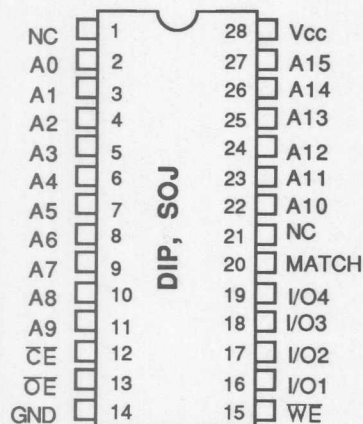
- Fast Match and Access times
- Access time of 15ns/20ns/25ns/35ns Commercial
- Match time of 15ns/20ns/25ns/35ns Commercial
- Low power, high-speed QCMOS™ technology
- 6-Transistor cell for high reliability
- MATCH signal with positive polarity
- Available in 300-mil, 28-pin DIP and SOJ
- Military product compliant to MIL-STD-883

DESCRIPTION

The QS86442 is a high-speed 256K TAG RAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. Low operating power and excellent latch-up and ESD protection are provided.

2

PIN CONFIGURATIONS



ALL PINS TOP VIEW

QS86442
ADVANCE
INFORMATION

High-Speed CMOS 64Kx4 Cache TAG RAM



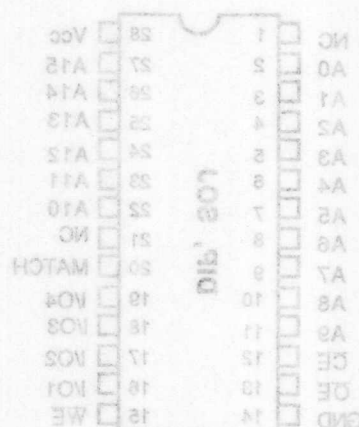
FEATURES/BENEFITS

- Fast Match and Access times
- Access time of 25ns/30ns/35ns Commercial
- Match time of 25ns/30ns/35ns Commercial
- Low power, high-speed CMOS[®] technology
- Military product compliant to MIL-STD-883C
- Available in 300-mil, 28-pin DIP and SOJ
- MATCH signal with positive polarity
- 8-Transistor cell for high reliability

DESCRIPTION

The QS86442 is a high-speed 256K TAG RAM organized as 64K words of 4-bits. It is manufactured in a high-performance CMOS process, and it is based on a 8-transistor cell design for high reliability of data retention. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW



High-Speed CMOS 64Kx4 SRAM with Separate I/O

QS86444
QS86449
ADVANCE
INFORMATION

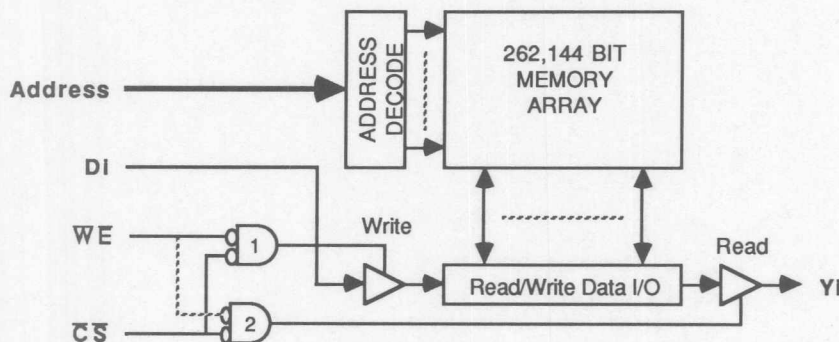
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 15ns/20ns/25ns Commercial
- 20ns/25ns/35ns Military
- TTL compatible I/O
- Low Standby current
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 28-pin DIPs, 28-pin 300 mil
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883

DESCRIPTION

The QS86444 and QS86449 are high-speed 256K SRAMs organized as 64Kx4 with separate read and write data buses. In the 86444, the read data outputs follow the inputs during a write; in the 86449, the outputs are disabled during a write. The 86444 and 86449 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

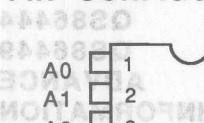
FUNCTIONAL BLOCK DIAGRAM



Note:

WE is not connected to Output Enable Gate 2 in the 86444.

WE is connected to Output Enable Gate 2 as shown in the 86449.



PDIP, SOIC

ALL PINS TOP VIEW



High-Speed CMOS 64Kx4 SRAM with Output Enable

QS86446
ADVANCE
INFORMATION

FEATURES/BENEFITS

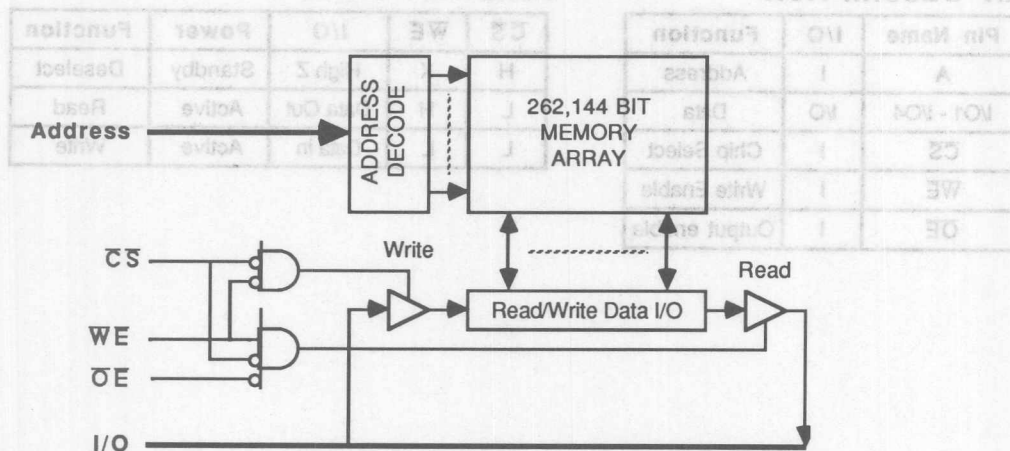
- High Speed Access and Cycle times
- 12ns/15ns/20ns/25ns Commercial
- 15ns/20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B

- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 28-pin DIP & 300 mil SOJ
- JEDEC standard pinout
- Low Standby current

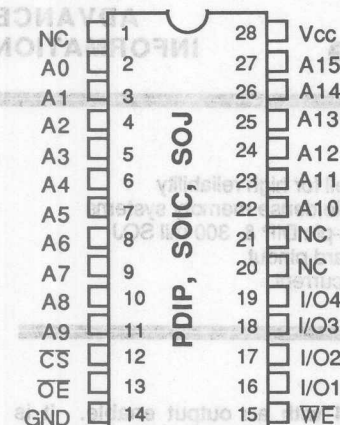
DESCRIPTION

The QS86446 is a high-speed 256K SRAM organized as 64Kx4 with an output enable. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS86446 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ALL PINS TOP VIEW

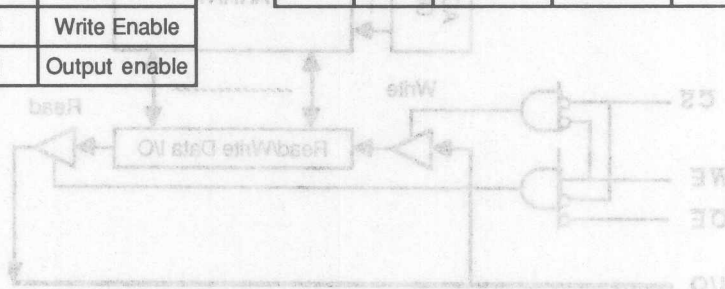
* For LCC pinout contact factory

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O4	I/O	Data
$\overline{CS}$	I	Chip Select
WE	I	Write Enable
$\overline{OE}$	I	Output enable

FUNCTION TABLE

$\overline{CS}$	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V		
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$	Parameter	Symbol
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$		
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V		
DC Output Current Max. sink current/pin.....	50 mA	Input HIGH Voltage	V_{IH}
DC Output Current Max. source current/pin.....	30 mA	Input LOW Voltage (1)	V_{IL}
T_{BIAS} Temperature Under Bias, COM.....	-65° to +125°C	Output HIGH Voltage	V_{OH}
T_{STG} Storage Temperature, COM.....	-65° to +125°C	Output LOW Voltage	V_{OL}
T_{BIAS} Temperature Under Bias, MIL.....	-65° to +135°C		
T_{STG} Storage Temperature, MIL.....	-65° to +155°C		

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

CAPACITANCE

$T_a = +25^\circ\text{C}$, $f = 1$ MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	$V_{in} = 0$ V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	$V_{in} = 0$ V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	$V_{out} = 0$ V PDIP Pkg.		7	pF
Cout	Output Capacitance	$V_{out} = 0$ V SOJ Pkg.		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

Symbol	Parameter	C	M	C	M	C	M	C	M	Am
I_{OQ1}	Static Operating Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IH}$, $t = 0$	100	120	100	120	100	120	100	120	120
I_{OQ2}	Dynamic Operating Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IH}$, $t = 1 \text{ MAX}$	170	-	185	175	185	185	185	145	155
I_{QB}	TTL Standby Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IH}$, $t = 1 \text{ MAX}$	80	100	80	100	80	100	80	100	100
I_{QB1}	Full Standby Current, $V_{CC} = \text{MAX}$ Outputs open $CS \leq V_{IH}$, $t = 0$ $V_{in} \leq V_{IH}$ or $V_{in} \geq V_{IH}$	15	20	15	20	15	20	15	20	20

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-12		15		-20		-25/-35		Unit
		C	M	C	M	C	M	C	M	
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	120	100	120	100	120	100	120	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	170	-	165	175	155	165	145	155	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	90	100	90	100	90	100	90	100	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	20	15	20	15	20	15	20	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±10% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15(3)		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE											
t RC	Read Cycle Time	12	-	15	-	19	-	25	-	35	-
t AA	Address Access Time	-	12	-	15	-	19	-	25	-	35
t ACS	Chip Select Access Time	-	12	-	15	-	19	-	25	-	35
t OH	Output Hold from Address Change	2	-	2	-	3	-	3	-	3	-
tCLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-	3	-
tCHZ	Chip Select to Output in High Z (2)	-	5	-	7	-	8	-	10	-	15
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2)	-	12	-	15	-	19	-	25	-	35
tOE	Output Enable to Data Valid	-	6	-	6	-	8	-	10	-	14
tOLZ	Output Enable to Output in Low-Z (2)	2	-	2	-	2	-	2	-	2	-
tOHZ	Output Enable to Output in High-Z (2)	-	4	-	5	-	7	-	8	-	10

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5%. Commercial Only-Preliminary Data.

QS86446

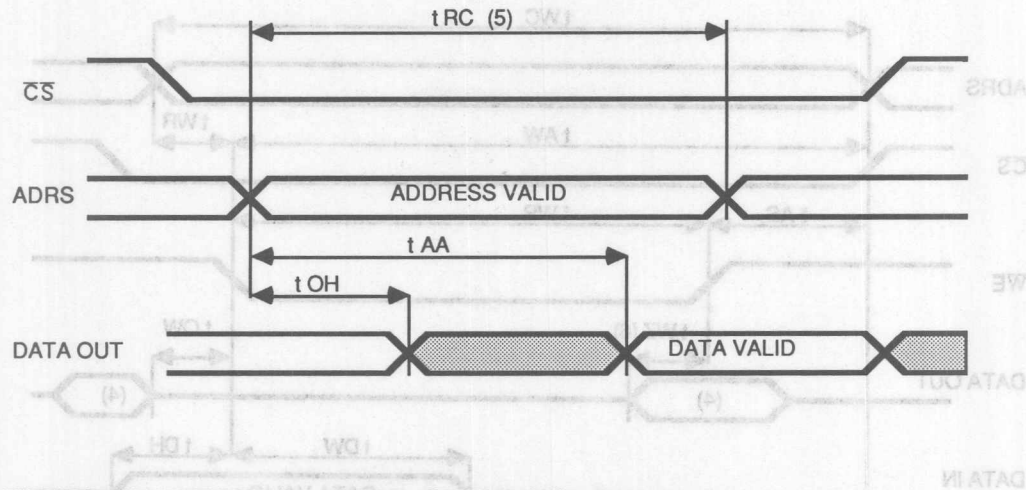
Commercial TA = 0° C to 70°C, Vcc = 5.0V±10% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter (1)	-12 (3)		-15(3)		-20		-25		-35	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	12	-	15	-	19	-	25	-	35	-
t CW	Chip Select Valid to End of Write	10	-	13	-	17	-	20	-	30	-
t AW	Address Valid to End of Write	10	-	13	-	17	-	20	-	30	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-	0	-
t WP	Write Pulse width	10	-	12	-	16	-	20	-	30	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	6	-	8	-	10	-	13	-	18	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in High Z (2)	-	5	-	6	-	7	-	8	-	12
t OW	Output Active from End of Write(2)	2	-	2	-	2	-	2	-	3	-

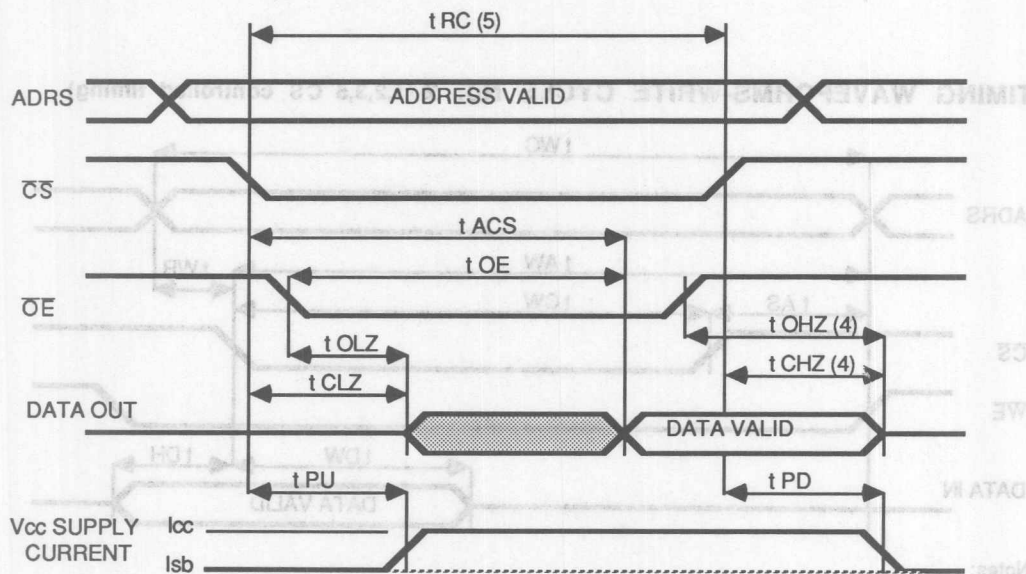
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) For Vcc±5% Commercial Only-Preliminary Data

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2)



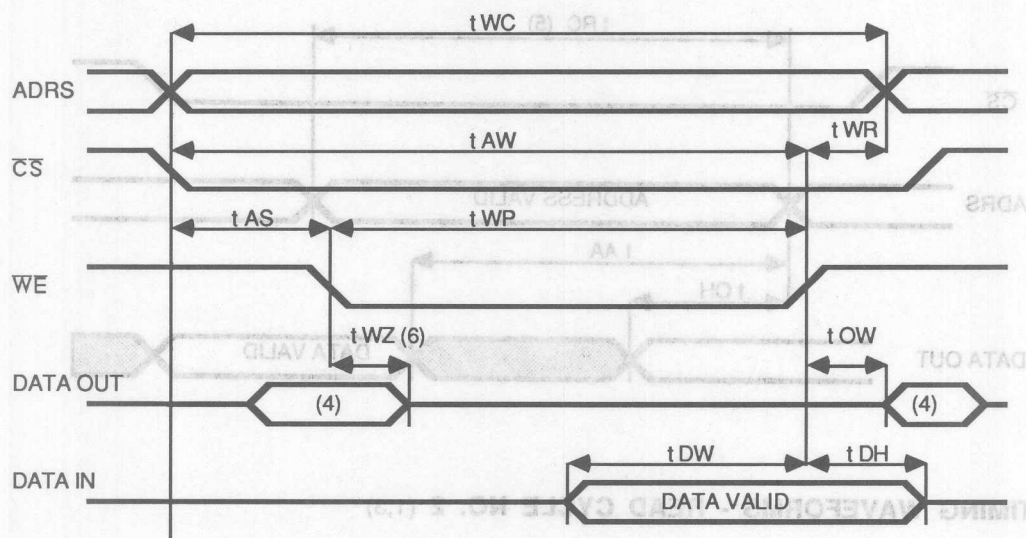
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3)



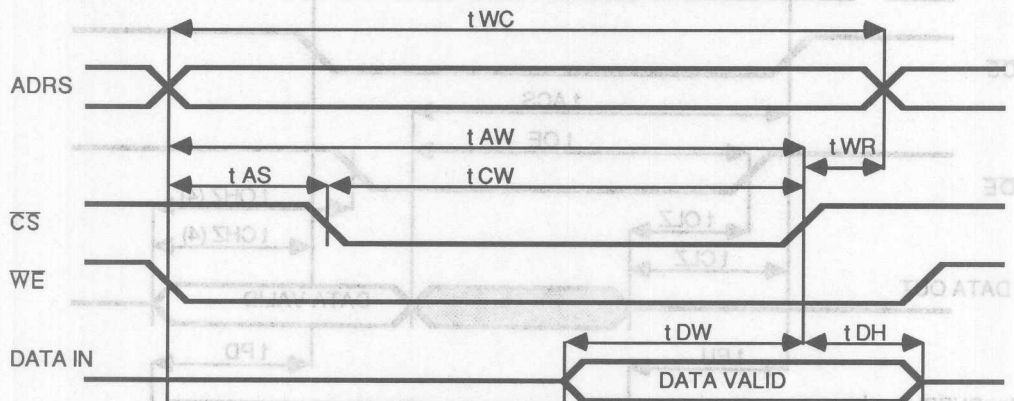
Notes:

1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3 WE controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,5 CS controlled timing)



Notes:

1. WE or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low WE.
3. t_{WR} is measured from the earlier of $\overline{CS}$ and WE going high to end of the write cycle.
4. During this period the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.
6. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.



High-Speed CMOS 64Kx4 SRAM with Address Latch

**QS86447
ADVANCE
INFORMATION**

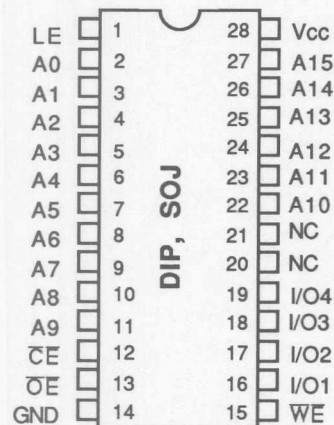
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 15ns/20ns/25ns/35ns Commercial
- Common I/O with Output Enable
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 300-mil, 28-pin DIP and SOJ
- Address input latches with single clock control
- TTL compatible I/O

DESCRIPTION

The QS86447 is a high-speed 256K SRAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. The QS86447 input address latches make it useful in cache data RAM, cache tag RAMs, and other high speed memory applications. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

QS86447
ADVANCE
INFORMATION

High-Speed CMOS 64Kx4 SRAM with Address Latch



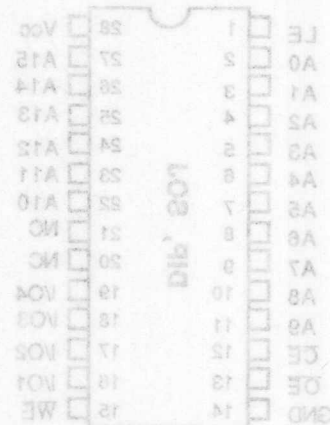
FEATURES/BENEFITS

- High Speed Access and Cycle times
- 15ns/50ns/30ns Commercial
- Common I/O with Output Enable
- Low power, high-speed CMOS technology
- Military product compliant to MIL-STD-883
- 8-Transistor cell for high reliability
- Ideal for reliable, dense memory systems
- Available in 300-mil, 28-pin DIP and SOJ
- Address input latches with single clock control
- TTL compatible I/O

DESCRIPTION

The QS86447 is a high-speed 256K SRAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. The QS86447 input address latches make it useful in cache data RAM, cache tag RAMs, and other high speed memory applications. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW



High-Speed CMOS 64Kx4 SRAM with Address Register

QS86448
ADVANCE
INFORMATION

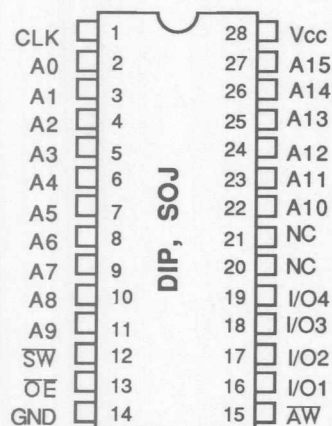
FEATURES/BENEFITS

- Fully synchronous, single clock operation
- 15ns/20ns/25ns/35ns Commercial
- Self timed write with late write abort
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883
- 6-Transistor cell for high reliability
- Ideal for reliable,dense memory systems
- Available in 300-mil, 28-pin DIP and SOJ
- Registered Address inputs
- TTL compatible I/O

DESCRIPTION

The QS86448 is a high-speed 256K SRAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. The QS86448 input address register makes it useful in cache data RAM, cache tag RAMs, and other high speed memory applications. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

QS86448
ADVANCE
INFORMATION

High-Speed CMOS 64Kx4 SRAM With Address Register



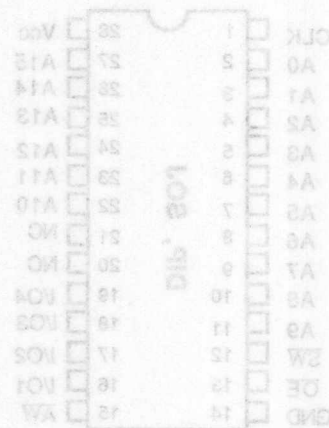
FEATURES/BENEFITS

- Fully synchronous, single clock operation
- 15nV/25nA/88ns Commercial
- Self timed with late write abort
- Low power, high-speed CMOS technology
- Military product compliant to MIL-STD-883
- TTL compatible I/O
- Registered Address Inputs
- Available in 300-mil, 28-pin DIP and SOJ
- Ideal for reliable, dense memory systems
- 8-Transistor cell for high reliability

DESCRIPTION

The QS86448 is a high-speed 256K SRAM organized as 64K words of 4 bits. It is manufactured in a high-performance CMOS process, and it is based on a 8-transistor cell design for high reliability of data retention. The QS86448 input address register makes it useful in cache data RAM, cache tag RAM, and other high speed memory applications. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW



High-Speed CMOS 128Kx8 SRAM

QS812880
ADVANCE
INFORMATION

FEATURES/BENEFITS

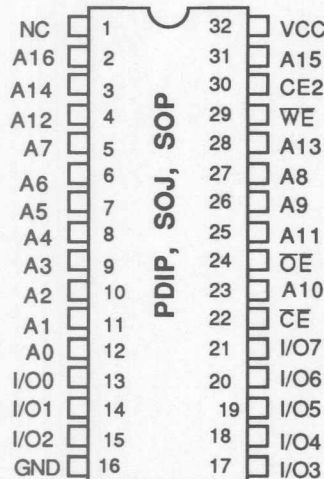
- Equal access and cycle times
- 20ns/25ns/30 ns Commercial
- 25ns/30 ns Military
- Common I/O with output enable
- Military product compliant to MIL-STD-883
- High performance QCMOS™ technology
- Dual chip select
- 6-Transistor cell for high reliability
- TTL compatible I/O
- High performance QCMOS™ technology
- Available in 400-mil 32-pin PDIP, 32-pin SOP, & 32-pin SOJ with JEDEC standard pinout

2

DESCRIPTION

The QS812880 is a high-speed 1024K SRAM organized as 128K words of 8 bits. It has two chip select control lines, and common I/O with output enable. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the QS812880 make it useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

Q881288Q
ADVANCE
INFORMATION

High-Speed CMOS 128Kx8 SRAM



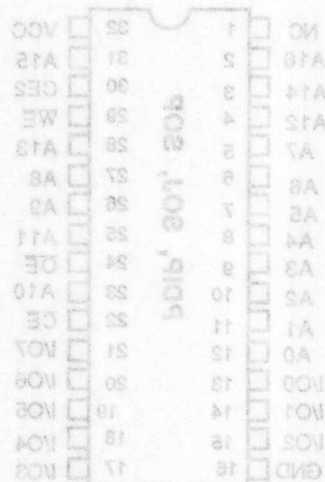
FEATURES/BENEFITS

- High performance CMOS™ technology
- Military product compliant to MIL-STD-883C
- Common NO with output enable
- 28-pin SOI as Military
- 28-pin SOI as Commercial
- Equal access and cycle times
- Dual chip select
- 6-Transistor cell for high reliability
- High performance CMOS™ technology
- TTL compatible I/O
- Available in 400-mil 28-pin PDIP, 32-pin SOP, & 32-pin SOI with JEDEC standard pinout

DESCRIPTION

The Q881288Q is a high-speed 1024K SRAM organized as 128K words of 8 bits. It has two chip select control lines, and common NO with output enable. It is manufactured in a high-performance CMOS process, and it is based on a 6-transistor cell design for high reliability of data retention. The high-speed access times of the Q881288Q make it useful in cache data RAM, cache tag RAM, high-speed scratchpad memories, look-up tables, pipelined DSP, and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

PIN CONFIGURATIONS



ALL PINS TOP VIEW

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FCT-T Logic Products	4
QuickSwitch Products	5
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Quality And Reliability	7
Package Information	8
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1	General Information
2	Static RAM Products
3	Static Memory Products
4	FCT-T Logic Products
5	QuickSwitch Products
6	Application Notes
7	Quality And Reliability
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9	Sales Offices

FIFO Table of Contents

FIFO MEMORY DATA SHEETS

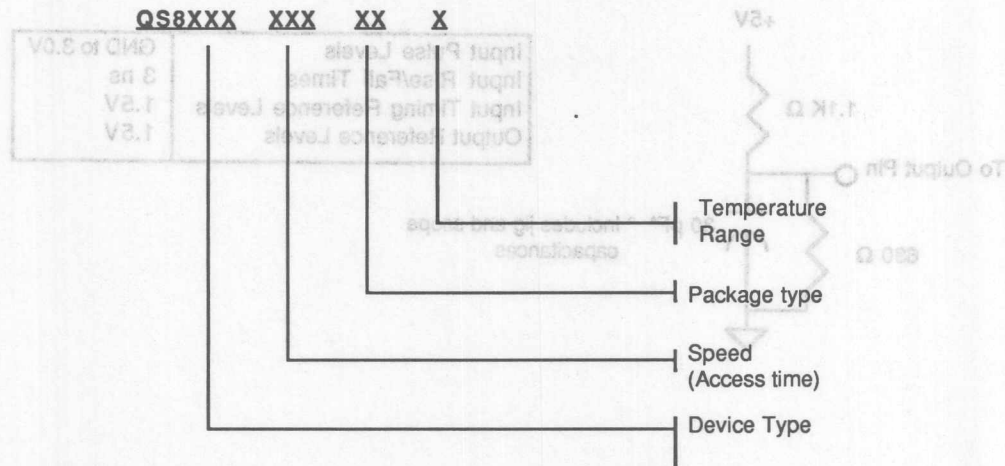
	Page
FIFO Ordering Information	3-3
FIFO Test Configuration	3-4
QS7201/2	512x9 and 1Kx9 FIFO
QS7203/4	2K and 4Kx9 FIFO
QS7211/2	512x9 and 1Kx9 FIFO with Output Enable
QS7223/4	2Kx9 and 4Kx9 Clocked FIFO
QS7306	64Kx4 Ultra Deep FIFO
QS7316	64Kx4 Burst Mode Dual Port RAM

FIFO Table of Contents

FIFO MEMORY DATA SHEETS

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3-3	FIFO Ordering Information	
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3-67	64Kx4 Ultra Deep FIFO	Q87308
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FIFO Ordering Information



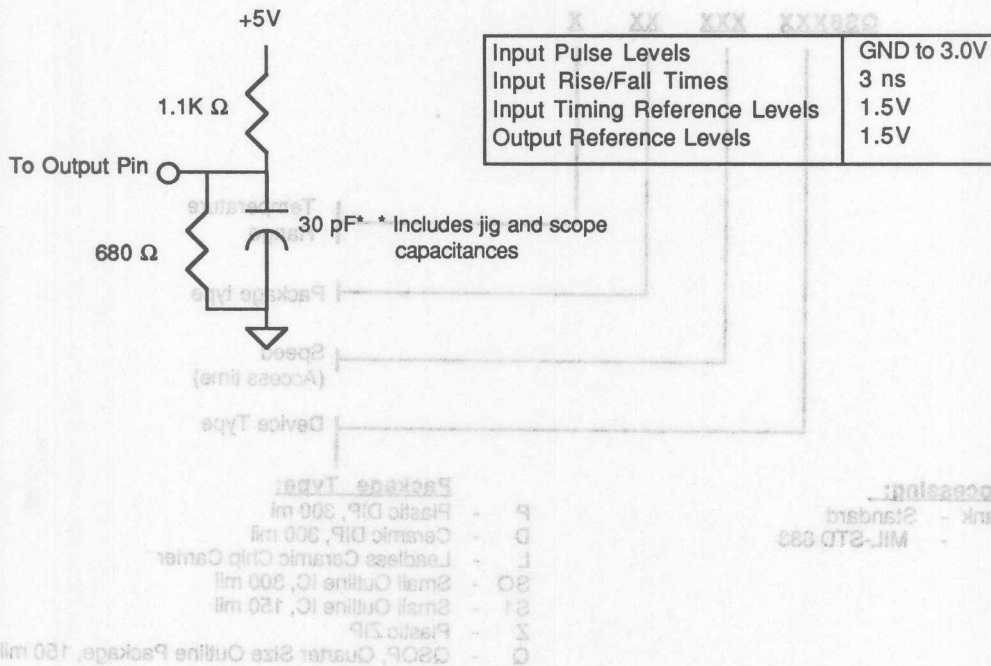
Processing:

Blank - Standard
B - MIL-STD 883

Package Type:

P - Plastic DIP, 300 mil
D - Ceramic DIP, 300 mil
L - Leadless Ceramic Chip Carrier
SO - Small Outline IC, 300 mil
S1 - Small Outline IC, 150 mil
Z - Plastic ZIP
Q - QSOP, Quarter Size Outline Package, 150 mil

FIFO Test Configuration



Q

High Speed CMOS 9-bit FIFO Buffer Memories

512x9: QS7201
1Kx9: QS7202

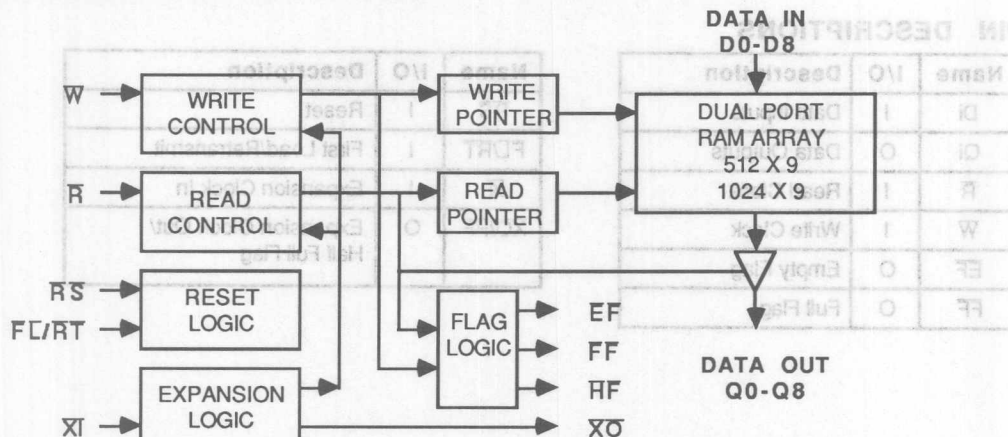
FEATURES/BENEFITS

- 15 ns flag and data access times
- Fully Asynchronous Read and Write
- Zero fall-through time
- Expandable in depth with no speed loss
- TTL input and output level compatible
- Military product compliant to MIL-STD-883, Class B
- 40 MHz cycle time
- Retransmit capability
- Dual Port RAM-based cell using 6T technology
- Available in 300 mil/600 mil PDIP, SOIC, SOJ, 300 mil/600 mil CERDIPs, PLCC, LCC
- Low Power with Industry standard pinouts

DESCRIPTION

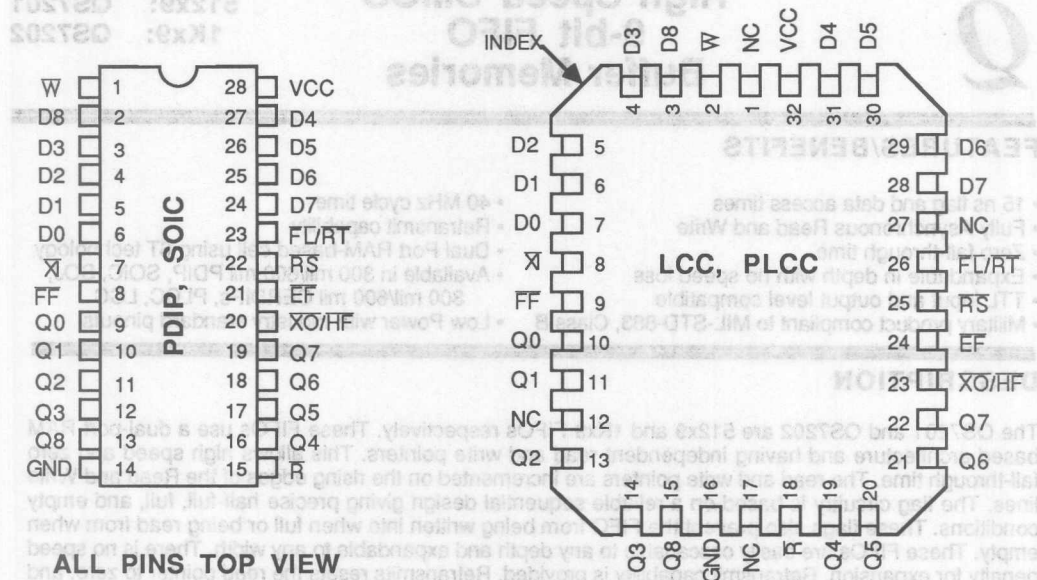
The QS7201 and QS7202 are 512x9 and 1Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. These FIFOs are easily cascadable to any depth and expandable to any width. There is no speed penalty for expansion. Retransmit capability is provided. Retransmits resets the read pointer to zero, and is useful for data communications and digital filtering applications.

FUNCTIONAL BLOCK DIAGRAM



Note: XO and HF share the same pin so the half-full flag is available only in standalone, not depth expansion mode.

PINOUTS



PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
R	I	Read Clock
W	I	Write Clock
EF	O	Empty Flag
FF	O	Full Flag

Name	I/O	Description
RS	I	Reset
FL/RT	I	First Load/Retransmit
X	I	Expansion Clock In
XO/HF	O	Expansion Clock Out/ Half Full Flag

FUNCTION TABLES

RESET AND RETRANSMIT FUNCTION TABLE

Stand Alone Device or Width Expansion

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	(3)	(3)	(3)
Read/Write	H	H	L	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes:

- (1) The Read Pointer will increment if the FIFO is not empty.
- (2) The Write flag will increment if the FIFO is not full.
- (3) The flags will change after the retransmit operation and will correspond to the read pointer being at location zero.
- (4) The flags will reflect the relative locations of the read and write pointers.

3

RESET AND FIRST LOAD FUNCTION TABLE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset 1st Device	L	L	(1)	Location Zero	Location Zero	L	H	H
Reset Other Devices	H	H	(1)	Location Zero	Location Zero	(3)	(3)	(3)
Read/Write	H	(2)	(1)	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes

- (1) The Expansion In (XI) is connected to the Expansion Out (XO) of the previous device.
- (2) The device with FL tied low will receive the first N writes and first N reads, where N is the FIFO size. On the Nth write, the XO pulse is sent to the next device to indicate that it will receive the (N+1)th write. Similarly on the Nth read another XO pulse is sent to the next device to indicate that it will output the (N+1)th read.
- (3) The read and write pointers will be activated according to whether the FIFO received a n XO pulse, or whether they were the first device in the daisy chain. The flags will reflect the empty or full conditions for the individual FIFOs. To create the composite Full and Empty flags, an OR-ing of the individual flags is required.
- (4) The flags will reflect the relative locations of the read and write pointers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Input Diode Current with $V_I > V_{CC}$	20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Diode Current with $V_O > V_{CC}$	50 mA
DC Output Current Max. sink current/pin.....	70 mA
DC Output Current Max. source current/pin.....	30 mA
Total DC Ground Current.....	($N \times I_{OL} + M \times \Delta I_{CC}$) mA
Total DC VCC Power Supply Current.....	($N \times I_{OH} + M \times \Delta I_{CC}$) mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
TSTG Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V	5	8	pF
Cout	Output Capacitance	Vout = 0 V	5	8	pF

Note: Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
V_{ih}	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
V_{il}	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
V_{oh}	Output HIGH Voltage	$I_{oh} = -2\text{ mA}$, $V_{cc} = \text{MIN}$	2.4		2.4		
V_{ol}	Output LOW Voltage	$I_{ol} = 8\text{ mA}$, $V_{cc} = \text{MIN}$		0.4		0.4	
$ I_{ii} $	Input Leakage	$V_{cc} = \text{MAX}$, $V_{in} = \text{GND to } V_{cc}$		1		10	μA
$ I_{lo} $	Output Leakage	$V_{cc} = \text{MAX}$, $V_{out} = \text{GND to } V_{cc}$		10		10	

Notes:

- Transient inputs with V_{il} not more negative than -1.5 volts are permitted for pulse widths $\leq 10\text{ ns}$

POWER SUPPLY CHARACTERISTICS

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 $V_{lc} = 0.2\text{ Volts}$, $V_{hc} = V_{cc} - 0.2\text{ Volts}$

Symbol	Parameter	≤ 35		≥ 50		Unit
		C	M	C	M	
I_{cc1}	Operating Operating Current $V_{cc} = \text{MAX}$, Outputs open	100	120	100	120	mA
I_{cc2}	Standby Current $R = W = RS = FL/RT = V_{ih}$	15	20	8	15	
I_{sb}	Power Down Current All Inputs at V_{hc} or V_{lc} $R = W = RS = FL/RT = V_{hc}$	5	9	5	9	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^\circ C$ to $+70^\circ C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^\circ C$ to $+125^\circ C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
READ CYCLE											
f _{RF}	Read Frequency, MHz	2	40	33	28	22	15	10	7	MHz	Min
t _{RC}	Read Cycle Time		25	30	35	45	65	100	140	ns	
t _A	Read Access Time		15	20	25	35	50	80	120		Max
t _{RR}	Read Recovery Time		10	10	10	10	15	20	20		Min
t _{RPW}	Read Pulse Width	1	15	20	25	35	50	80	120		
t _{RLZ}	RData Bus Low Z	2	3	3	3	3	3	3	3		
t _{WLZ}	WData Bus LowZ	2,3	3	3	3	3	3	3	3		
t _{DV}	Rhigh to Data Hold Time		5	5	5	5	5	5	5		
t _{RHZ}	Rto Data High Z		14	18	18	20	30	35	35		Max
WRITE CYCLE											
f _{WF}	Write Frequency,MHz	2	40	33	28	22	15	10	7	MHz	Min
t _{WC}	Write Cycle Time		25	30	35	45	65	100	140	ns	
t _{WPW}	Write Pulse Width	1	15	20	25	35	50	80	120		
t _{WR}	Write Recovery Time		10	10	10	10	15	20	20		
t _{DS}	Write Data Setup Time		9	12	15	18	30	40	40		
t _{DH}	Write Data Hold Time		0	0	0	0	0	0	0		
RESET AND RETRANSMIT CYCLES											
t _{RSC}	Reset Cycle Time		25	30	35	45	65	100	140	ns	Min
t _{RS}	Reset Pulse Width	1	15	20	25	35	50	80	120		
t _{RSS}	Reset Setup Time		15	20	25	35	50	80	120		
t _{RSR}	Reset Recovery Time		10	10	10	10	15	20	20		
t _{RTC}	Retransmit Cycle Time		25	30	35	45	65	100	140		
t _{RT}	Retransmit Pulse Width	1	15	20	25	35	50	80	120		
t _{RTS}	Retransmit Setup Time	2	15	20	25	35	50	80	120		
t _{RTR}	Retransmit Recovery		10	10	10	10	15	20	20		

Notes: These timings are measured as defined in AC Test Conditions

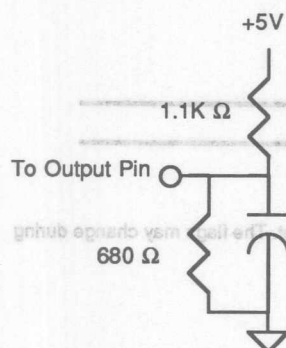
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. This applies to the read data flow-through mode only.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
 COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^{\circ}C$ to $+70^{\circ}C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
FLAG TIMING											
t REF	Read Low to $\overline{EF}$ Low		15	20	25	30	45	60	60	ns	Max
t RFF	Read High to $\overline{FF}$ High		15	20	25	30	45	60	60		
t RHF	Read High to $\overline{HF}$ High		15	20	25	35	45	60	60		
t RPE	Read Pulse after $\overline{EF}$ High		15	20	25	35	50	80	120		
t WEF	Write High to $\overline{EF}$ High		15	20	25	30	45	60	60		
t WFF	Write Low to $\overline{FF}$ Low		15	20	25	30	45	60	60		
t WHF	Write Low to $\overline{HF}$ Low		15	20	25	35	45	60	60		
t WPF	Write Pulse after $\overline{EF}$ Hi		15	20	25	35	50	80	120		
t EFL	Reset to $\overline{EF}$ Low		15	20	25	35	45	60	60		
t FFH	Reset to $\overline{FF}$ High		15	20	25	35	45	60	60		
t HFH	Reset to $\overline{HF}$ High		15	20	25	35	45	60	60		
EXPANSION TIMING											
t XOL	Read/Write to $\overline{XO}$ Low		15	20	25	35	50	80	120	ns	Max
t XOH	Read/Write to $\overline{XO}$ High		15	20	25	35	50	80	120		
t XI	$\overline{XI}$ Pulse Width		15	20	25	35	50	80	120		
t XIR	$\overline{XI}$ Recovery Time		10	10	10	10	10	10	10		Min
t XIS	$\overline{XI}$ Setup Time		10	15	15	15	15	15	15		

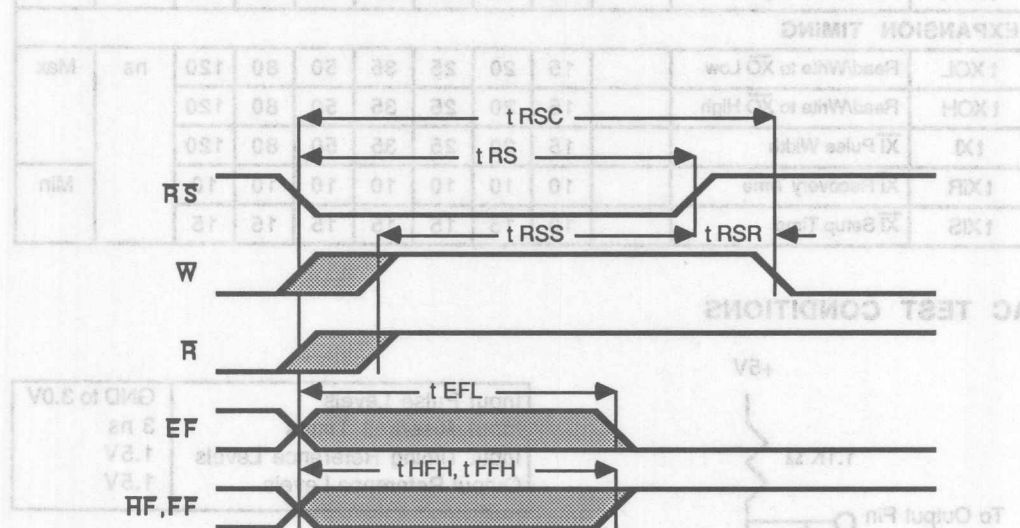
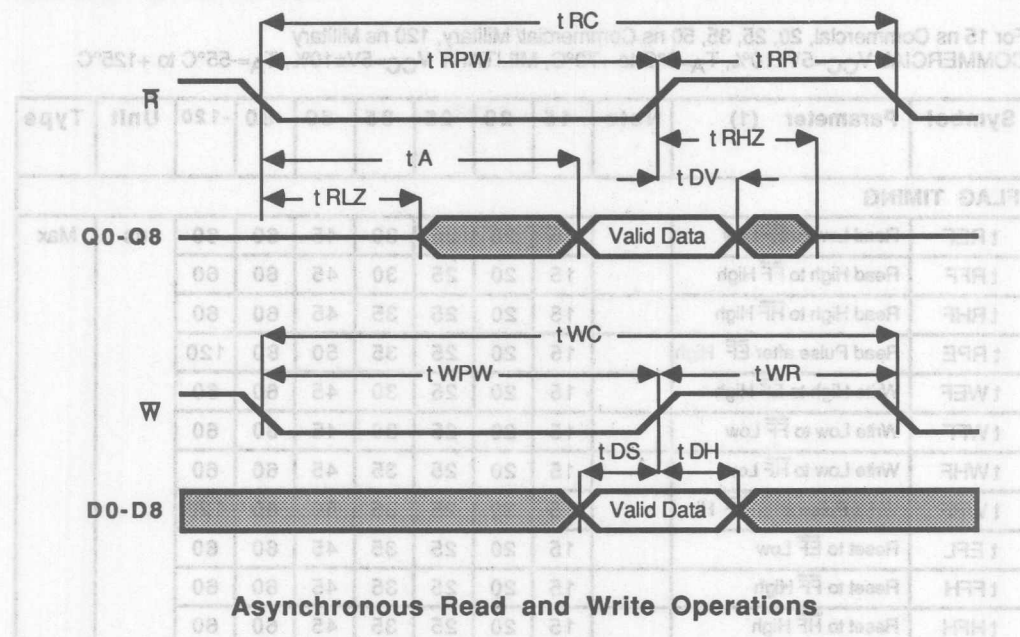
AC TEST CONDITIONS



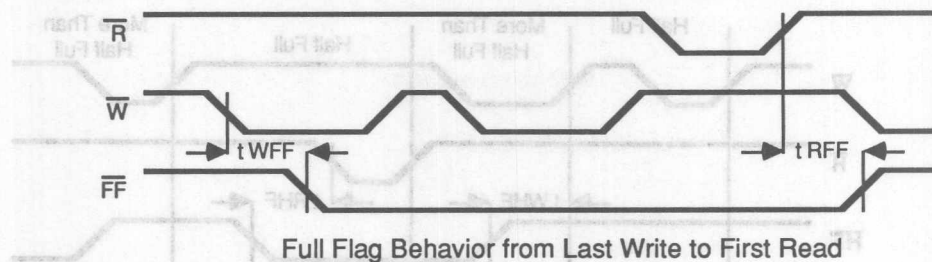
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

30 pF* * Includes jig and scope capacitances

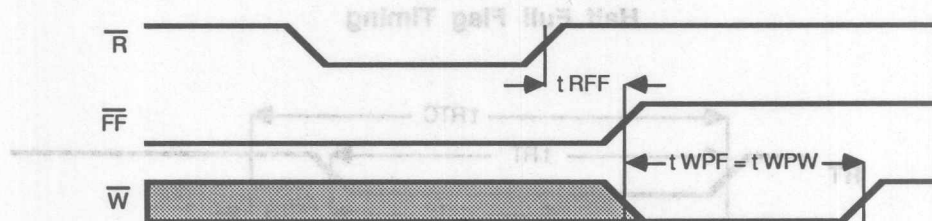
TIMING DIAGRAMS



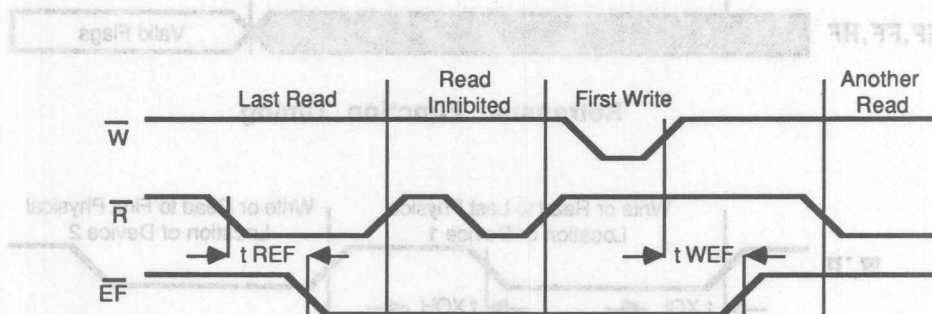
Notes: Read and Write have to be at a HIGH level around the rising edge of Reset. The flags may change during reset but are valid at tRSC.



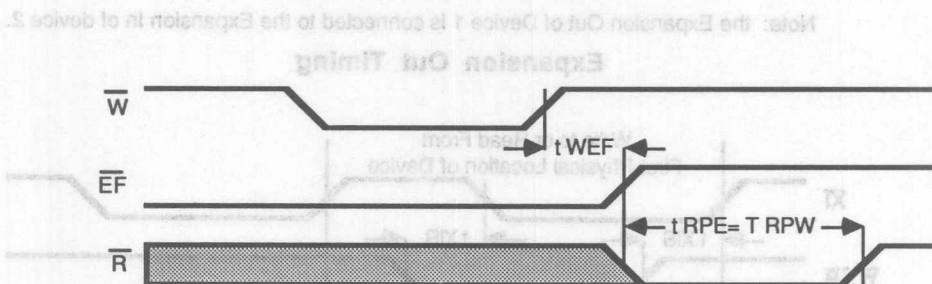
Full Flag Behavior from Last Write to First Read



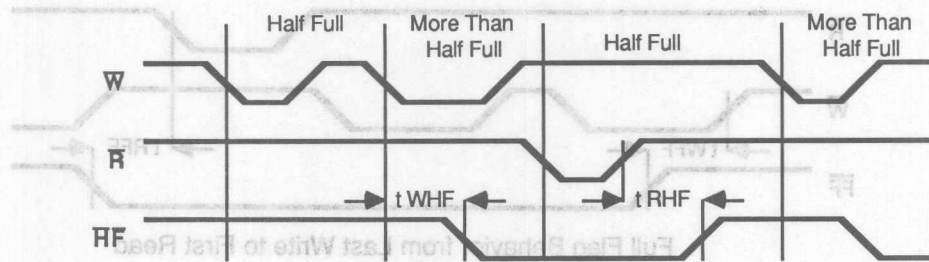
Full Flag and Required Write Pulse at Full Condition



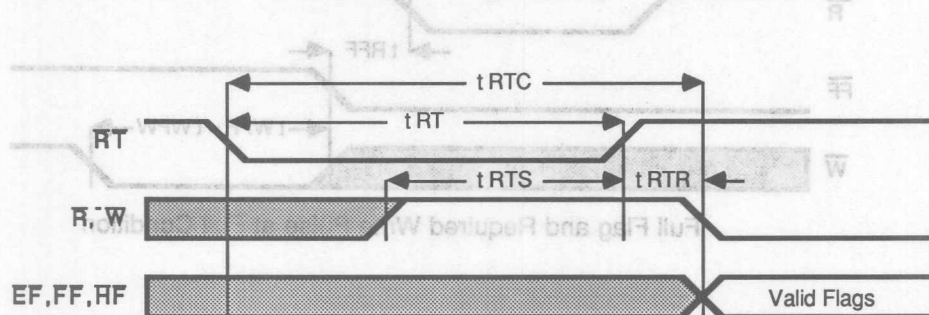
Empty Flag Behavior from Last Read to First Write



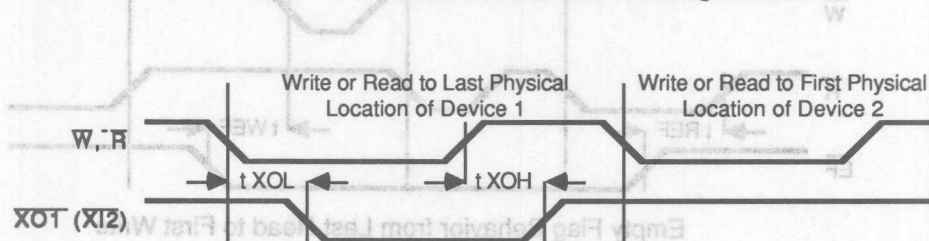
Empty Flag and Required Pulse Width at Empty Condition



Half Full Flag Timing

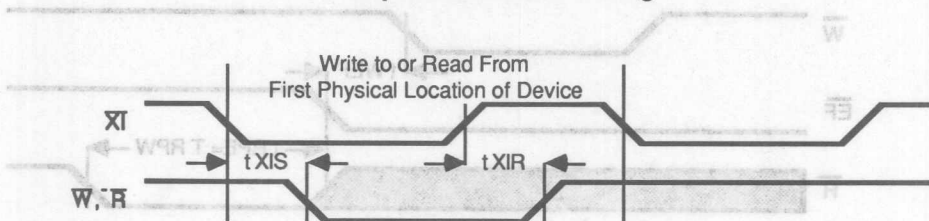


Retransmit Function Timing

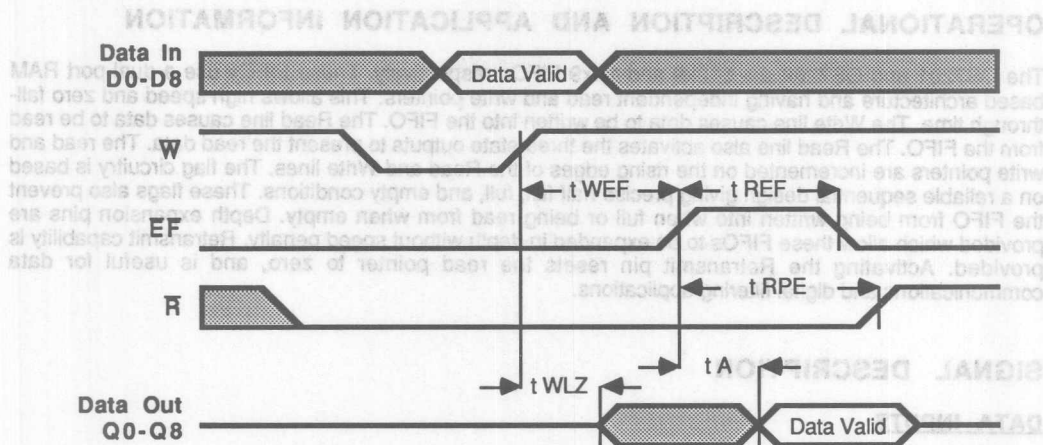


Note: the Expansion Out of Device 1 is connected to the Expansion In of device 2.

Expansion Out Timing

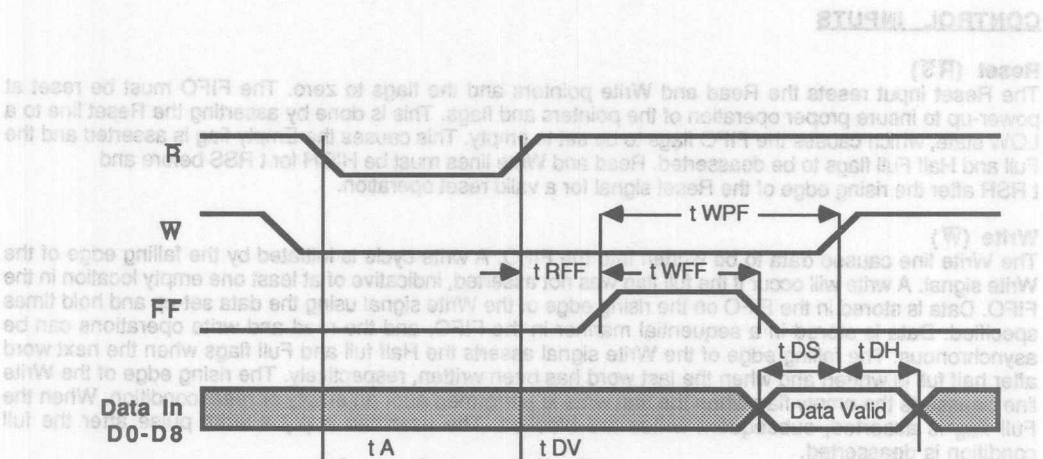


Expansion In Timing



The Data In lines D0 to D8 provide data to be written into the FIFO. Note: unused inputs must be tied to V_{CC} or Gnd.

3



The Read signal causes data to be read from the FIFO. A read is performed if the empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write signal. After the Read control is deasserted the data outputs go from a valid state into high-impedance. The output of the Read signal is active low. When all the data is read on the next read cycle, the Empty flag is asserted and the Read signal is deasserted, allowing the next read cycle to begin. The output may also be in high-impedance when the FIFO is empty. In this case, only the active FIFO asserts data, and the other FIFOs data outputs are in high-impedance. The falling edge of the read signal will set the Empty flag during the read of the last word in the FIFO. The falling edge of the read signal will deassert the Full flag when the Full flag has reached half full and when the FIFO was full, respectively.

OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS7201 and QS7202 are 512x9 and 1Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The Write line causes data to be written into the FIFO. The Read line causes data to be read from the FIFO. The Read line also activates the three-state outputs to present the read data. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Depth expansion pins are provided which allow these FIFOs to be expanded in depth without speed penalty. Retransmit capability is provided. Activating the Retransmit pin resets the read pointer to zero, and is useful for data communications and digital filtering applications.

SIGNAL DESCRIPTION

DATA INPUTS

D₀-D₈

The Data In lines D₀ to D₈ provide data to be written into the FIFO. Note: unused inputs must be tied to Vcc or Gnd.

CONTROL INPUTS

Reset ($\overline{RS}$)

The Reset input resets the Read and Write pointers and the flags to zero. The FIFO must be reset at power-up to insure proper operation of the pointers and flags. This is done by asserting the Reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag to be asserted and the Full and Half Full flags to be deasserted. Read and Write lines must be HIGH for t_{RSS} before and t_{RSR} after the rising edge of the Reset signal for a valid reset operation.

Write ($\overline{W}$)

The Write line caused data to be written into the FIFO. A write cycle is initiated by the falling edge of the Write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the Write signal using the data set-up and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the Write signal asserts the Half full and Full flags when the next word after half full is written and when the last word has been written, respectively. The rising edge of the Write line deasserts the empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read ($\overline{R}$)

The Read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the Read signal. A read is performed if the empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write operations. After the Read control is deasserted the data outputs go from a valid state into high-impedance. The outputs remain in high-impedance until the next read cycle. When all the data is read on the last read cycle, the Empty flag is asserted, and will inhibit any subsequent reads. The outputs will be in high-impedance for subsequent read operation until a write occurs that deasserts the Empty flag, allowing a read cycle to begin. The outputs may also be in high impedance when the FIFOs are cascaded in depth. In this case, only the active FIFO asserts data, and the other FIFOs data outputs are in high-impedance. The falling edge of the read signal will set the Empty Flag during the read of the last word in the FIFO. The rising edge of the Read signal will deassert the Half Full and the Full flags when the FIFO has reached half full and when the FIFO was full, respectively.

First Load/ Retransmit (FL/RT)

This is a dual purpose input. In the depth expansion mode, this pin indicates the first FIFO device that will be loaded or read from after a reset operation. In the standalone or width expansion mode (when the expansion input is grounded) this pin initiates the a retransmit function.

Retransmit resets the read pointer to zero. The Read and Write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing retransmit pin will cause the read pointer to be reset to zero and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

Expansion In (XI)

This is a dual purpose pin. When it is grounded then it indicates that the FIFO is a standalone device. When it is not grounded, it indicates that the FIFO is in the depth expansion mode. In the depth expansion mode this pin is connected to the $\overline{XO}$ pin of the previous device.

DATA OUTPUTS

Data Outputs Q_0 - Q_8

The 9-bit data output bus, Q_0 - Q_8 receives the read data from the FIFO. It is active whenever the Read signal is low. It is in a high impedance state when the Read signal is high. It is also in high impedance when the FIFO Empty flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag (FF)

The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag (EF)

The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the write signal deasserts the flag, as one word is now present in the FIFO.

Expansion Out/Half Full flag ($\overline{XO}$ /HF)

This is a dual purpose flag. In the single device mode, the Expansion In is grounded and the Half Full flag output is present on this pin. Whenever the FIFO is more than half full the flag remains asserted. When the FIFO is exactly half full and the next falling edge of the Write signal asserts the flag. The rising edge of read that causes the FIFO to be half full, will deassert the half full flag. It will remain asserted until the FIFO is half full or less than half full. The name given to the flag is half full, but it is asserted on the one plus the half full condition.

In the depth expansion mode, the Expansion Out is connected to the Expansion In of the next device. This causes the next device to perform write or read operations.

OPERATING MODES

SINGLE DEVICE MODE

A FIFO is in standalone mode when the Expansion In control is grounded. In this mode the half full flag is available on the shared XO/HF line. Figure 1 shows the standalone mode and this applies to FIFO width expansion, as shown in figure 2.

DEPTH EXPANSION MODE

A FIFO is in the depth expansion mode when the Expansion In control is not grounded but tied to the Expansion Out pin of the previous FIFO. Using the depth expansion mode, the 7201/02 can be easily cascaded to create FIFOs of larger depth. The devices are cascaded as shown in figure 3. In the depth expansion mode, the device that receives the first word of data has its First Load input grounded. The other devices have their First Load inputs in the high state. Two 4-input OR gates are required to create the composite Full and Empty flags for the FIFO array. In using the depth expansion mode, care must be taken to keep the traces short between the Expansion In of one device to the Expansion Out of the next device to minimize crosstalk noise.

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a read flow-through and a write flow-through, are supported by the FIFO. In the read flow-through mode the FIFO is empty, and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its Read line held low, and a write occurs. This rising edge of the Write would deassert the Empty flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The Read line being low would cause the data to be read and also assert the empty flag once again. The user must raise the Read line in order to increment the read pointer.

In the write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A write flow-through operation permits the writing of a single word of data immediately after reading one word of data from a full FIFO. This is similar to the read flow-through case, and the Write line must be toggled to increment the write pointer.

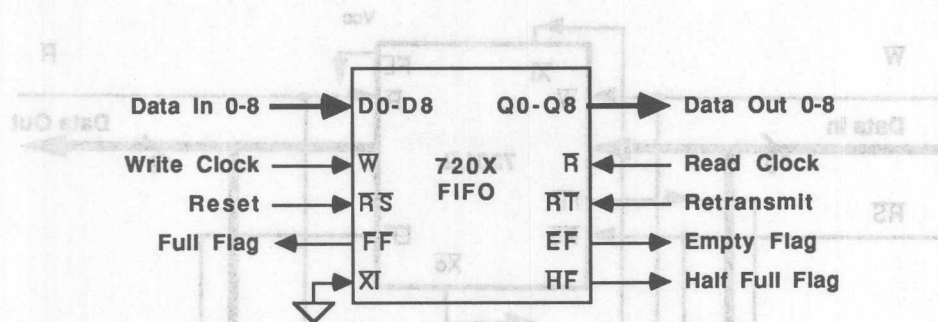


Figure 1. The FIFO in Standalone Mode.

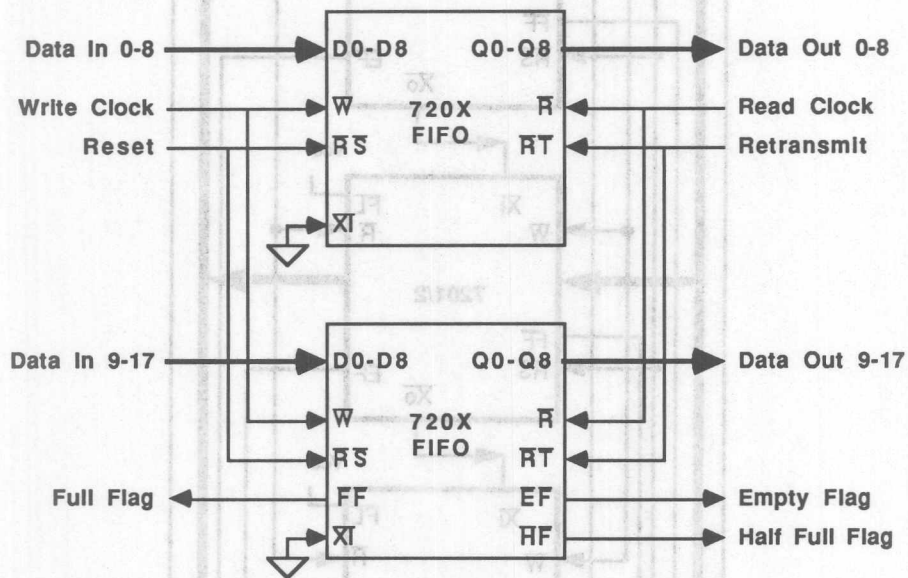
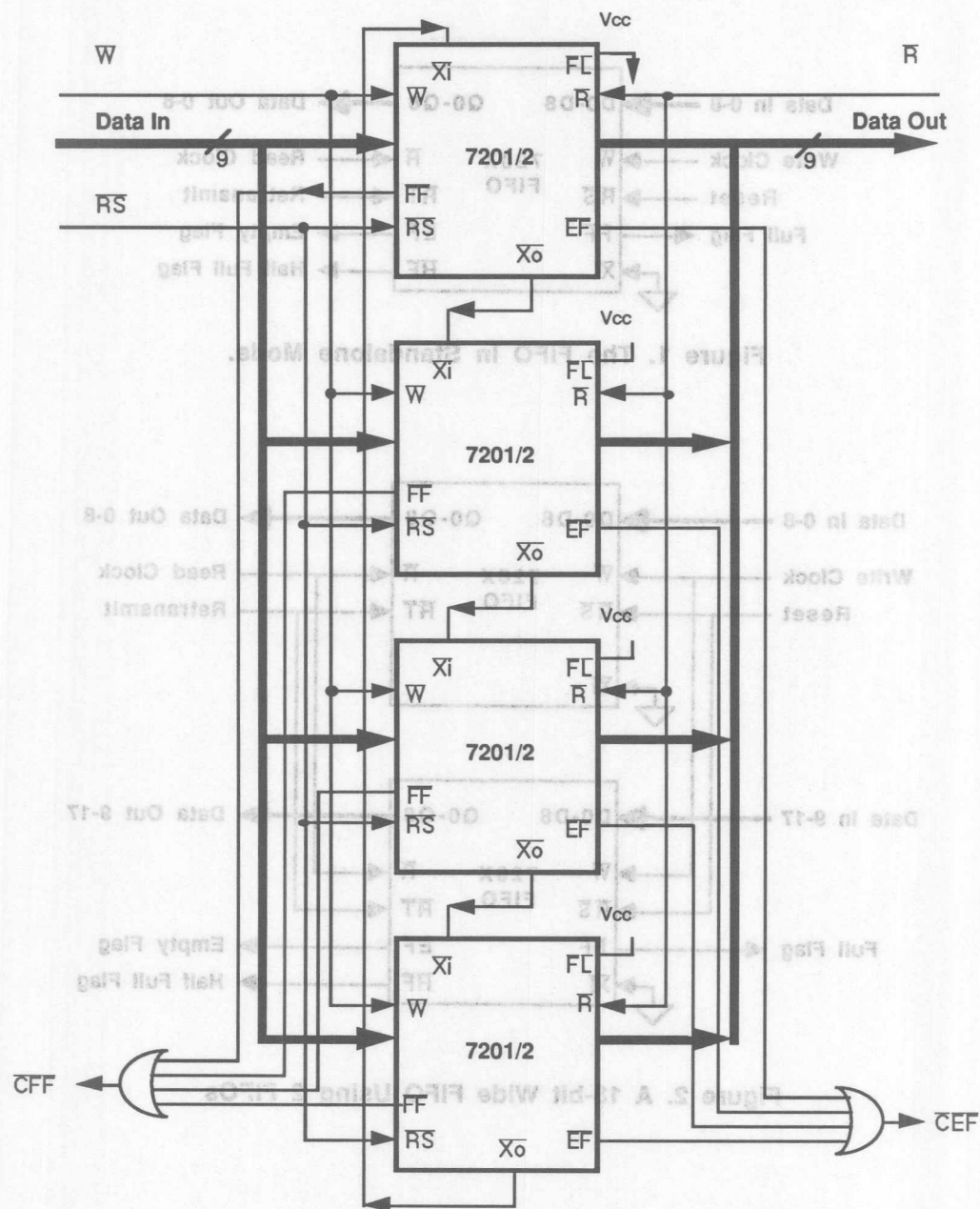


Figure 2. A 18-bit Wide FIFO Using 2 FIFOs

Note: The composite Empty and Full flags require the OR'ing of the individual Empty and Full flags, respectively.

Figure 3. Building a 4K-deep FIFO Using Four 1K-deep FIFOs



Note: The composite Empty and Full flags require the OR-ing of the individual Empty and Full flags, respectively

Figure 3. Building a 4N-deep FIFO Using Four N-deep FIFOs

Q

High Speed CMOS 9-bit FIFO Buffer Memories

2Kx9: QS7203
4Kx9: QS7204
PRELIMINARY

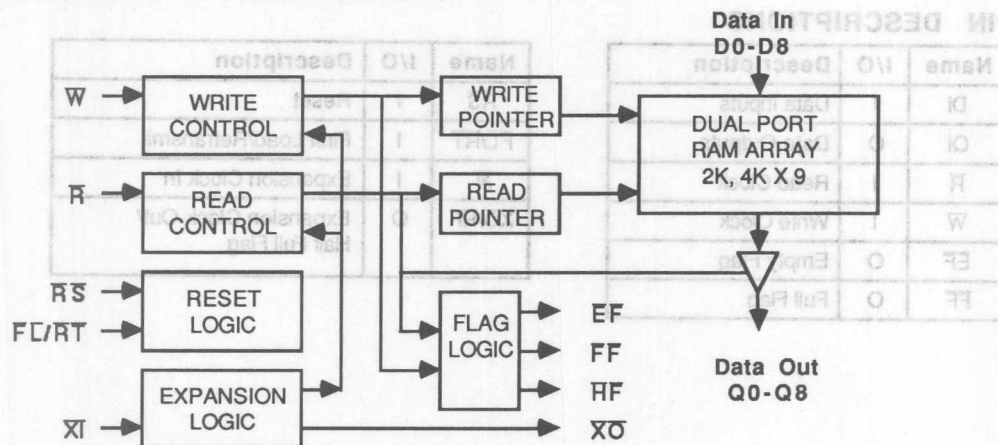
FEATURES/BENEFITS

- 15 ns flag and data access times
- Fully Asynchronous Read and Write
- Zero fall-through time
- Expandable in depth with no speed loss
- TTL input and output level compatible
- Military product compliant to MIL-STD-883, Class B
- 40 MHz cycle time
- Retransmit capability
- Dual Port RAM-based cell using 6T technology
- Available in 300 mil/600 mil PDIP, SOIC, SOJ, 300 mil/600 mil CerdIPs, PLCC, LCC
- Low Power with Industry standard pinouts

DESCRIPTION

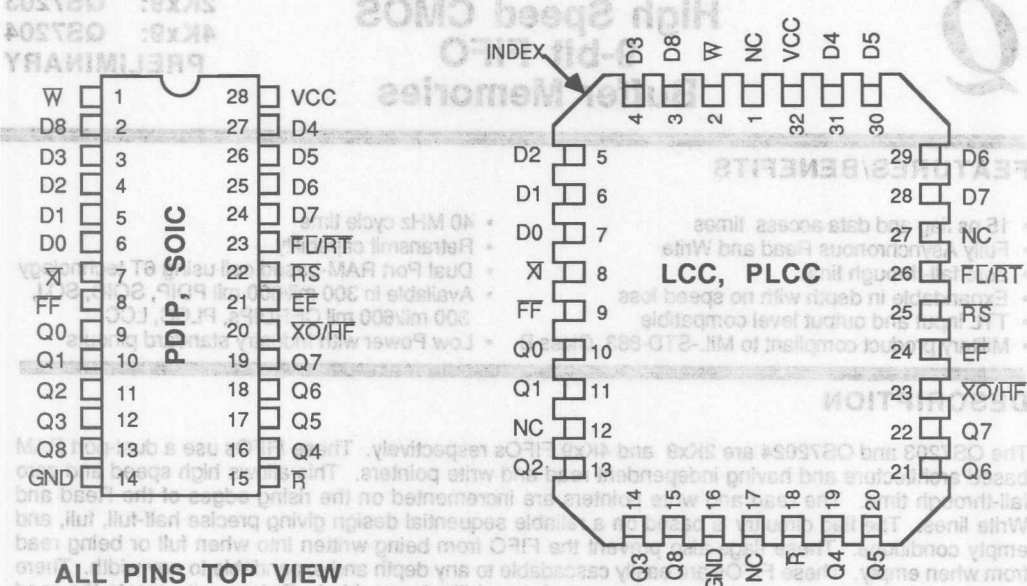
The QS7203 and QS7204 are 2Kx9 and 4Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. These FIFOs are easily cascadable to any depth and expandable to any width. There is no speed penalty for expansion. Retransmit capability is provided. Retransmits resets the read pointer to zero, and is useful for data communications and digital filtering applications.

FUNCTIONAL BLOCK DIAGRAM



Note: $\overline{X0}$ and $\overline{HF}$ share the same pin so the half-full flag is available only in standalone, not depth expansion mode.

PINOUTS



PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
R	I	Read Clock
W	I	Write Clock
EF	O	Empty Flag
FF	O	Full Flag

Name	I/O	Description
RS	I	Reset
FL/RT	I	First Load/Retransmit
X	I	Expansion Clock In
XO/HF	O	Expansion Clock Out/ Half Full Flag

Note: XO and HF share the same pin so the half-full flag is available only in expansion mode.

FUNCTION TABLES

RESET AND RETRANSMIT FUNCTION TABLE

Stand Alone Device or Width Expansion

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	(3)	(3)	(3)
Read/Write	H	H	L	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes:

- (1) The Read Pointer will increment if the FIFO is not empty.
- (2) The Write flag will increment if the FIFO is not full.
- (3) The flags will change after the retransmit operation and will correspond to the read pointer being at location zero.
- (4) The flags will reflect the relative locations of the read and write pointers.

RESET AND FIRST LOAD FUNCTION TABLE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	FL/RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset 1st Device	L	L	(1)	Location Zero	Location Zero	L	H	H
Reset Other Devices	H	H	(1)	Location Zero	Location Zero	(3)	(3)	(3)
Read/Write	H	(2)	(1)	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes

- (1) connected to the Expansion Out (XI) of the previous device.
- (2) The device with FL tied low will receive the first N writes and first N reads, where N is the FIFO size. On the Nth write, the XI pulse is sent to the next device to indicate that it will receive the (N+1)th write. Similarly on the Nth read another XI pulse is sent to the next device to indicate that it will output the (N+1)th read.
- (3) The read and write pointers will be activated according to whether the FIFO received a n XI pulse, or whether they were the first device in the daisy chain. The flags will reflect the empty or full conditions for the individual FIFOs. To create the composite Full and Empty flags, an OR-ing of the individual flags is required.
- (4) The flags will reflect the relative locations of the read and write pointers.

The Expansion In (XI) is

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....-0.5V to +7.0V.

DC Output Voltage V_O -0.5V to $V_{CC} + 0.5V$.

DC Input Voltage V_I $-0.5V$ to $V_{CC} + 0.5V$.

AC Input Voltage (for pulse width ≤ 20 ns).....-3.0 V

DC Input Diode Current with $V_I < 0$ -20 mADC Input Diode Current with $V_I > V_{CC}$ 20 mA

DC Output Diode Current with $V_O \leq 0$ -50 mA

DC Output Diode Current with $V_O \geq V_{CC}$	50 mA
--	-------

DC Output Current, Max. sink current/pin	70 mA
--	-------

DC Output Current Max. sink current/pin.....	15 mA
DC Output Current Max. source current/pin.....	30 mA

Total DC Ground Current..... (NxIOL +MxΔI CC) mA

Total DC VCC Power Supply Current..... (N $\times$ I_{OH} + M $\times$ I_{CC}) mA

N=Number of Outputs, M=Number of inputs

Maximum Power Dissipation.....0.5 watts

TSTG Storage Temperature..... -65° to $+165^{\circ}\text{C}$

CAPACITANCE

$T_a = 25\text{ }^\circ\text{C}$, $f = 1\text{ mHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V	5	8	pF
Cout	Output Capacitance	Vout = 0 V	5	8	pF

Note: Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
V_{ih}	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
V_{il}	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
V_{oh}	Output HIGH Voltage	$I_{oh} = -2\text{ mA}$, $V_{cc} = \text{MIN}$	2.4		2.4		
V_{ol}	Output LOW Voltage	$I_{ol} = 8\text{ mA}$, $V_{cc} = \text{MIN}$		0.4		0.4	
$ I_{ii} $	Input Leakage	$V_{cc} = \text{MAX}$, $V_{in} = \text{GND to } V_{cc}$		1		10	μA
$ I_{lo} $	Output Leakage	$V_{cc} = \text{MAX}$, $V_{out} = \text{GND to } V_{cc}$		10		10	

Notes:

1. Transient inputs with V_{il} not more negative than -1.5 volts are permitted for pulse widths $\leq 10\text{ ns}$

POWER SUPPLY CHARACTERISTICS

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 $V_{ic} = 0.2\text{ Volts}$, $V_{hc} = V_{cc} - 0.2\text{ Volts}$

Symbol	Parameter	≤ 35		≥ 50		Unit
		C	M	C	M	
I_{cc1}	Operating Operating Current $V_{cc} = \text{MAX}$, Outputs open	100	120	100	120	mA
I_{cc2}	Standby Current $R = W = RS = FL/RT = V_{ih}$	15	20	8	15	
I_{sb}	Power Down Current All Inputs at V_{hc} or V_{ic} $R = W = RS = FL/RT = V_{hc}$	5	9	5	9	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^\circ C$ to $+70^\circ C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^\circ C$ to $+125^\circ C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
READ CYCLE											
f RF	Read Frequency, MHz	2	40	33	28	22	15	10	7	MHz	Min
t RC	Read Cycle Time		25	30	35	45	65	100	140	ns	
t A	Read Access Time		15	20	25	35	50	80	120		Max
t RR	Read Recovery Time		10	10	10	10	15	20	20		Min
t RPW	Read Pulse Width	1	15	20	25	35	50	80	120		
t RLZ	$\overline{R}$ Data Bus Low Z	2	3	3	3	3	3	3	3		
t WLZ	$\overline{W}$ Data Bus Low Z	2,3	3	3	3	3	3	3	3		
t DV	$\overline{R}$ high to Data Hold Time		3	3	3	3	3	3	3		
t RHZ	$\overline{R}$ to Data High Z		14	18	18	20	30	35	35		
WRITE CYCLE											
f WF	Write Frequency, MHz	2	40	33	28	22	15	10	7	MHz	Min
t WC	Write Cycle Time		25	30	35	45	65	100	140	ns	
t WPW	Write Pulse Width	1	15	20	25	35	50	80	120		
t WR	Write Recovery Time		10	10	10	10	15	20	20		
t DS	Write Data Setup Time		8	12	15	18	30	40	40		
t DH	Write Data Hold Time		0	0	0	0	0	0	0		
RESET AND RETRANSMIT CYCLES											
t RSC	Reset Cycle Time		25	30	35	45	65	100	140	ns	Min
t RS	Reset Pulse Width	1	15	20	25	35	50	80	120		
t RSS	Reset Setup Time		15	20	25	35	50	80	120		
t RSR	Reset Recovery Time		10	10	10	10	15	20	20		
t RTC	Retransmit Cycle Time		25	30	35	45	65	100	140		
t RT	Retransmit Pulse Width	1	15	20	25	35	50	80	120		
t RTS	Retransmit Setup Time	2	15	20	25	35	50	80	120		
t RTR	Retransmit Recovery		10	10	10	10	15	20	20		

Notes: These timings are measured as defined in AC Test Conditions

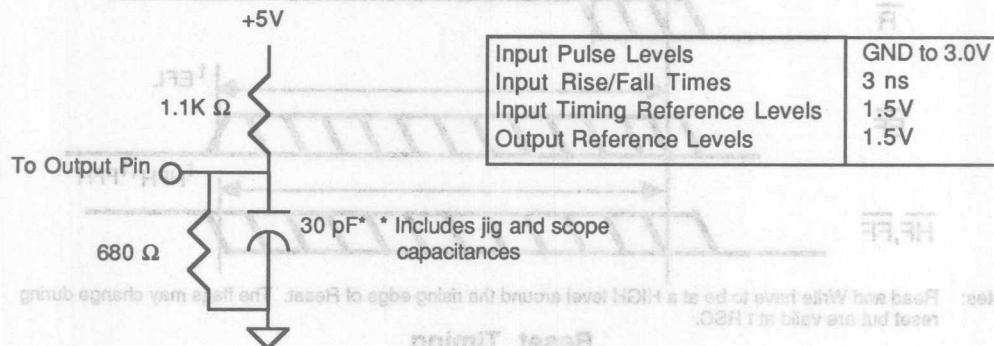
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. This applies to the read data flow-through mode only.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

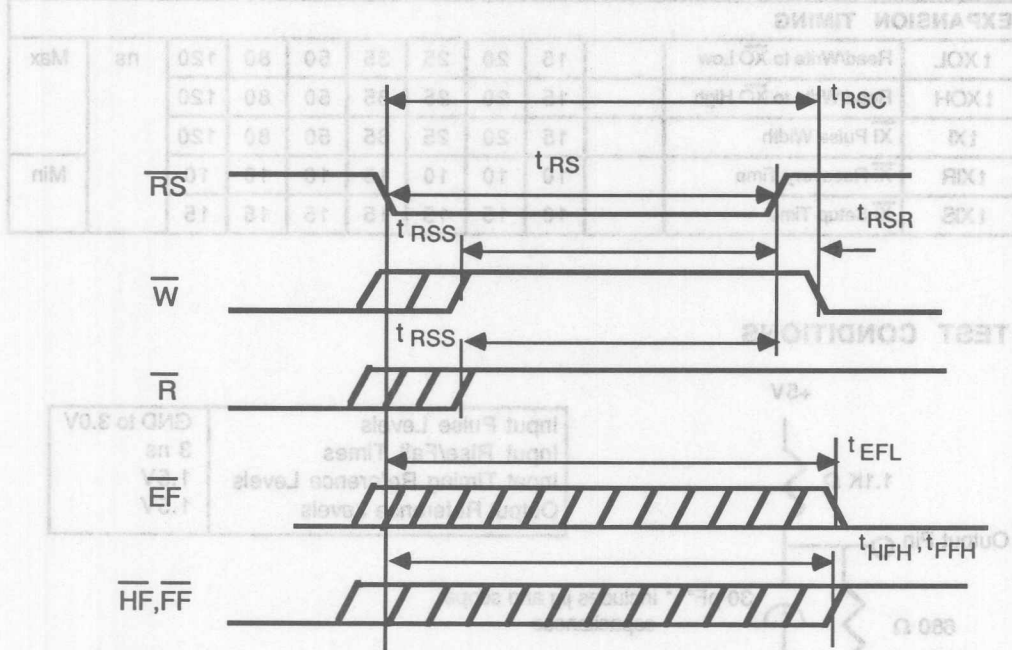
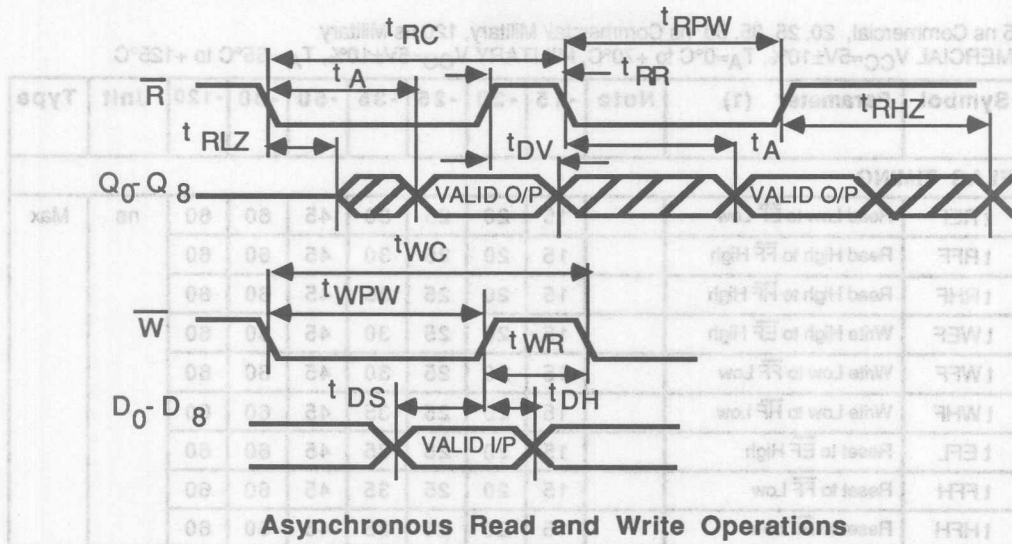
For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
 COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^{\circ}C$ to $+70^{\circ}C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
FLAG TIMING											
t REF	Read Low to EF Low		15	20	25	30	45	60	60	ns	Max
t RFF	Read High to FF High		15	20	25	30	45	60	60		
t RHF	Read High to HF High		15	20	25	35	45	60	60		
t WEF	Write High to EF High		15	20	25	30	45	60	60		
t WFF	Write Low to FF Low		15	20	25	30	45	60	60		
t WHF	Write Low to HF Low		15	20	25	35	45	60	60		
t EFL	Reset to EF High		15	20	25	35	45	60	60		
t FFH	Reset to FF Low		15	20	25	35	45	60	60		
t HFH	Reset to HF Low		15	20	25	35	45	60	60		
EXPANSION TIMING											
t XOL	Read/Write to XO Low		15	20	25	35	50	80	120	ns	Max
t XOH	Read/Write to XO High		15	20	25	35	50	80	120		
t XI	XI Pulse Width		15	20	25	35	50	80	120		
t XIR	XI Recovery Time		10	10	10	10	10	10	10		Min
t XIS	XI Setup Time		10	15	15	15	15	15	15		

AC TEST CONDITIONS

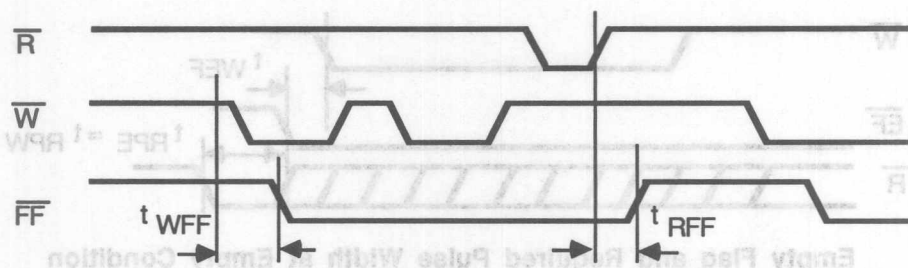


TIMING DIAGRAMS

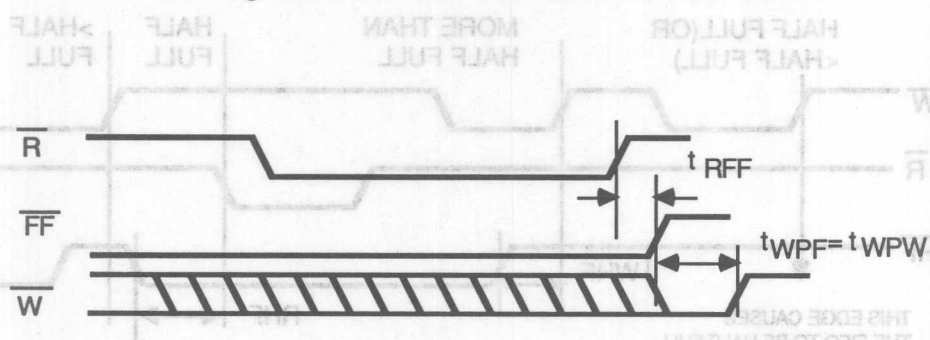


Notes: Read and Write have to be at a HIGH level around the rising edge of Reset. The flags may change during reset but are valid at tRSC.

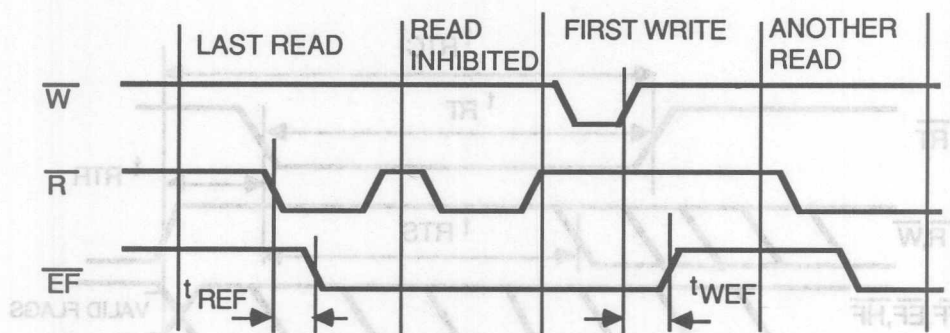
Reset Timing



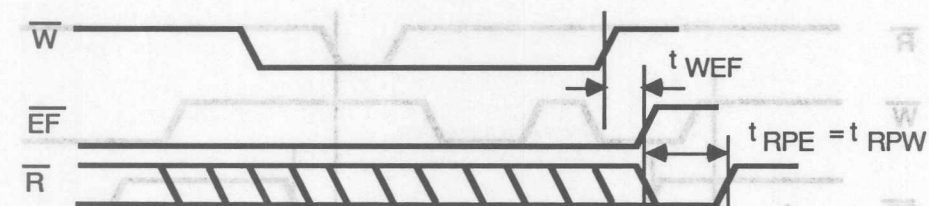
Full Flag Behavior from Last Write to First Read



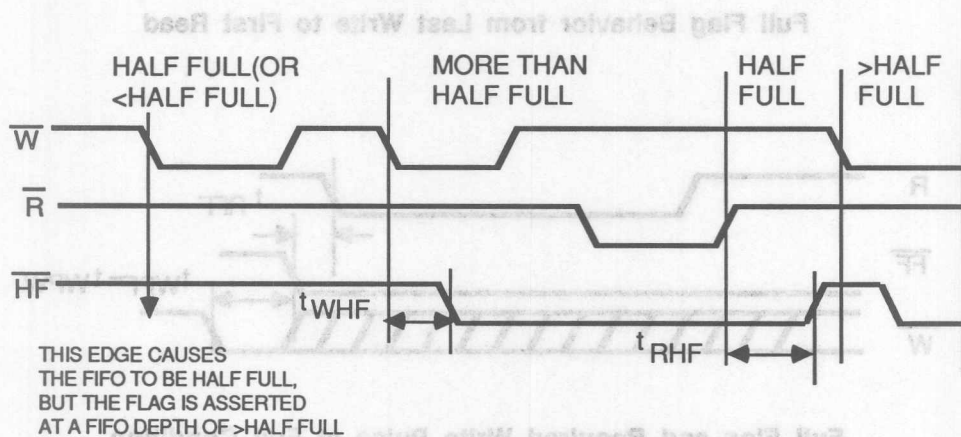
Full Flag and Required Write Pulse at Full Condition



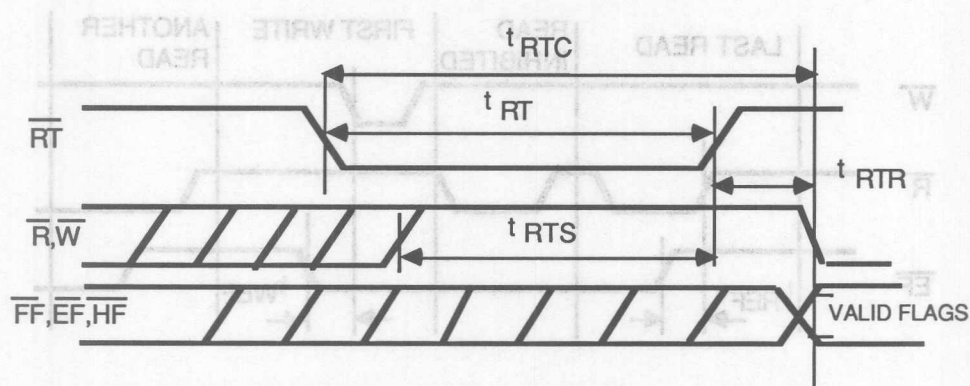
Empty Flag Behavior from Last Read to First Write



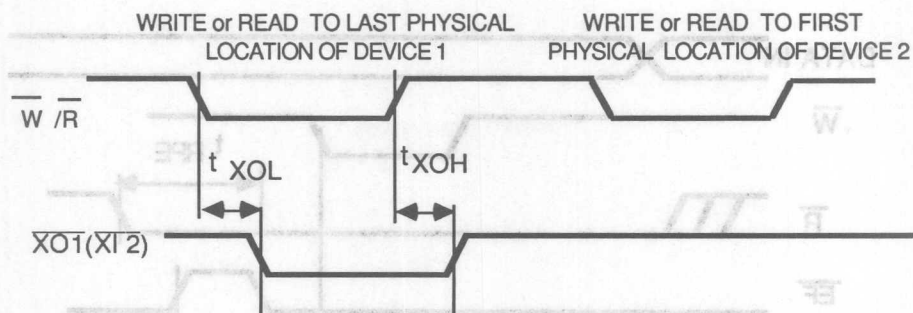
Empty Flag and Required Pulse Width at Empty Condition



Half Full Flag Timings

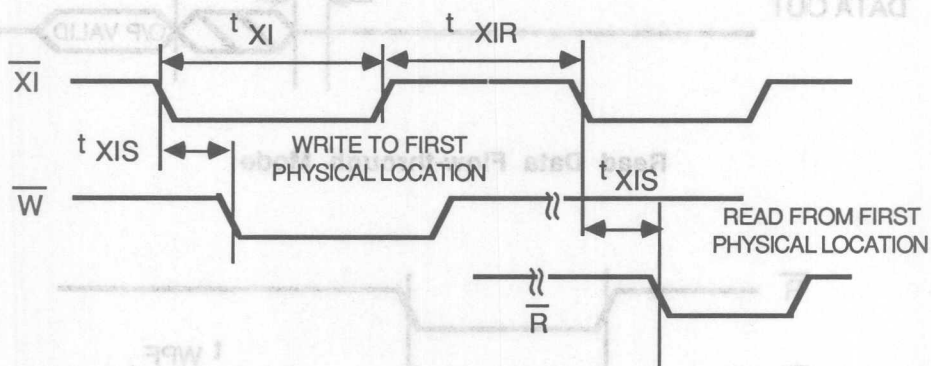


Retransmit Function Timing

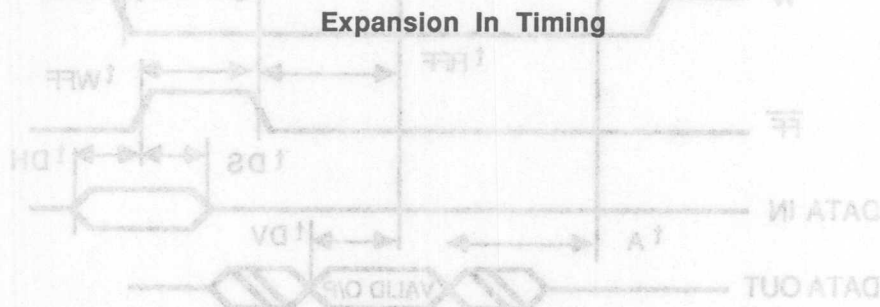


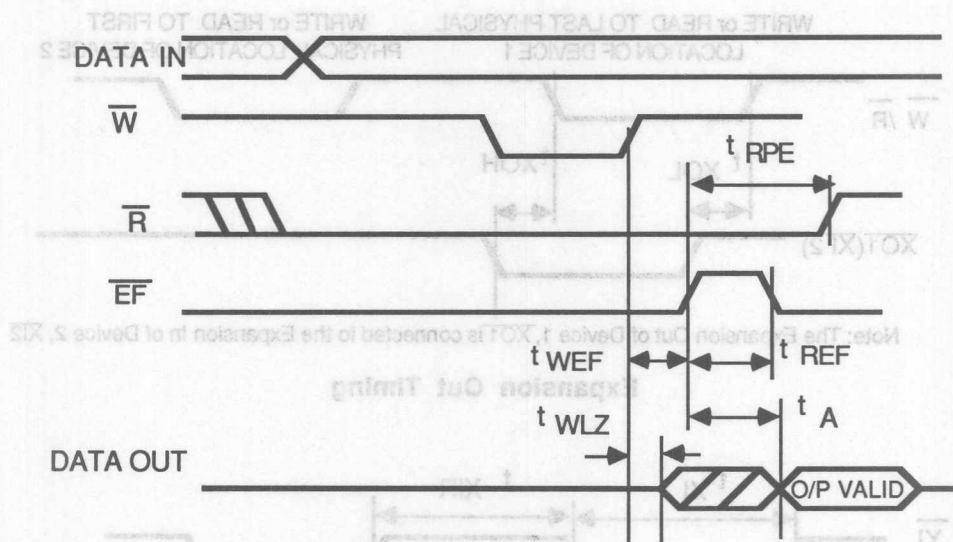
Note: The Expansion Out of Device 1, $\overline{XO1}$ is connected to the Expansion In of Device 2, $\overline{XI2}$

Expansion Out Timing

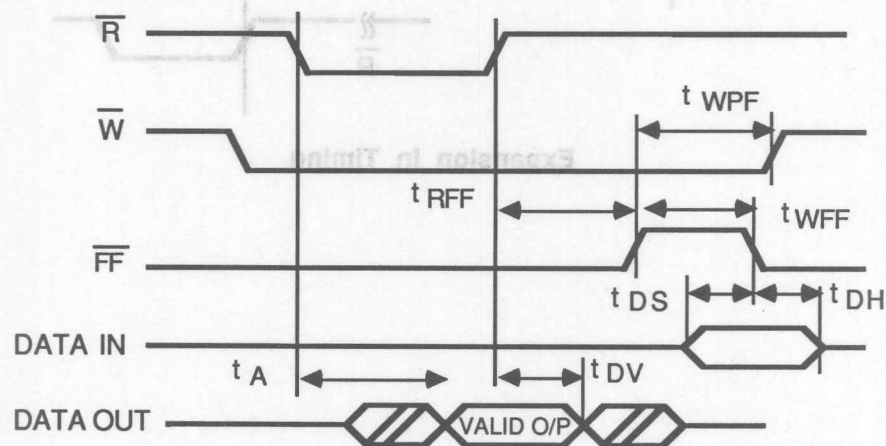


Expansion In Timing





Read Data Flow-through Mode



Write Data Flow-through Mode

OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS7201 through QS7204 are 512x9 through 4Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The Write line causes data to be written into the FIFO. The Read line causes data to be read from the FIFO. The Read line also activates the three-state outputs to present the read data. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Depth expansion pins are provided which allow these FIFOs to be expanded in depth without speed penalty. Retransmit capability is provided. Activating the Retransmit pin resets the read pointer to zero, and is useful for data communications and digital filtering applications.

SIGNAL DESCRIPTION

DATA INPUTS

D₀-D₈

The Data In lines D₀ to D₈ provide data to be written into the FIFO. Note: unused inputs must be tied to Vcc or Gnd.

CONTROL INPUTS

Reset ($\overline{RS}$)

The Reset input resets the Read and Write pointers and the flags to zero. The FIFO must be reset at power-up to insure proper operation of the pointers and flags. This is done by asserting the Reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag is asserted and the Full and Half Full flags to be deasserted. Read and Write lines must be HIGH for t_{RSS} before and t_{RSR} after the rising edge of the Reset signal for a valid reset operation.

Write ($\overline{W}$)

The Write line caused data to be written into the FIFO. A write cycle is initiated by the falling edge of the Write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the Write signal using the data set-up and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the Write signal asserts the Half full and Full flags when the next word after half full is written and when the last word has been written, respectively. The rising edge of the Write line deasserts the empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read ($\overline{R}$)

The Read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the Read signal. A read is performed if the empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write operations. After the Read control is deasserted the data outputs go from a valid state into high-impedance. The outputs remain in high-impedance until the next read cycle. When all the data is read on the last read cycle, the Empty flag is asserted, and will inhibit any subsequent reads. The outputs will be in high-impedance for subsequent read operation until a write occurs that deasserts the Empty flag, allowing a read cycle to begin. The outputs may also be in high impedance when the FIFOs are cascaded in depth. In this case, only the active FIFO asserts data, and the other FIFOs data outputs are in high-impedance. The falling edge of the read signal will set the Empty Flag during the read of the last word in the FIFO. The rising edge of the Read signal will deassert the Half Full and the Full flags when the FIFO has reached half full and when the FIFO was full, respectively.

First Load/ Retransmit (FL/RT)

This is a dual purpose input. In the depth expansion mode, this pin indicates the first FIFO device that will be loaded or read from after a reset operation. In the standalone or width expansion mode (when the expansion input is grounded) this pin initiates the a retransmit function.

Retransmit resets the read pointer to zero. The Read and Write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing retransmit pin will cause the read pointer to be reset to zero and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

Expansion In (XI)

This is a dual purpose pin. When it is grounded then it indicates that the FIFO is a standalone device. When it is not grounded, it indicates that the FIFO is in the depth expansion mode. In the depth expansion mode this pin is connected to the X $\bar{O}$ pin of the previous device.

DATA OUTPUTS

Data Outputs Q $_0$ -Q $_8$

The 9-bit data output bus, Q $_0$ -Q $_8$ receives the read data from the FIFO. It is active whenever the Read signal is low. It is in a high impedance state when the Read signal is high. It is also in high impedance when the FIFO Empty flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag (FF)

The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag (EF)

The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the write signal deasserts the flag, as one word is now present in the FIFO.

Expansion Out/Half Full flag (X $\bar{O}$ /HF)

This is a dual purpose flag. In the single device mode, the Expansion In is grounded and the Half Full flag output is present on this pin. Whenever the FIFO is more than half full the flag remains asserted. When the FIFO is exactly half full and the next falling edge of the Write signal asserts the flag. The rising edge of read that causes the FIFO to be half full, will deassert the half full flag. It will remain asserted until the FIFO is half full or less than half full. The name given to the flag is half full, but it is asserted on the one plus the half full condition.

In the depth expansion mode, the Expansion Out is connected to the Expansion In of the next device. This causes the next device to perform write or read operations.

OPERATING MODES

SINGLE DEVICE MODE

A FIFO is in standalone mode when the Expansion In control is grounded. In this mode the half full flag is available on the shared $\overline{XO}/HF$ line. Figure 1 shows the standalone mode and this applies to FIFO width expansion, as shown in figure 2.

DEPTH EXPANSION MODE

A FIFO is in the depth expansion mode when the Expansion In control is not grounded but tied to the Expansion Out pin of the previous FIFO. Using the depth expansion mode, the 7201/02 can be easily cascaded to create FIFOs of larger depth. The devices are cascaded as shown in figure 3. In the depth expansion mode, the device that receives the first word of data has its First Load input grounded. The other devices have their First Load inputs in the high state. Two 4-input OR gates are required to create the composite Full and Empty flags for the FIFO array. In using the depth expansion mode, care must be taken to keep the traces short between the Expansion In of one device to the Expansion Out of the next device to minimize crosstalk noise.

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a read flow-through and a write flow-through, are supported by the FIFO. In the read flow-through mode the FIFO is empty, and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its Read line held low, and a write occurs. This rising edge of the Write would deassert the Empty flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The Read line being low would cause the data to be read and also assert the empty flag once again. The user must raise the Read line in order to increment the read pointer.

In the write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A write flow-through operation permits the writing of a single word of data immediately after reading one word of data from a full FIFO. This is similar to the read flow-through case, and the Write line must toggled to increment the write pointer.

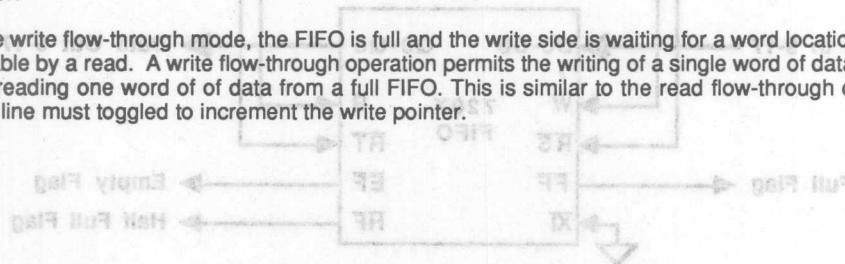


Figure 2. A 18-bit wide FIFO using 2 FIFOs

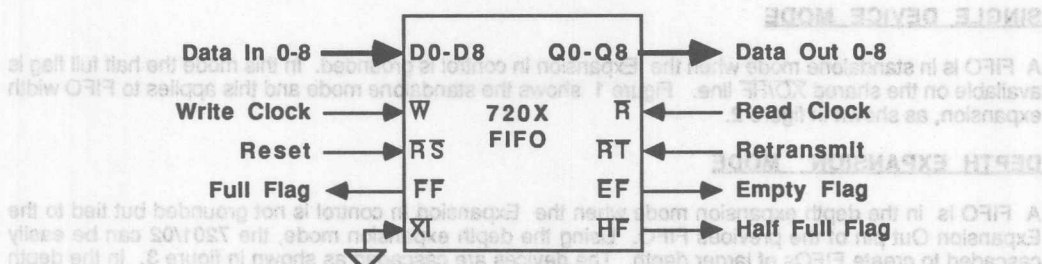


Figure 1. The FIFO in a Standalone Mode.

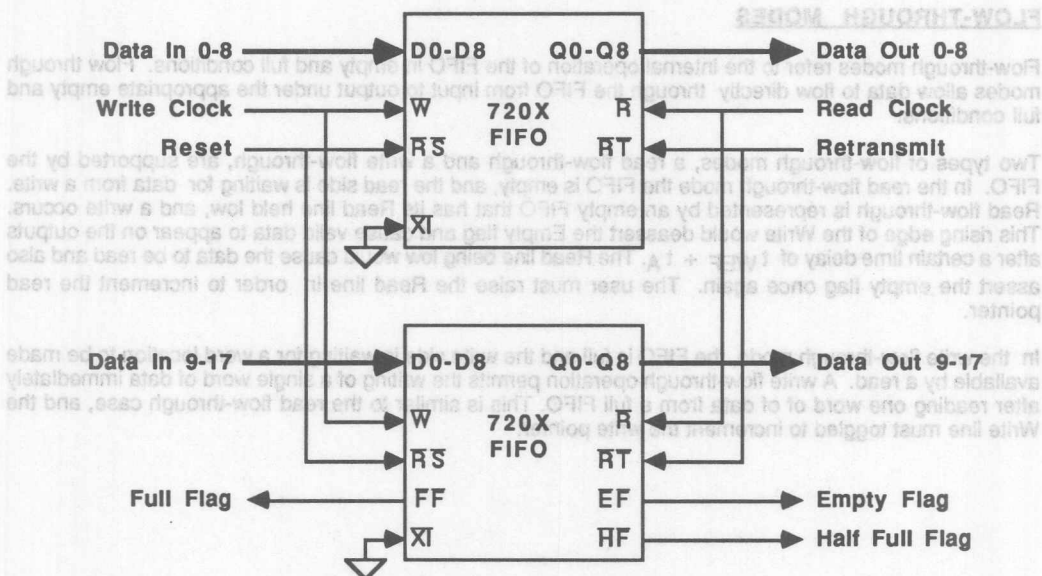
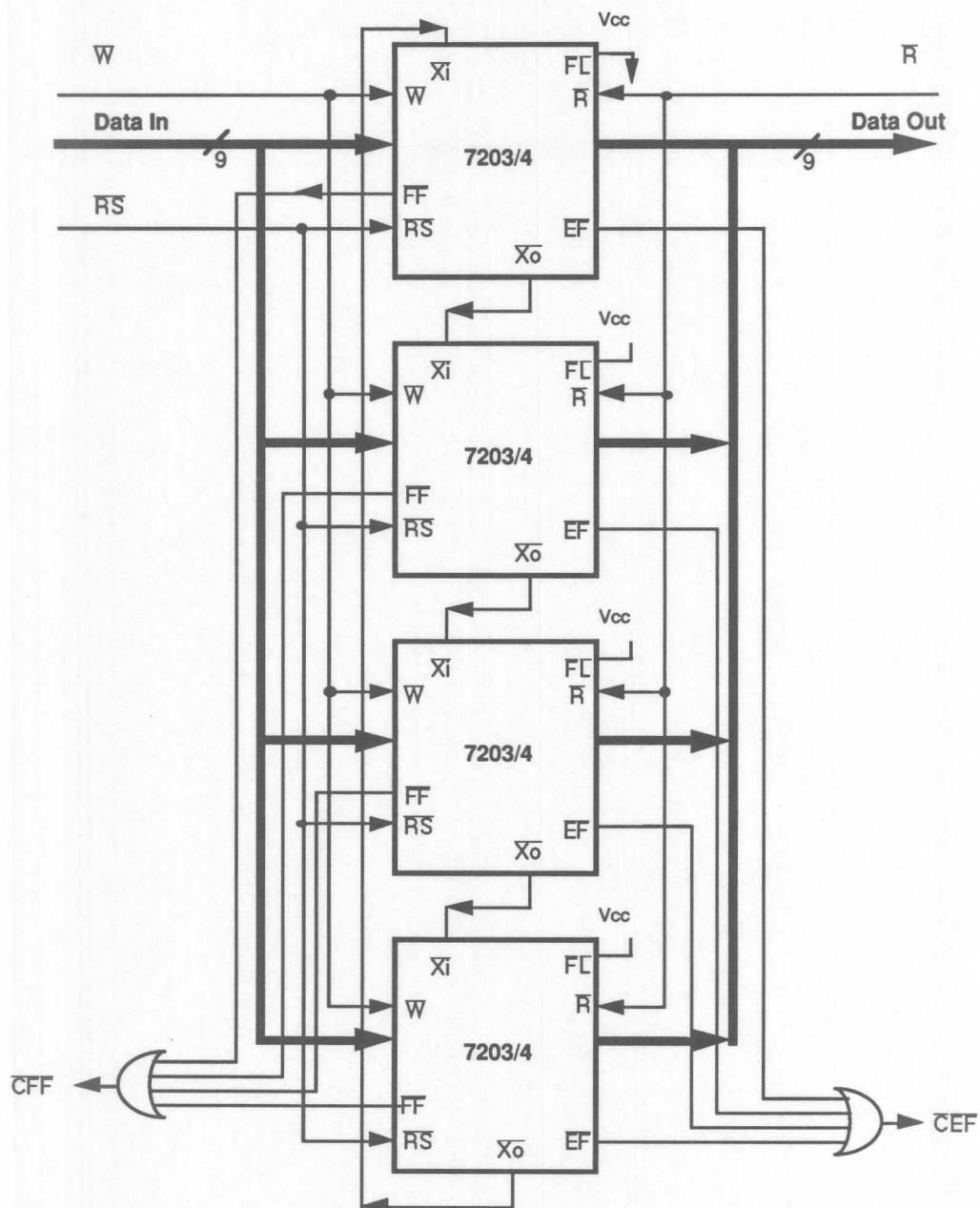


Figure 2. A 18-bit wide FIFO using 2 FIFOs



3

Note that the composite Empty Flag and Full flag requires the OR-ing of the individual Empty and Full flags, respectively.

Figure 3. Building a 4N-deep FIFO using Four N-deep FIFOs

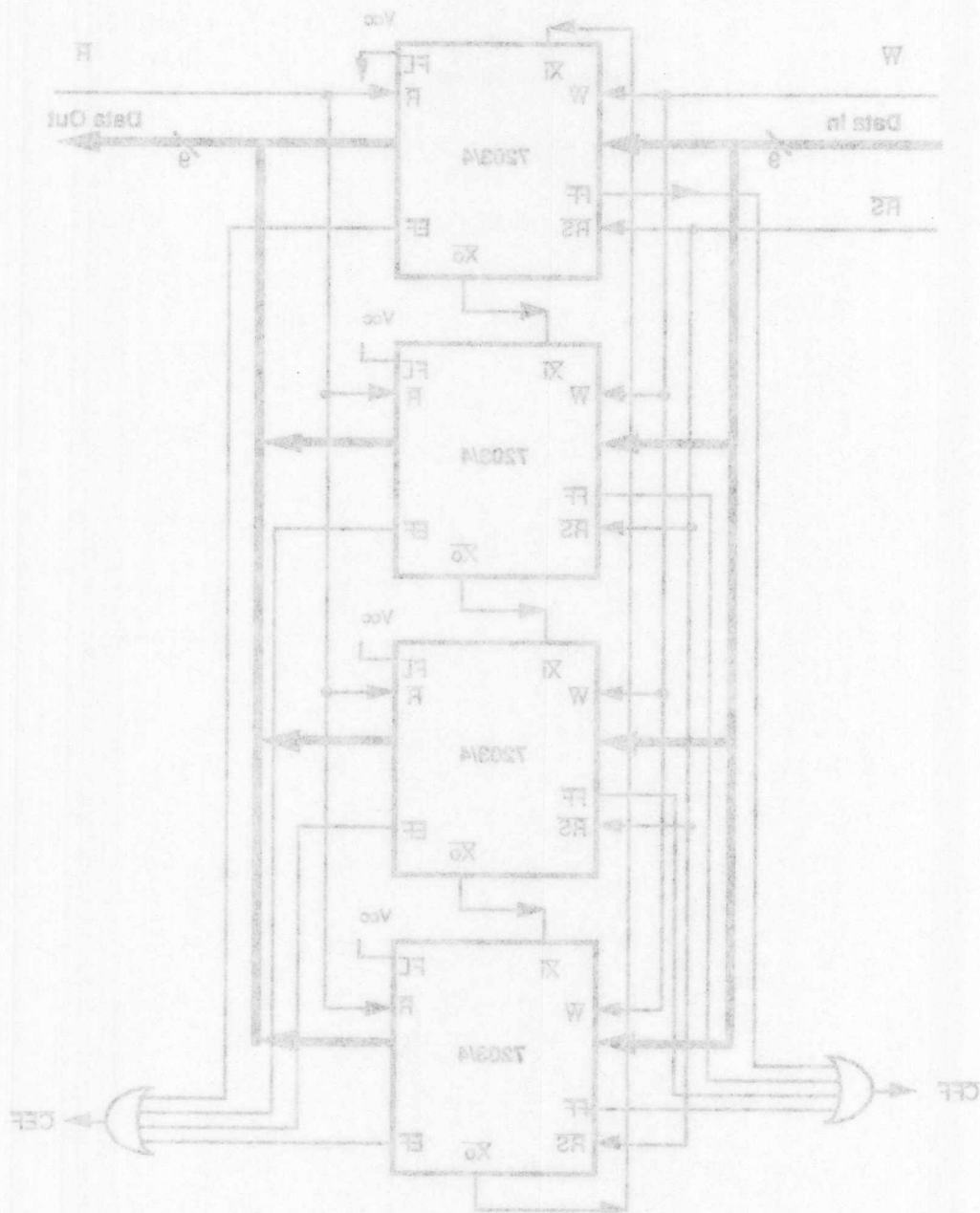


Figure 3. Building a 4N-deep FIFO using Four 7203A chips. Note that the composite Empty Flag and Full Flag requires the OR-ing of the individual Empty and Full flags, respectively.

Q

High Speed CMOS 9-bit FIFO with Output Enable

512x9: QS7211
1Kx9: QS7212

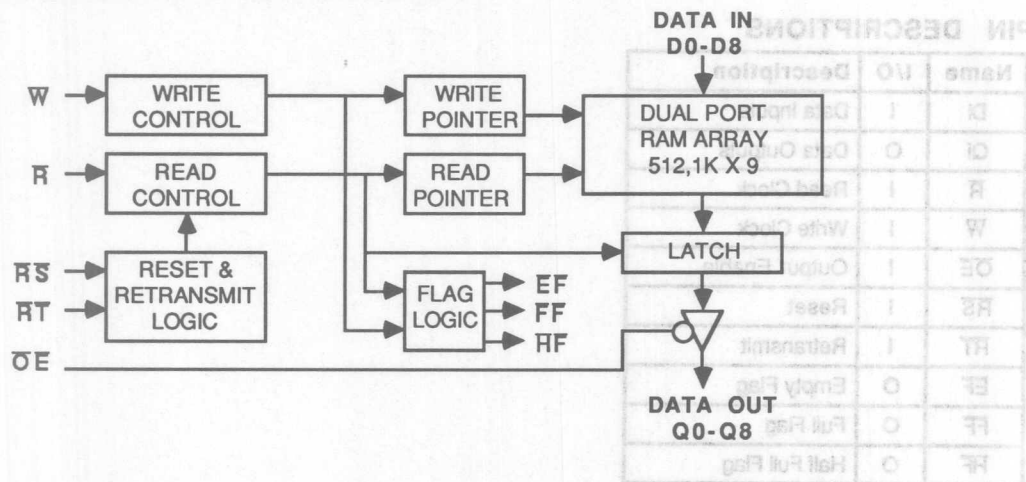
FEATURES/BENEFITS

- 15 ns flag and data access times
- Separate Output Enable and Read Clock
- Fully Asynchronous Read and Write
- Zero fall-through time
- Dual Port RAM-based cell using 6T technology
- 40 MHz cycle time
- Output latch holds data while Read Clock high
- TTL input and output level compatible
- Available in 28-pin 300 mil PDIP, SOIC, and SOJ

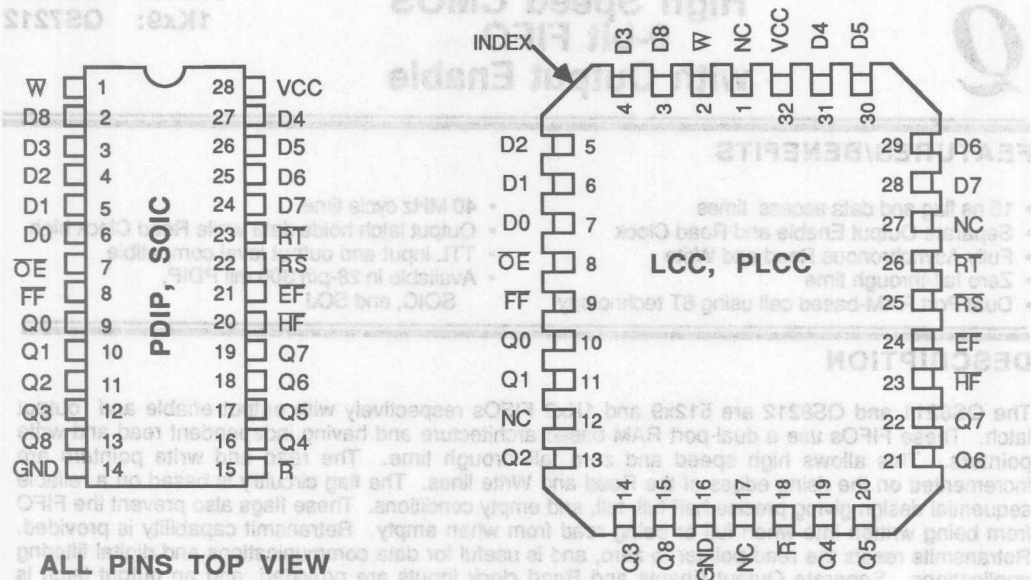
DESCRIPTION

The QS8211 and QS8212 are 512x9 and 1Kx9 FIFOs respectively with output enable and output latch. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Retransmit capability is provided. Retransmits resets the read pointer to zero, and is useful for data communications and digital filtering applications. Separate Output Enable and Read clock inputs are provided, and an output latch is provided to hold data when the read clock is high, allowing these FIFOs to be used in bus applications.

FUNCTIONAL BLOCK DIAGRAM



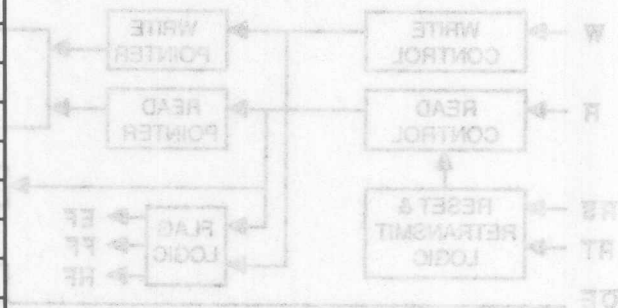
PINOUTS



ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
R	I	Read Clock
W	I	Write Clock
OE	I	Output Enable
RS	I	Reset
RT	I	Retransmit
EF	O	Empty Flag
FF	O	Full Flag
HF	O	Half Full Flag



FUNCTION TABLE

Mode	Inputs					Internal Status			Outputs			
	RS	RT	W	R	OE	Read Pointer	Write Pointer	Read Latch	EF	HF	FF	QI
Reset	L	X	H	H	X	Location Zero	Location Zero	X	L	H	H	X
Re-transmit	H	L	X	H	X	Location Zero	-	X	(3)	(3)	(3)	X
Write	H	H	↑	H	X	-	Increment (2)	Q(i)	(3)	(3)	(3)	X
Read	H	H	H	↓	L	Increment (1)	-	Q(i)	(3)	(3)	(3)	Q(i)
Hold	H	H	H	H	L	Q(i+1)	-	Q(i)	(3)	(3)	(3)	Q(i)
Next Data	H	H	H	L	L	Q(i+2)	-	Q(i+1)	(3)	(3)	(3)	Q(i+1)
Disable	H	H	H	L	H	-	-	Q(i)	(3)	(3)	(3)	Hi-Z

3

Notes:

- (1) The Read Pointer will increment if the FIFO is not empty.
- (2) The Write flag will increment if the FIFO is not full.
- (3) The flags will reflect the relative locations of the read and write pointers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Input Diode Current with $V_I > V_{CC}$	20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Diode Current with $V_O > V_{CC}$	50 mA
DC Output Current Max. sink current/pin.....	70 mA
DC Output Current Max. source current/pin.....	30 mA
Total DC Ground Current.....	$(N \times I_{OL} + M \times I_{CC})$ mA
Total DC VCC Power Supply Current.....	$(N \times I_{OH} + M \times I_{CC})$ mA
N=Number of Outputs, M=Number of Inputs	
Maximum Power Dissipation.....	0.5 watts
TSTG Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	$V_{in} = 0\text{ V}$	5	8	pF
Cout	Output Capacitance	$V_{out} = 0\text{ V}$	5	8	pF

Note: Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -2 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Iii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		1		10	μA
Ilo	Output Leakage	Vcc = MAX, Vout = GND to Vcc		10		10	

Notes:

1. Transient inputs with Vil not more negative than -1.5 volts are permitted for pulse widths ≤ 10 ns

POWER SUPPLY CHARACTERISTICS

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 $V_{IC} = 0.2$ Volts, $V_{HC} = V_{CC} - 0.2$ Volts

Symbol	Parameter	≤ 35		≥ 50		Unit
		C	M	C	M	
Icc1	Operating Operating Current Vcc = MAX, Outputs open	100	120	100	120	mA
Icc2	Standby Current $R = W = RS = FL/RT = V_{IH}$	15	20	8	15	
I _{sb}	Power Down Current All Inputs at V _{HC} or V _{IC} $R = W = RS = FL/RT = V_{HC}$	5	9	5	9	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^\circ C$ to $+70^\circ C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^\circ C$ to $+125^\circ C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	Unit	Type
READ CYCLE								
f RF	Read Frequency, mHz	2	40	33	28	22	mHz	Min
t RC	Read Cycle Time		25	30	35	45	ns	Max
t A	Read Access Time		15	20	25	35		
t RR	Read Recovery Time		10	10	10	10		
t RPW	Read Pulse Width	1	15	20	25	35		Min
t OE	$\overline{OE}$ to Data Low Z	2	3	3	3	3		
			6	6.5	7	8		
t OZ	$\overline{OE}$ to Data High Z	2	3	3	3	3	Min	
			14	18	18	20	Max	
WRITE CYCLE								
f WF	Write Frequency, mHz	2	40	33	28	22	mHz	Min
t WC	Write Cycle Time		25	30	35	45	ns	
t WPW	Write Pulse Width	1	15	20	25	35		
t WR	Write Recovery Time		10	10	10	10		
t DS	Write Data Setup Time		8	12	15	18		
t DH	Write Data Hold Time		0	0	0	0		
RESET CYCLE								
t RSC	Reset Cycle Time		25	30	35	45	ns	Min
t RS	Reset Pulse Width	1	15	20	25	35		
t RSS	Reset Setup Time		15	20	25	35		
t RSR	Reset Recovery Time		10	10	10	10		
t RTC	Retransmit Cycle Time		25	30	35	45		
t RT	Retransmit Pulse Width	1	15	20	25	35		
t RTS	Retransmit Setup Time	2	15	20	25	35		
t RTR	Retransmit Recovery		10	10	10	10		

Notes: These timings are measured as defined in AC Test Conditions

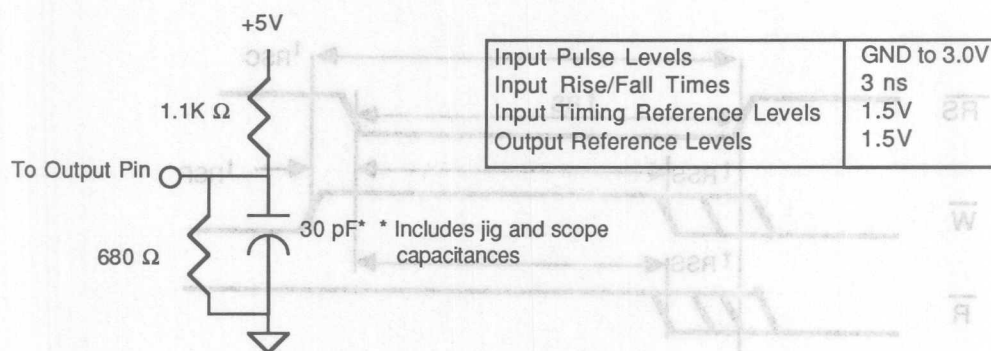
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. This applies to the read data flow-through mode only.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

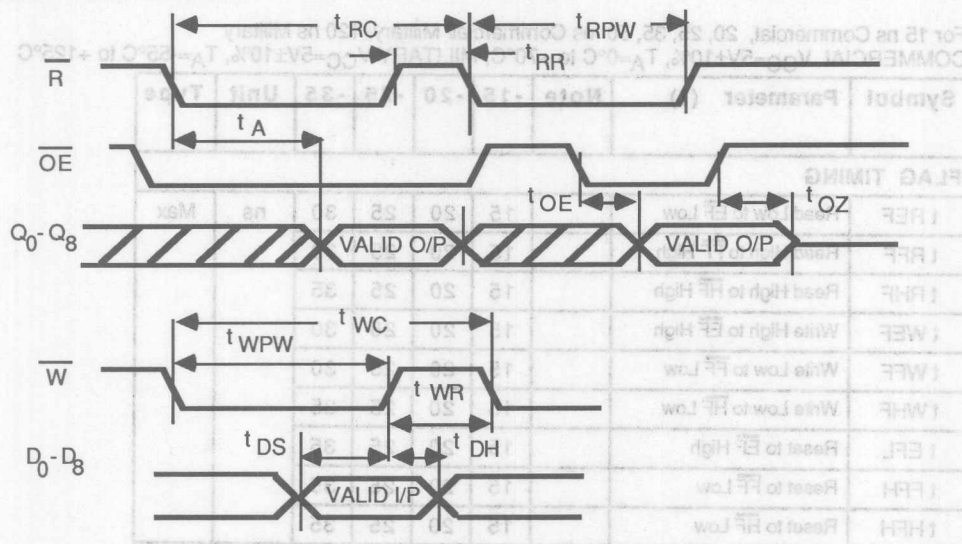
For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
 COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^{\circ}C$ to $+70^{\circ}C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter (1)	Note	-15	-20	-25	-35	Unit	Type
FLAG TIMING								
t_{REF}	Read Low to $\overline{EF}$ Low		15	20	25	30	ns	Max
t_{RFF}	Read High to $\overline{FF}$ High		15	20	25	30		
t_{RHF}	Read High to $\overline{HF}$ High		15	20	25	35		
t_{WEF}	Write High to $\overline{EF}$ High		15	20	25	30		
t_{WFF}	Write Low to $\overline{FF}$ Low		15	20	25	30		
t_{WHF}	Write Low to $\overline{HF}$ Low		15	20	25	35		
t_{EFL}	Reset to $\overline{EF}$ High		15	20	25	35		
t_{FFH}	Reset to $\overline{FF}$ Low		15	20	25	35		
t_{HFH}	Reset to $\overline{HF}$ Low		15	20	25	35		

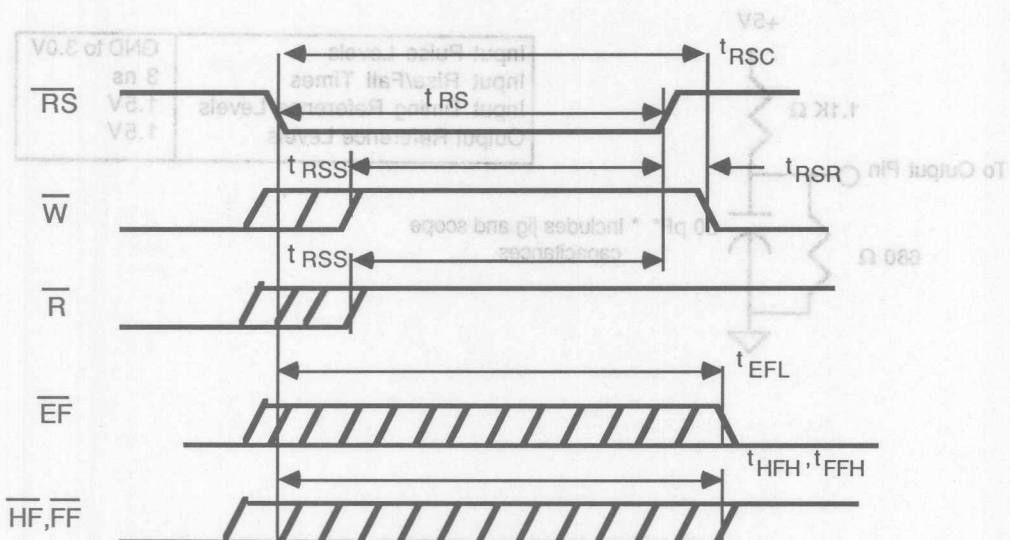
AC TEST CONDITIONS



TIMING DIAGRAMS

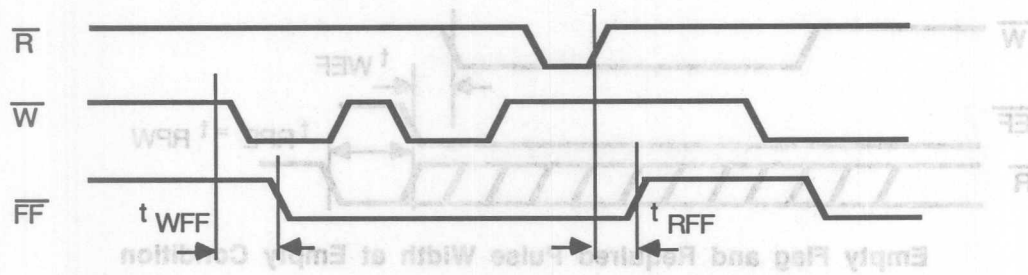


Asynchronous Read and Write Operations

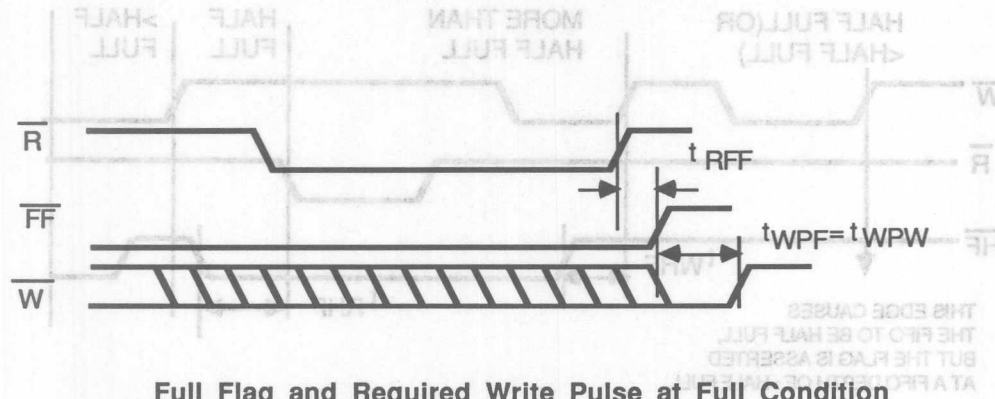


Notes: Read and Write have to be at a HIGH level around the rising edge of Reset. The flags may change during reset but are valid at t_{RSC} .

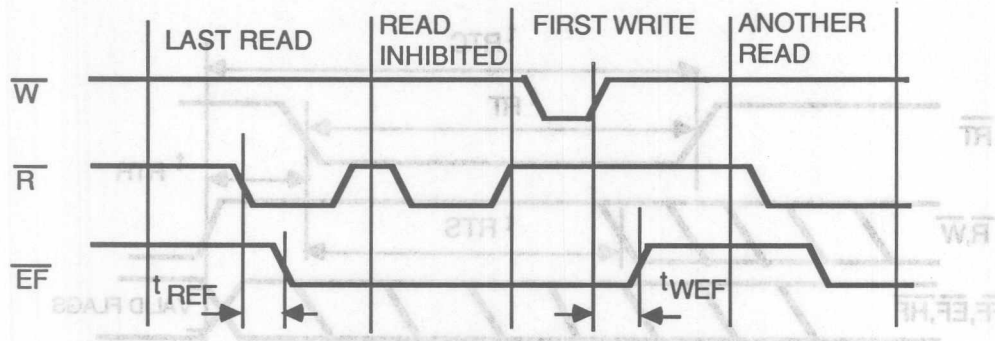
Reset Timing



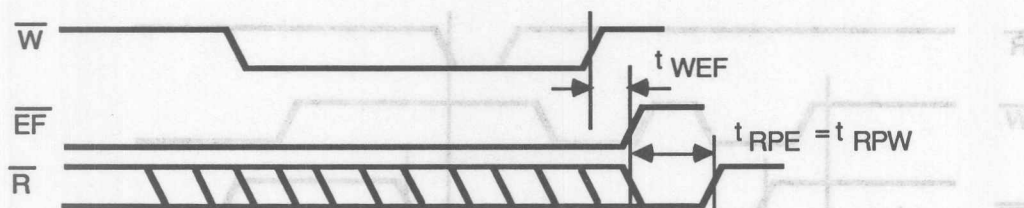
Full Flag Behavior from Last Write to First Read



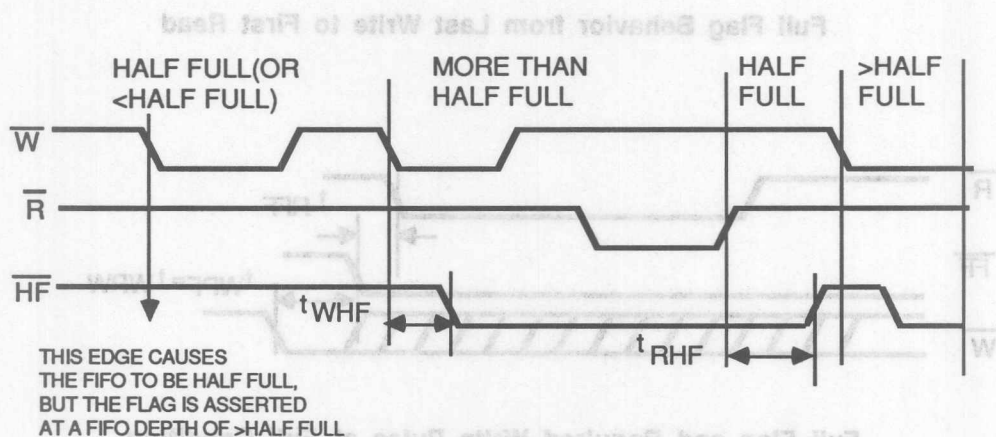
Full Flag and Required Write Pulse at Full Condition



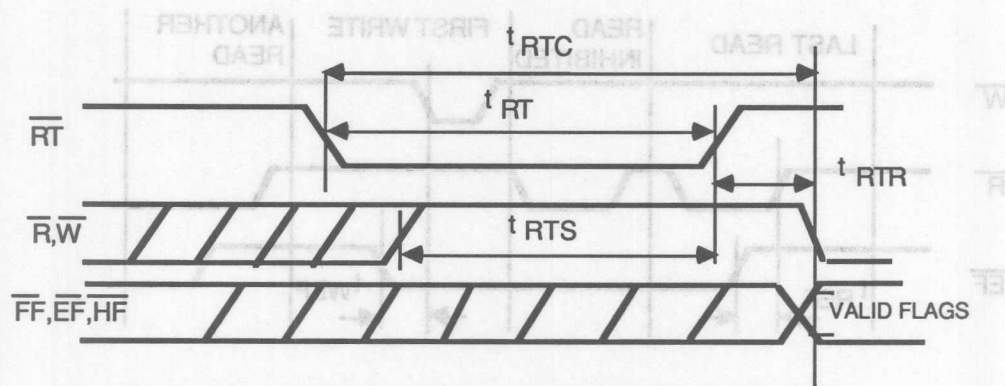
Empty Flag Behavior from Last Read to First Write



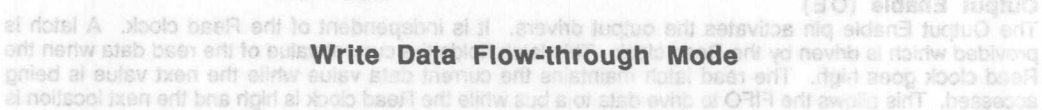
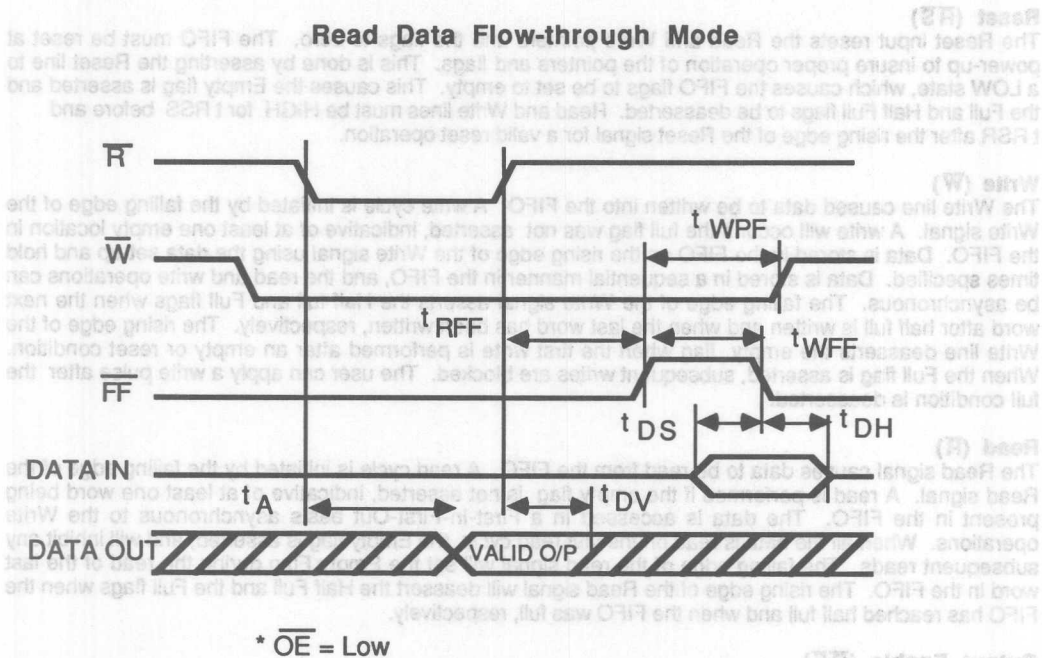
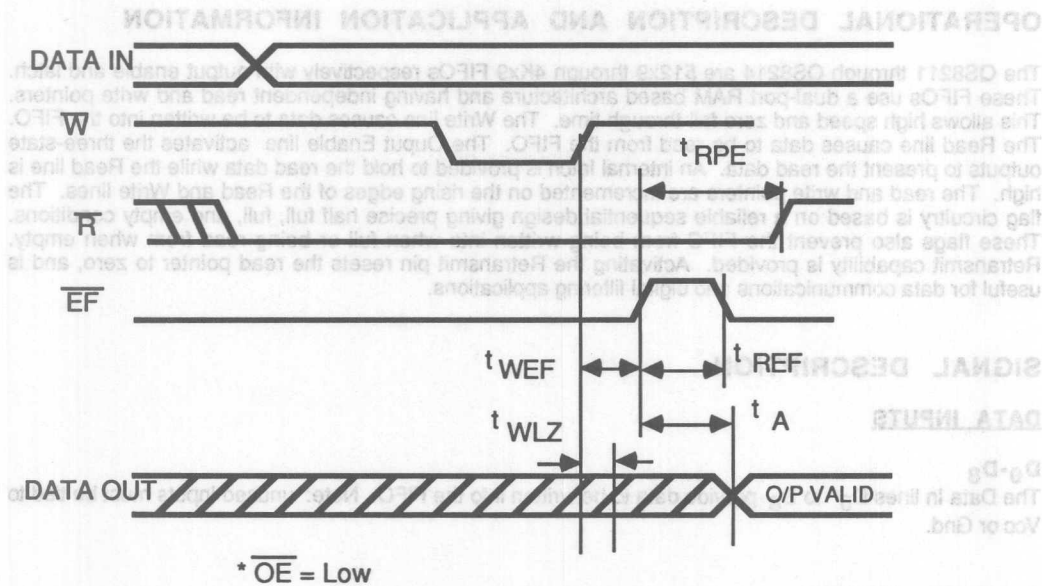
Empty Flag and Required Pulse Width at Empty Condition



Half Full Flag Timings



Retransmit Function Timing



OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS8211 through QS8214 are 512x9 through 4Kx9 FIFOs respectively with output enable and latch. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The Write line causes data to be written into the FIFO. The Read line causes data to be read from the FIFO. The Output Enable line activates the three-state outputs to present the read data. An internal latch is provided to hold the read data while the Read line is high. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Retransmit capability is provided. Activating the Retransmit pin resets the read pointer to zero, and is useful for data communications and digital filtering applications.

SIGNAL DESCRIPTION

DATA INPUTS

D₀-D₈

The Data In lines D₀ to D₈ provide data to be written into the FIFO. Note: unused inputs must be tied to Vcc or Gnd.

CONTROL INPUTS

Reset (R̄S)

The Reset input resets the Read and Write pointers and the flags to zero. The FIFO must be reset at power-up to insure proper operation of the pointers and flags. This is done by asserting the Reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag is asserted and the Full and Half Full flags to be deasserted. Read and Write lines must be HIGH for t_{RSS} before and t_{RSR} after the rising edge of the Reset signal for a valid reset operation.

Write (W)

The Write line caused data to be written into the FIFO. A write cycle is initiated by the falling edge of the Write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the Write signal using the data set-up and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the Write signal asserts the Half full and Full flags when the next word after half full is written and when the last word has been written, respectively. The rising edge of the Write line deasserts the empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read (R)

The Read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the Read signal. A read is performed if the empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write operations. When all the data is read on the last read cycle, the Empty flag is asserted, and will inhibit any subsequent reads. The falling edge of the read signal will set the Empty Flag during the read of the last word in the FIFO. The rising edge of the Read signal will deassert the Half Full and the Full flags when the FIFO has reached half full and when the FIFO was full, respectively.

Output Enable (OE)

The Output Enable pin activates the output drivers. It is independent of the Read clock. A latch is provided which is driven by the Read clock. This latch holds the current value of the read data when the Read clock goes high. The read latch maintains the current data value while the next value is being accessed. This allows the FIFO to drive data to a bus while the Read clock is high and the next location is

being accessed. If the read clock high time is greater than the read cycle time, the outputs will change only on the falling edge of the Read clock.

Retransmit (RT)

This pin initiates the a retransmit function. Retransmit resets the read pointer to zero. The Read and Write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing retransmit pin will cause the read pointer to be reset to zero and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

DATA OUTPUTS

Data Outputs Q₀-Q₈

The 9-bit data output bus, Q₀-Q₈ receives the read data from the FIFO. It is active whenever the Read signal is low. It is in a high impedance state when the Read signal is high. It is also in high impedance when the FIFO Empty flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag (FF)

The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag (EF)

The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the write signal deasserts the flag, as one word is now present in the FIFO.

Half Full flag (HF)

Whenever the FIFO is more than half full the Half Full flag remains asserted. When the FIFO is exactly half full, the next falling edge of the Write signal asserts the flag. The rising edge of read that causes the FIFO to be half full, will deassert the half full flag. It will remain asserted until the FIFO is half full or less than half full. The name given to the flag is half full, but it is asserted on the one plus the half full condition.

OPERATING MODES

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a read flow-through and a write flow-through, are supported by the FIFO. In the read flow-through mode the FIFO is empty, and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its Read line held low, and a write occurs. This rising edge of the Write would deassert the Empty flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The Read line being low would cause the data to be read and also assert the empty flag once again. The user must raise the Read line in order to increment the read pointer.

In the write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A write flow-through operation permits the writing of a single word of data immediately after reading one word of data from a full FIFO. This is similar to the read flow-through case, and the Write line must be toggled to increment the write pointer.

Full Flag (FF)
The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag (EF)
The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the Write signal deasserts the flag, as one word is now present in the FIFO.

Half Full Flag (HFF)
Whenever the FIFO is more than half full the Half Full flag remains asserted. When the FIFO is exactly half full, the next falling edge of the Write signal asserts the flag. The rising edge of the Read signal causes the FIFO to be half full, but it is asserted on the one plus the half full condition. The name given to the flag is half full, but it is asserted on the one plus the half full condition.



High Speed CMOS 9-bit Clocked FIFO

2Kx9: QS7223

4Kx9: QS7224

ADVANCE
INFORMATION

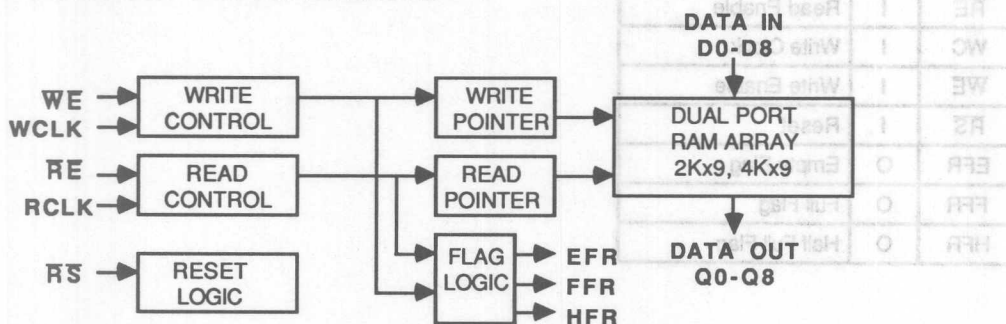
FEATURES/BENEFITS

- Clocked interface FIFOs for high speed systems
- Data and flags change on rising edge of clocks
- Fully Asynchronous Read and Write
- TTL input and output level compatible
- Dual Port RAM-based cell using 6T technology
- 40 MHz cycle time with symmetrical clocks
- Depth expansion without additional logic or pins
- Register-like: outputs show current word in FIFO
- Available in 28-pin 300 mil PDIP, SOIC, and SOJ

DESCRIPTION

The QS7223 and QS7224 are 2Kx9 and 4Kx9 FIFOs respectively with clocked interfaces for both read and write. These interfaces provide high speed data buffering in system designs and allow symmetrical clocks at speeds to 40 MHz. Free running independent read and write clocks are controlled by read and write enable lines. All signals are relative to the rising edges of the clocks. Write enable and write data are accepted at the rising edge and the full flag and the half full flag change after the rising edge of the write clock. Read enable is accepted at the rising edge and read data and the full flag changes after the rising edge of the read clock. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. The read and write pointers are set to zero by the reset pulse. A Write Enable causes data to be written and the write pointer to be incremented by the rising edge of the write clock. If the FIFO was empty, the write data will be present at the read outputs, and the empty flag will be cleared at the next rising edge of the read clock. A Read Enable will cause the read pointer to be incremented to the next word on the rising edge of the read clock. If there was only one word in the FIFO, the empty flag will be set by this same rising edge. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty.

FUNCTIONAL BLOCK DIAGRAM



PINOUTS

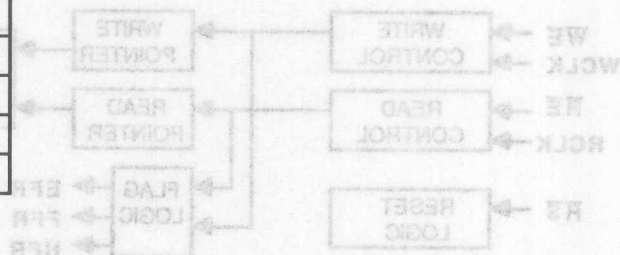
WC	1	28	VCC
D8	2	27	D4
D3	3	26	D5
D2	4	25	D6
D1	5	24	D7
D0	6	23	WE
RE	7	22	RS
FFR	8	21	EFR
Q0	9	20	HFR
Q1	10	19	Q7
Q2	11	18	Q6
Q3	12	17	Q5
Q8	13	16	Q4
GND	14	15	RC

PDIP, SOIC

ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
RC	I	Read Clock
RE	I	Read Enable
WC	I	Write Clock
WE	I	Write Enable
RS	I	Reset
EFR	O	Empty Flag
FFR	O	Full Flag
HFR	O	Half Full Flag



FUNCTION TABLE

MODE	Inputs					Internal Status		Outputs (After Clock)			
	RS	WE	WC	RE	RC	Write Pointer	Read Pointer	EFR	FFR	HFR	QI
Read/Write Controls											
Reset	L	X	X	X	X	0000	0000	H	L	L	Q(0)
Write	H	L	↑	X	X	YY+1	XX	(3)	(3)	(3)	Q(XX)
Read	H	X	X	L	↑	YY	XX+1	(3)	(3)	(3)	Q(XX+1)
Hold	H	H	↑	H	↑	YY	XX	(3)	(3)	(3)	Q(XX)
Read/Write at Empty											
Reset	L	X	X	X	X	0000	0000	H	L	L	Q(0)
1st Write	H	L	↑	H	X	0001	0000	L	L	L	Q(0)
2nd Write	H	L	↑	H	X	0002	0000	L	L	L	Q(0)
1st Read	H	H	X	L	↑	0002	0001	L	L	L	Q(1)
2nd Read	H	H	X	L	↑	0002	0002	H	L	L	Q(2)
Read/Write at Full											
Last Write	H	L	↑	H	X	1000	0000	L	H	H	Q(0)
1st Read @ Full	H	H	X	L	↑	1000	0001	L	L	H	Q(1)
Read/Write at Half Full											
2048th Write	H	L	↑	X	X	0800	0000	L	L	L	Q(0)
2048th+1 Write	H	L	↑	X	X	0801	0000	L	L	H	Q(0)
1st Read @ HF	H	H	X	L	↑	0801	0001	L	L	L	Q(1)

Notes:

- (1) The Read Pointer will increment if the FIFO is not empty.
- (2) The Write flag will increment if the FIFO is not full.
- (3) The flags will reflect the relative locations of the read and write pointers.

ABSOLUTE MAXIMUM RATINGS

FUNCTION TABLE

Supply Voltage to Ground.....-0.5V to +7.0V
 DC Output Voltage V_O -0.5V to $V_{CC} + 0.5V$
 DC Input Voltage V_I -0.5V to $V_{CC} + 0.5V$
 AC Input Voltage (for pulse width ≤ 20 ns).....-3.0V
 DC Input Diode Current with $V_I < 0$-20 mA
 DC Input Diode Current with $V_I > V_{CC}$20 mA
 DC Output Diode Current with $V_O < 0$-50 mA
 DC Output Diode Current with $V_O > V_{CC}$50 mA
 DC Output Current Max. sink current/pin.....70 mA
 DC Output Current Max. source current/pin.....30 mA
 Total DC Ground Current.....(NxIOL + MxΔI CC) mA
 Total DC VCC Power Supply Current.....(NxIOH + MxΔI CC) mA
 N=Number of Outputs, M=Number of inputs
 Maximum Power Dissipation.....0.5 watts
 TSTG Storage Temperature.....-65° to +165°C

CAPACITANCE

Ta = 25 °C, f = 1 mHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V	5	8	pF

Note: Capacitance is guaranteed but not tested

1st Read @ HF	H	H	X	L	↑	0801	0001	L	L	L	Q(1)
2048th White	H	L	↑	X	X	0800	0000	L	L	L	Q(0)
2048th+1 White	H	L	↑	X	X	0801	0000	L	L	H	Q(0)
1st Read @ Full	H	H	X	L	↑	1000	0001	L	L	H	Q(1)
Last White	H	L	L	L	X			L	L	L	
Read/Write at											
2nd Read	H	H	X	L	↑	0002	0001	L	L	L	
1st Read	H	H	X	L	↑	0002	0001	L	L	L	
2nd White	H	L	↑	H	X	0002	0000	L	L	L	
1st White	H	L	↑	H	X	0001	0000	L	L	L	Q(0)
Reset	L	X	X	X	X						
Read/Write Controls											
MODE											

Notes:
 (1) The Read Pointer will increment if the FIFO is not empty.
 (2) The Write flag will increment if the FIFO is not full.
 (3) The flags will reflect the relative locations of the read and write pointers.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -2 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
iil	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA

Notes:

1. Transient inputs with Vil not more negative than -1.5 volts are permitted for pulse widths ≤ 10 ns

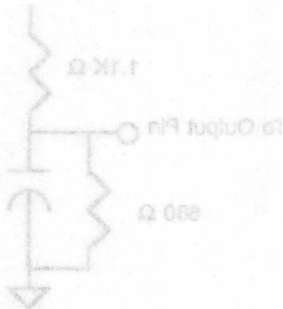
POWER SUPPLY CHARACTERISTICS

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
Vic = 0.2 Volts, Vhc = Vcc - 0.2 Volts

Symbol	Parameter		Clock Rate, mHz				Unit
			40	33	25	20	
Icc1	Operating Operating Current Vcc = MAX, Outputs open RE = WE = Vil, f = MAX	Com	150	140	130	120	mA
		MII					
Icc2	Standby Current RE = WE = RS = Vih	Com	15	15	10	10	
		MII					

Output Reference Levels	1.5V
Input Timing Reference Levels	1.5V
Input Pulse Width Times	3 ns
Input Pulse Levels	GND to 3.0V

30 pF * includes jig and scope capacitance



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

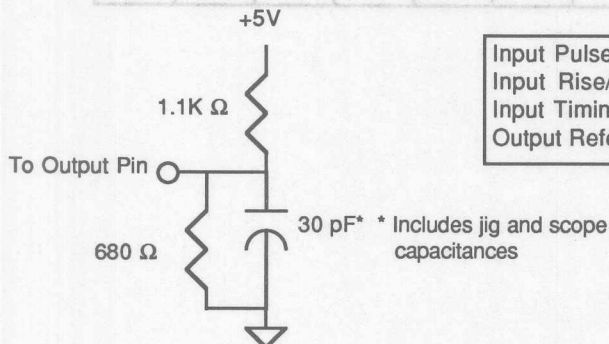
For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
 COMMERCIAL $V_{CC}=5V\pm10\%$, $T_A=0^\circ C$ to $+70^\circ C$, MILITARY $V_{CC}=5V\pm10\%$, $T_A=-55^\circ C$ to $+125^\circ C$

Symbol	Parameter (1)	Note	-40	-33	-25	-20	Unit	Type
f RC, f WC	Read or Write Clock, mHz	2	40	33	25	20	mHz	Min
t RC, t WC	Read or Write Cycle Time		25	30	40	50	ns	
t CW	Read or Write Clock High or Low	1	10	12	15	20		
t S	Enable, Write Data Setup Time		5	6	7	8		
t H	Enable, Write Data Hold Time		0	0	0	0		
t CF	Clock to Flag Output Delay		8	10	12	15		Max
t CD	Clock to Data Output Delay		7	8	9	10		
t RS	Reset Pulse Width	1	15	20	25	35		Min
t RSR	Reset Recovery Time	3	10	10	10	10		
t RF	Reset to Flag Delay		12	15	17	20		Max
t EFL, t FFL	Flag Latency, R/W to E/F	4	12	15	17	20		

Notes: These timings are measured as defined in AC Test Conditions

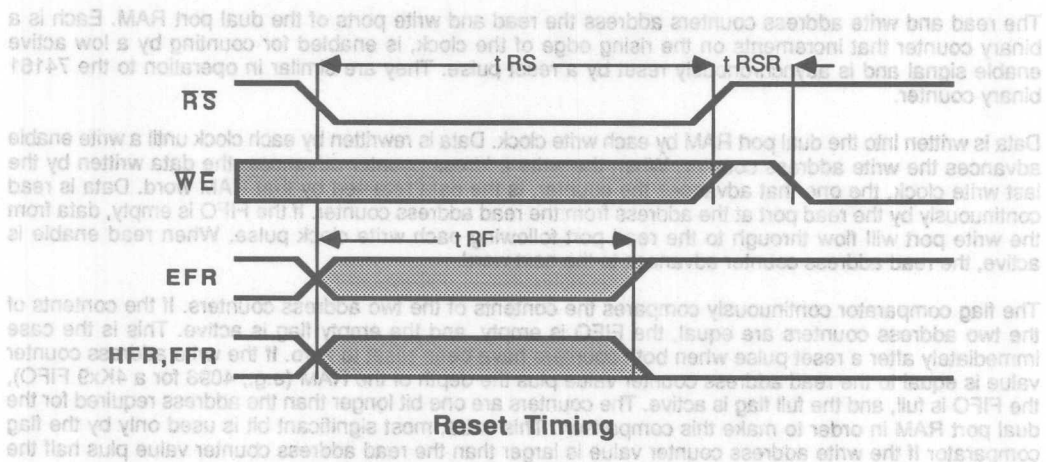
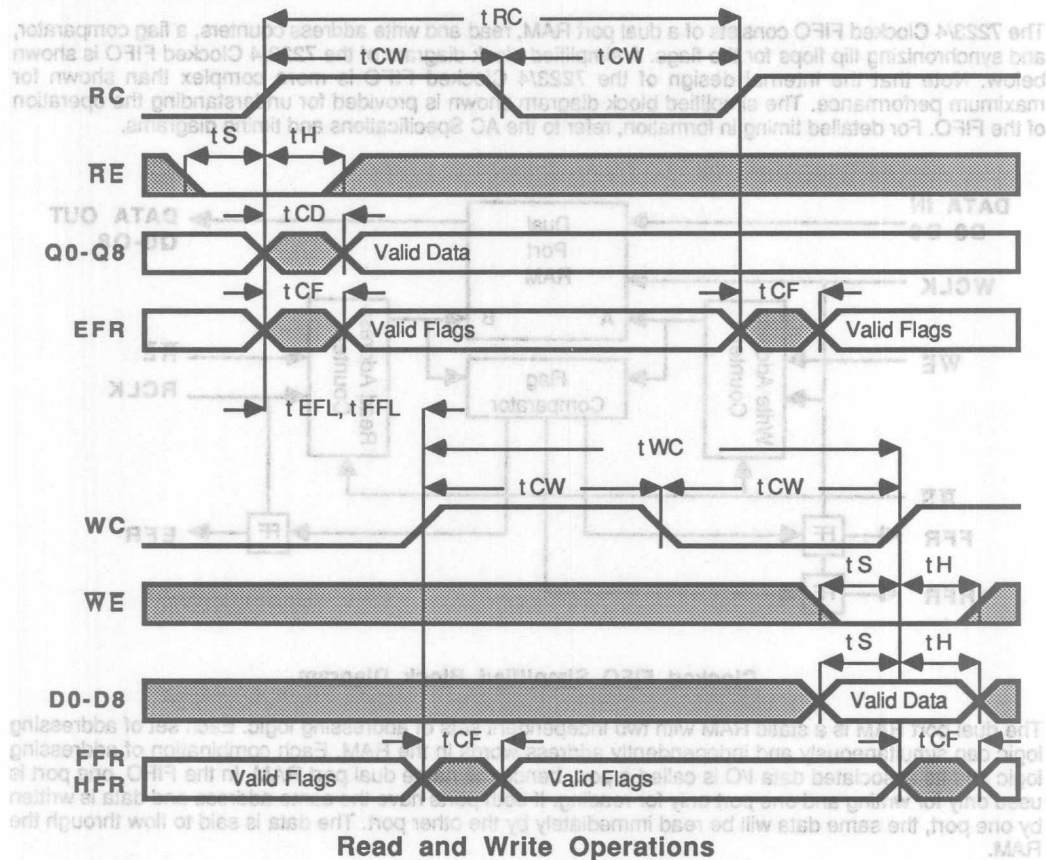
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. Minimum time to write clock edge for valid write enable to be accepted.
4. Time required from write clock edge to read clock edge for write to turn off empty on next clock;
 Time required from read clock edge to write clock edge for read to turn off full on next clock.

AC TEST CONDITIONS



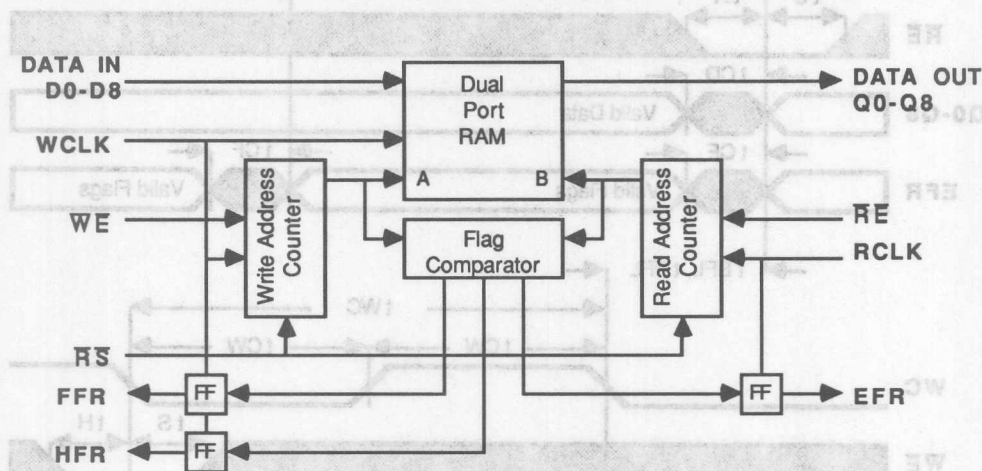
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

TIMING DIAGRAMS



OPERATIONAL DESCRIPTION

The 7223/4 Clocked FIFO consists of a dual port RAM, read and write address counters, a flag comparator, and synchronizing flip flops for the flags. A simplified block diagram of the 7223/4 Clocked FIFO is shown below. Note that the internal design of the 7223/4 Clocked FIFO is more complex than shown for maximum performance. The simplified block diagram shown is provided for understanding the operation of the FIFO. For detailed timing information, refer to the AC Specifications and timing diagrams.



Clocked FIFO Simplified Block Diagram

The dual port RAM is a static RAM with two independent sets of addressing logic. Each set of addressing logic can simultaneously and independently address words in the RAM. Each combination of addressing logic and its associated data I/O is called a port, hence the name dual port RAM. In the FIFO, one port is used only for writing and one port only for reading. If both ports have the same address and data is written by one port, the same data will be read immediately by the other port. The data is said to flow through the RAM.

The read and write address counters address the read and write ports of the dual port RAM. Each is a binary counter that increments on the rising edge of the clock, is enabled for counting by a low active enable signal and is asynchronously reset by a reset pulse. They are similar in operation to the 74161 binary counter.

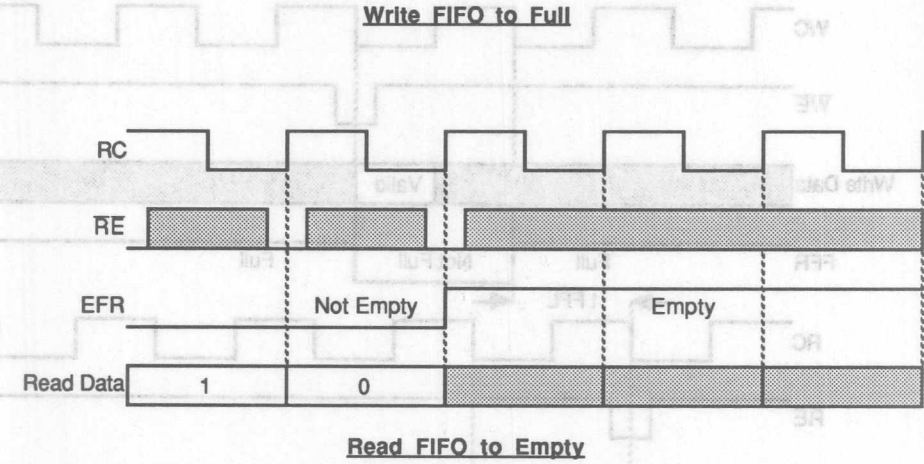
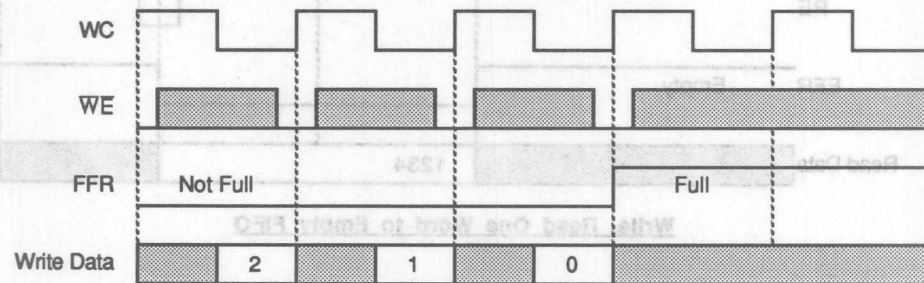
Data is written into the dual port RAM by each write clock. Data is rewritten by each clock until a write enable advances the write address counter. When the write address counter advances, the data written by the last write clock, the one that advances the counter, is the data retained by that RAM word. Data is read continuously by the read port at the address from the read address counter. If the FIFO is empty, data from the write port will flow through to the read port following each write clock pulse. When read enable is active, the read address counter advances to the next word.

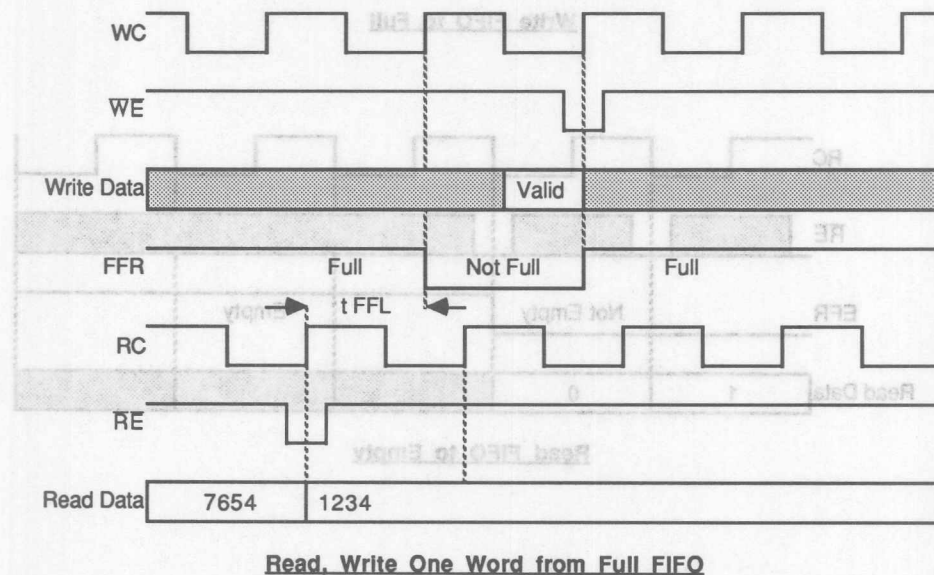
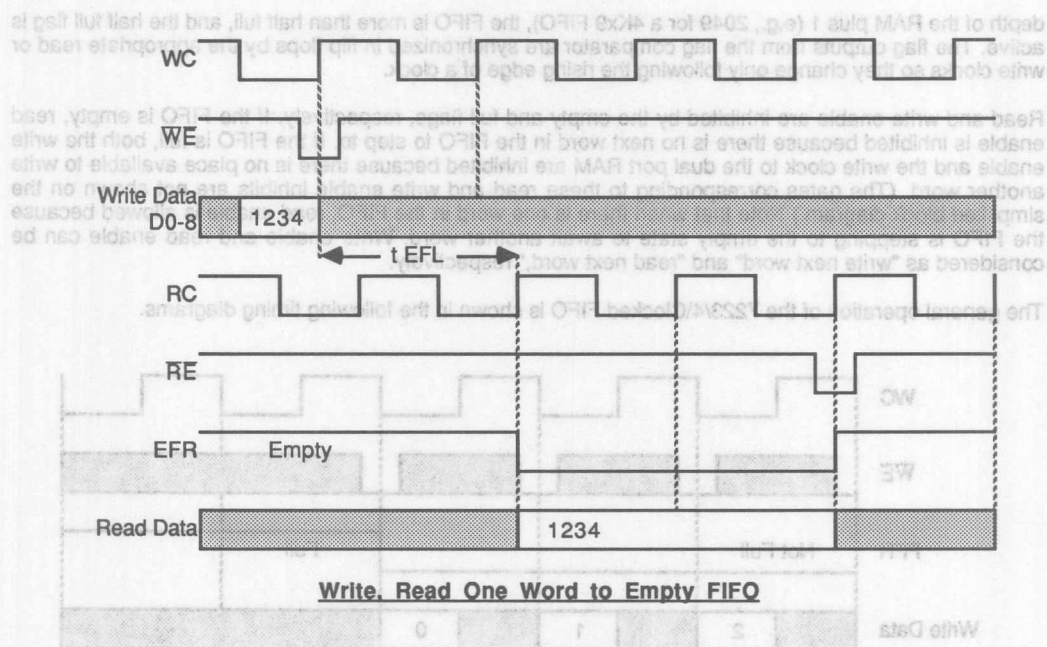
The flag comparator continuously compares the contents of the two address counters. If the contents of the two address counters are equal, the FIFO is empty, and the empty flag is active. This is the case immediately after a reset pulse when both counters have been reset to zero. If the write address counter value is equal to the read address counter value plus the depth of the RAM (e.g., 4096 for a 4Kx9 FIFO), the FIFO is full, and the full flag is active. The counters are one bit longer than the address required for the dual port RAM in order to make this comparison. This extra, most significant bit is used only by the flag comparator. If the write address counter value is larger than the read address counter value plus half the

depth of the RAM plus 1 (e.g., 2049 for a 4Kx9 FIFO), the FIFO is more than half full, and the half full flag is active. The flag outputs from the flag comparator are synchronized in flip flops by the appropriate read or write clocks so they change only following the rising edge of a clock.

Read and write enable are inhibited by the empty and full flags, respectively. If the FIFO is empty, read enable is inhibited because there is no next word in the FIFO to step to. If the FIFO is full, both the write enable and the write clock to the dual port RAM are inhibited because there is no place available to write another word. (The gates corresponding to these read and write enable inhibits are not shown on the simplified block diagram.) Note that when there is one word in the FIFO, read enable is allowed because the FIFO is stepping to the empty state to await another word. Write enable and read enable can be considered as "write next word" and "read next word," respectively.

The general operation of the 7223/4 Clocked FIFO is shown in the following timing diagrams.





APPLICATION INFORMATION

Width Expansion

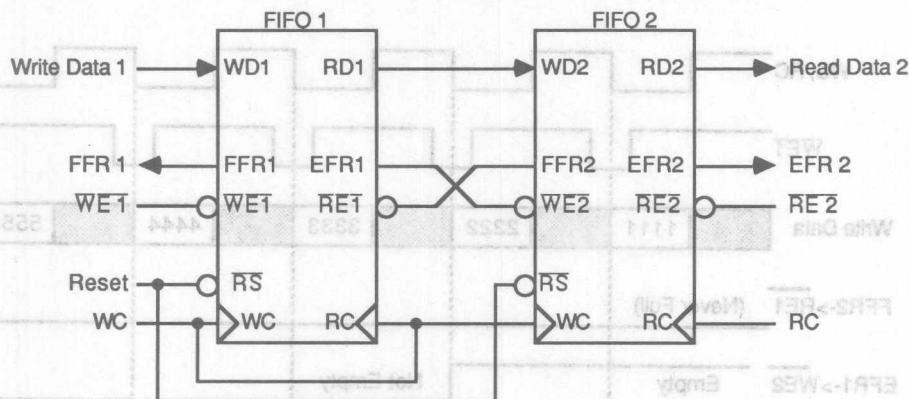
The 7223/4 Clocked FIFOs may be expanded in width by connecting the read and write clocks and enables and the reset lines of the FIFOs in parallel. The flags on all FIFOs will track, so any FIFO can be used for flag information.

Bus Width Funneling

The 7223/4 FIFOs simplify bus width funneling in high speed systems. Bus width funneling is where data must pass between two buses of different width, such as 32 bits and 8 bits. Funneling with the 7223/4 FIFOs is accomplished with external logic. The advantage of the 7223/4 Clocked FIFO interface is the simplification of the timing parameters for the funneling action. Funneling logic requires deciding which FIFOs are to be enabled for read or write on a particular cycle. For example, on a 32-bit to 8-bit transfer, 32-bit data is written into four FIFOs simultaneously. The 8-bit data is read out of the four FIFOs in round-robin fashion. With the 7223/4, most of the clock cycle is available for the round robin FIFO enable decision, since the read and write enables require only a short setup time before the rising edge of clock.

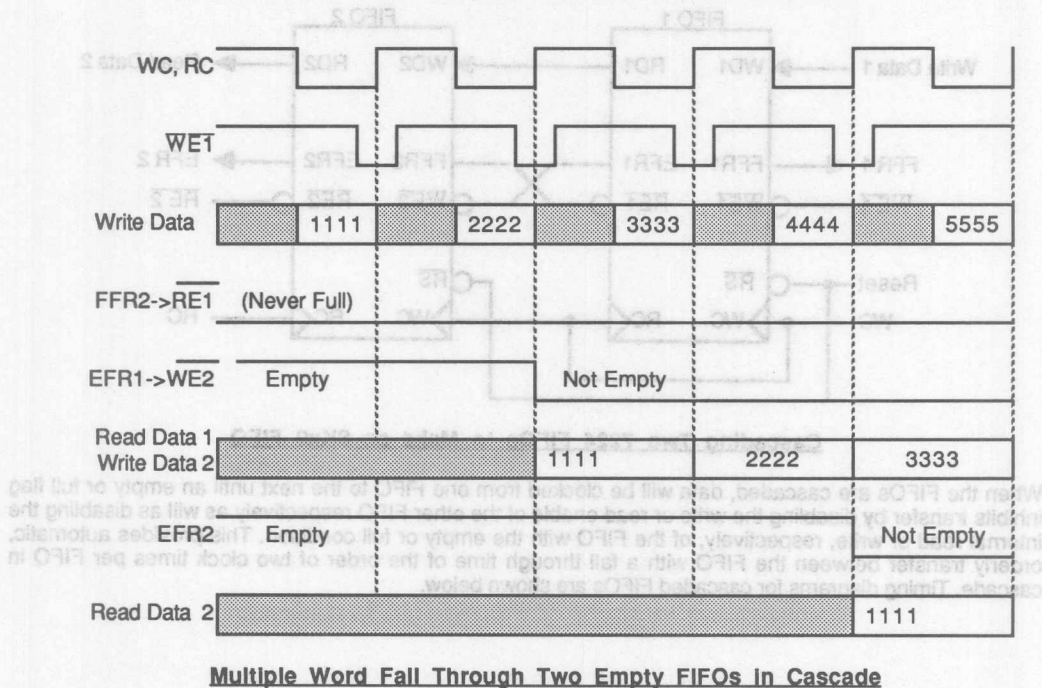
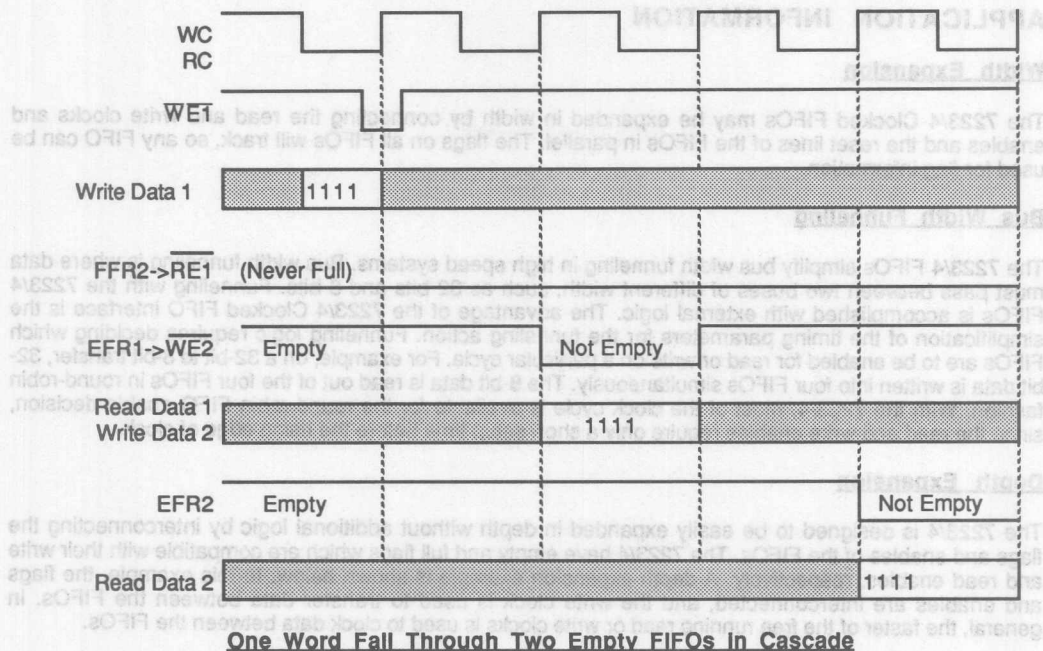
Depth Expansion

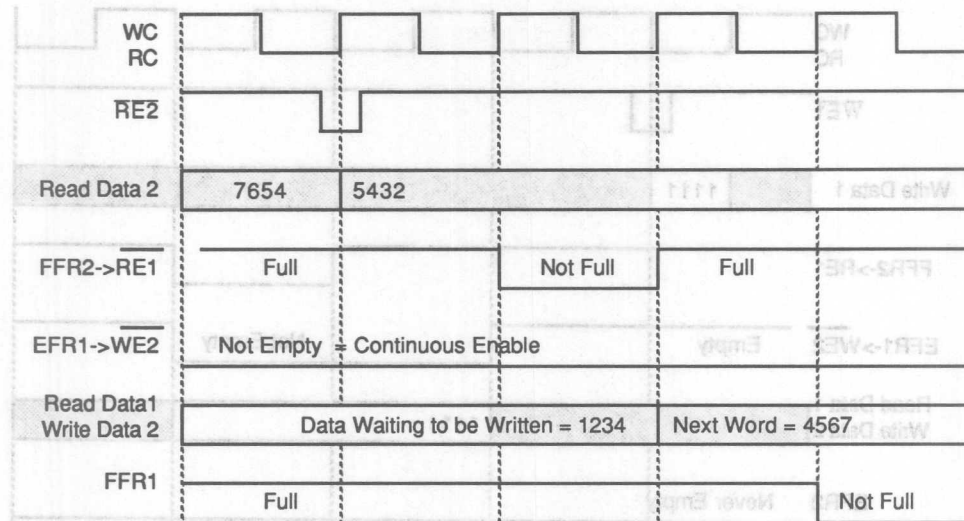
The 7223/4 is designed to be easily expanded in depth without additional logic by interconnecting the flags and enables of the FIFOs. The 7223/4 have empty and full flags which are compatible with their write and read enables, respectively. A depth expansion example is shown below. In this example, the flags and enables are interconnected, and the write clock is used to transfer data between the FIFOs. In general, the faster of the free running read or write clocks is used to clock data between the FIFOs.



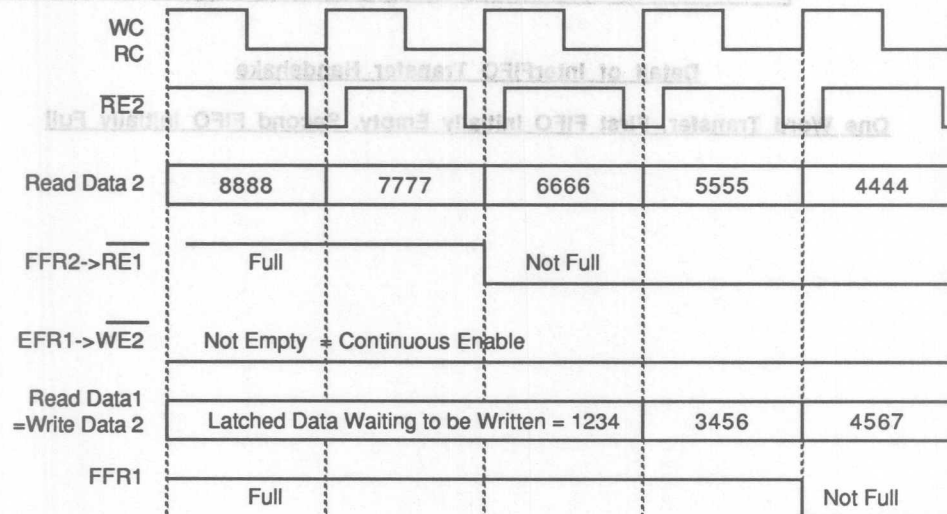
Cascading Two 7224 FIFOs to Make an 8Kx9 FIFO

When the FIFOs are cascaded, data will be clocked from one FIFO to the next until an empty or full flag inhibits transfer by disabling the write or read enable of the other FIFO respectively as well as disabling the internal read or write, respectively, of the FIFO with the empty or full condition. This provides automatic, orderly transfer between the FIFO with a fall through time of the order of two clock times per FIFO in cascade. Timing diagrams for cascaded FIFOs are shown below.



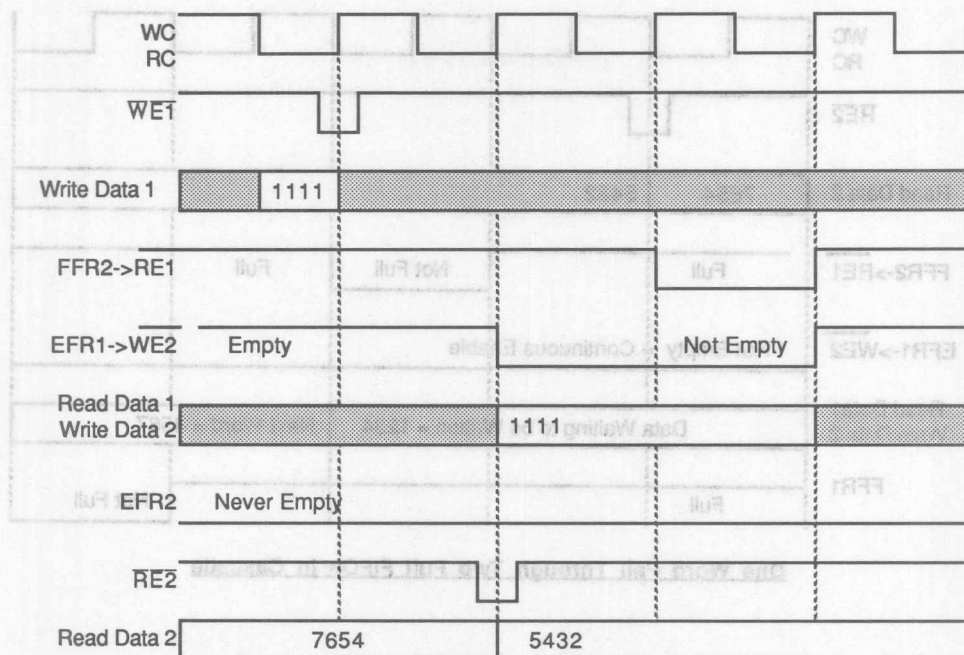


One Word Fall Through Two Full FIFOs in Cascade



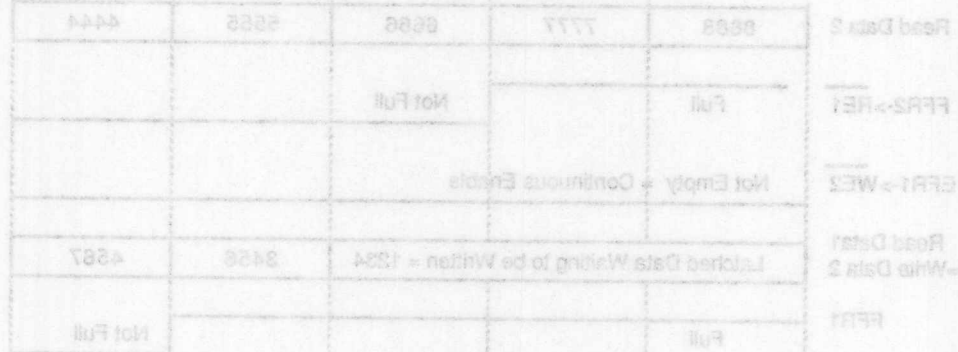
Multiple Word Fall Through Two Full FIFOs in Cascade

QS7223, QS7224



Detail of InterFIFO Transfer Handshake

One Word Transfer, First FIFO Initially Empty, Second FIFO Initially Full



Multiple Word Transfer Through Two FIFOs to Cascade



64K x 4 Ultra Deep FIFO Memory

QS7306
ADVANCE
INFORMATION

FEATURES/BENEFITS

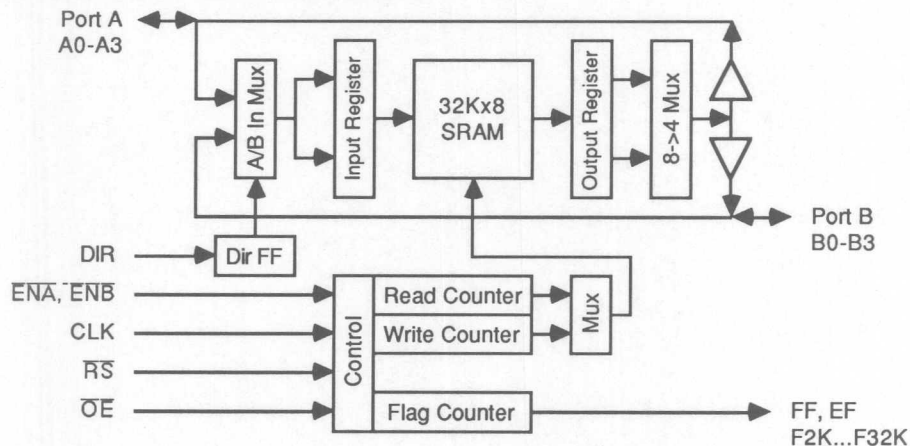
- 64Kx4 Ultra Deep FIFO
- Reversible (A to B or B to A)
- OE control pin
- 1/2, 1/4, 1/16, 1/32 status flags
- Directly cascades with another UD FIFO
- 50 MHz clocked interface
- Simultaneous read and write
- Empty and Full flags
- 24-pin DIP, SO, and ZIP packages

DESCRIPTION

The 7306 is a high density, high performance , 64K deep, 4-bit-wide FIFO. The 7306 has clocked interface with a single clock common to both its ports. Clock enables allow independent data transfer on either port at rates to 50 MHz, up to and including simultaneous read and write on both ports at 50 MHz. It is capable of moving data from port A to port B or from port B to port A. The direction is set upon reset by the direction control pin. The 7306 allows simultaneous read and write operations at speeds up to 50MHz. All operations occur on rising edge of the clock. The 7306 has an output enable pin which controls the port that is configured for read operation. The 7306 directly cascades to another 7306 or to QSI's 8224 clocked FIFO with no external logic. The 7306 has an Empty flag, a Full flag and 1/2, 1/4, 1/8, 1/16, and 1/32 status flags.

3

FUNCTIONAL BLOCK DIAGRAM

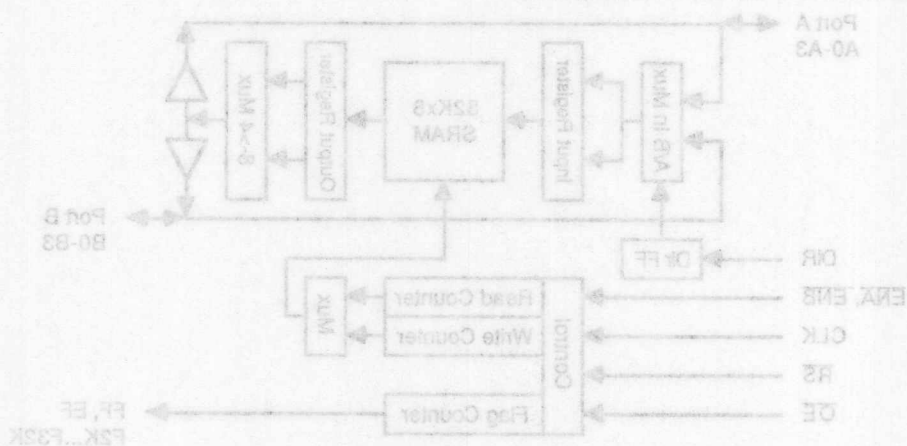


PIN CONFIGURATIONS

ENA	1	24	VCC
ENB	2	23	F32K
RS	3	22	F16K
DIR	4	21	F8K
FF	5	20	F4K
EF	6	19	F2K
CLK	7	18	OE
DA	8	17	DB
DA	9	16	DB
DA	10	15	DB
DA	11	14	DB
GND	12	13	GND

The 7306 is a high density, high performance, 64K deep, 4-bit-wide FIFO. The 7306 has clocked internal data paths with a single clock common to both ports. Clock enables allow independent data transfer on either port at rates to 50 MHz, up to and including simultaneous read and write on both ports at 50 MHz. It is capable of moving data from port A to port B or from port B to port A. The direction is set upon reset by the direction control pin. The 7306 allows simultaneous read and write operations at speeds up to 50MHz. All operations occur on rising edge of the clock. The 7306 has an output enable pin which controls the port that is configured for read operation. The 7306 directly cascades to another 7306 or to QSI's 8234 clocked FIFO with no external logic. The 7306 has an Empty flag, a Full flag and 1/2, 1/4, 1/8, 1/16, and 1/32 status flags.

FUNCTIONAL BLOCK DIAGRAM





64K x 4 Ultra Deep Burst Mode Dual Port RAM

QS7316
ADVANCE
INFORMATION

FEATURES/BENEFITS

- 64Kx4 Ultra Deep Dual Port
- Allows simultaneous access on both ports
- 4 cycles first read access, 1 cycle burst read access
- All operations occur on rising edge of clock
- 2 cycle first write access, 1 cycle burst write access
- Single 50MHz clocked interface
- Simultaneous burst access on both ports
- 32-pin package
- 64Kx4 internal single-port RAM architecture

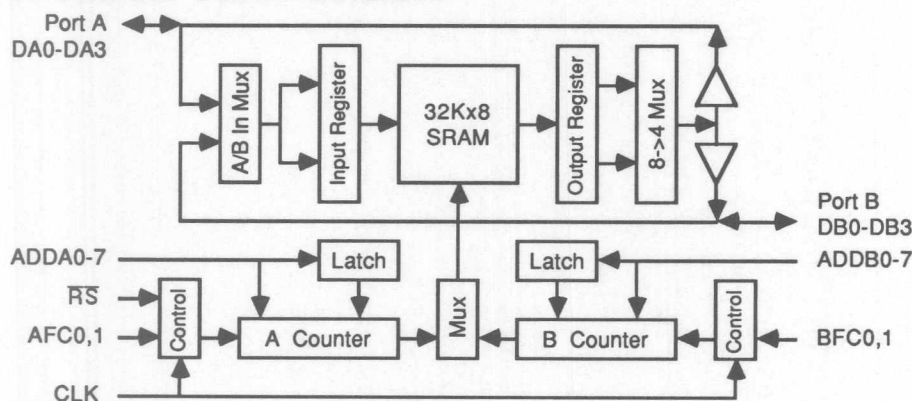
DESCRIPTION

The 7316 is a high density, high performance , 64K deep, 4-bits-wide dual port SRAM with burst mode. The 7316 has clocked interface with a single clock common to both its ports. Each port can be read from or written to in a random access manner as well as in the burst mode. The 7316 allows simultaneous read and write operations at speeds up to 50MHz. All operation occur on rising edge of the clock.

The 7316 may be addressed randomly or sequentially (burst) on either port. Address counter registers provide the addresses for sequential access and built-in control logic allows simultaneous access on both ports with the provision of three clocks (max) for first access and one clock burst access thereafter.

Two function control bits are used to control each port interface. The select the functions of Load Address for Read (LAR), Load Address for Write (LAW), Next Word (NW) for burst transfers, and HOLD. The Load Address functions cause the address register to be loaded on the rising edge of the clock. The 7316 uses a multiplexed address bus for each of its ports. When an LAR or LAW code is presented, the 8 most significant bits (MSBs) on the address bus are loaded into an address latch. On the rising edge of clock, the 16-bit address counter is loaded with the 8 MSBs from the address latch and the 8 LSBs from the bus.

FUNCTIONAL BLOCK DIAGRAM



AFC0

DA	13	20	DB
DA	14	19	DB
DA	15	18	DB
GND	16	17	DB

[illegible]

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Quality And Reliability	7
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8	Package Information
9	Sales Offices

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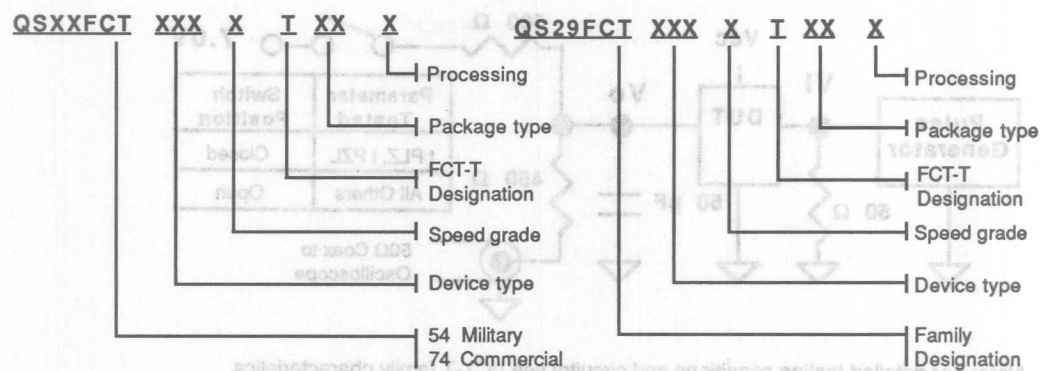
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QS54/74FCT574	4-173
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FCT-T Ordering Information



Speed Grades:

Blank - Standard

A

B

C

D

Processing:

Blank - Standard

B - MIL-STD 883

Package Type:

P - Plastic DIP, 300 mil

D - Ceramic DIP, 300 mil

L - Leadless Ceramic Chip Carrier

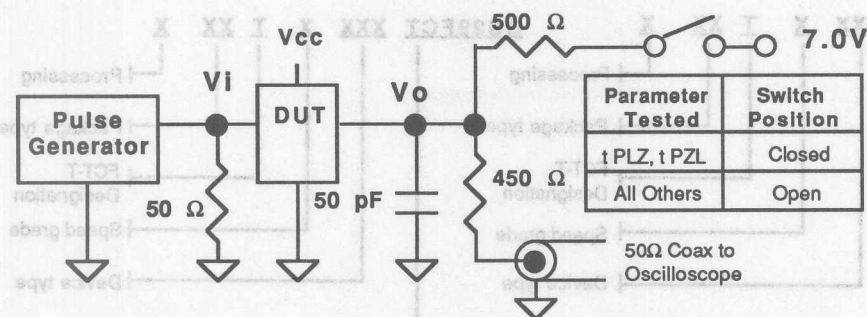
SO - Small Outline IC, 300 mil

S1 - Small Outline IC, 150 mil

Z - Plastic ZIP

Q - QSOP, Quarter Size Outline Package, 150 mil

FCT-T Test Configuration



Note: For detailed testing conditions and circuitry see FCT-T family characteristics

Package Type	
P	Plastic DIP, 300 mil
D	Plastic DIP, 300 mil
L	Leadless Ceramic Chip Carrier
SC	Small Outline IC, 300 mil
SO	Small Outline IC, 180 mil
Σ	Plastic DIP
Q	QSO, Quarter Size Outline Package, 180 mil

Processing	
B	MIL-STD 883
Blank	Standard
A	Blank - Standard

FCT-T Family Characteristics

FCT-T Family Circuit Characteristics

FCT-T Logic Family Characteristics

FCT Logic was introduced in 1985 as a low power CMOS replacement for the popular 74F series bipolar logic. It became popular almost immediately, and it is now a JEDEC standard logic family available from multiple vendors. Specifications on the original FCT logic family were, by intent, exactly the same as their 74F bipolar equivalents except for significantly lower power: FCT devices typically required less than 50 mW versus 500 mW or more for 74F, a 90% power savings.

While the original FCT logic family has its outputs typically swing from ground to 4.5V, the state-of-the-art FCT logic family have reduced output voltage swings, from ground to typically 3.5V. This makes the family more compatible with TTL logic and help to control system noise at high speeds. The reduced output swing FCT logic is denoted FCT-T, and all its part numbers carry a suffix T after the speed grade letter. In this chapter we use FCT and FCT-T interchangeably. All QSI FCT products have reduced output swing and are marked 74QSFCXXXXYT (e.g. 74QSFC138AT).

When the FCT-T family was introduced, testing showed that the parts were significantly faster than the bipolar parts they replaced. The advantage of using advanced CMOS technology resulted in an immediate 25 to 35% speed improvement. These higher speed parts were identified by an "A" suffix. This immediately made them the fastest TTL logic available. FCT-T continues to be the fastest TTL logic family, as successive improvements have resulted in additional speed grades including "B", "C" and now "D" grades, with each speed grade being 20-35% faster than the previous grade. The continual improvement in FCT-T performance follows the general trend of performance improvement of CMOS technology. This allows FCT-T to keep pace with the continual performance improvement of other system components.

The FCT-T family from QSI has additional features and options available to the system designer. FCT-T from QSI has hysteresis on all inputs, which reduces noise sensitivity for signals with slow rise and fall times. QSI has also introduced the FCT2000 series resistor family which adds an on chip 25Ω resistor to each output. This resistor significantly reduces system noise and ringing without reducing speed. Adding series resistors has been a common design practice in high speed systems for many years. QSI supports this practice by providing the resistor inside the part. This reduces the board space required and allows the speed of the part to be specified with the resistor included. QSI was the first to extend this concept to the full FCT-T family and to fully specify and control the resistor value. For each standard FCT-T part (e.g. FCT244), QSI also offers a resistor output version (e.g. FCT2244).

QSI has also pioneered new packages for logic to reduce board space and increase performance. The ZIP package provides a 50% space savings over a PDIP, providing surface mount density in a through-hole environment. The Quarter-size Small Outline Package (QSOP) is half the length and half the width of the SOIC it replaces, resulting in a four times increase in board density.

High Performance CMOS Technology

High performance CMOS technology has revolutionized logic. In 1980, bipolar was the logic of choice for high speed systems. CMOS, although very low power, was ten times slower and used only where its low power was a significant advantage. That all changed with the development of high performance, short channel length CMOS technology and the corresponding creation of the FCT family. Suddenly, CMOS was the fastest technology, and bipolar was the medium speed, power hungry prior logic generation. This happened because of differences in the potential for improvement of each technology.

Improvement in semiconductor technology is driven by improvement in the precision of creating patterns on the silicon - called lithography, as governed by the optics of the machines which project these patterns. This precision is specified by the smallest feature that can be reliably printed, the minimum feature size.

FCT-T Family Characteristics

Processes are identified by this feature size, e.g. 1.0 micron CMOS. Increased precision allows the creation of smaller devices. Smaller devices are faster devices; however, there is a difference between CMOS and bipolar types. CMOS improves much more rapidly than bipolar with reduction in device size.

In a bipolar device, the delay of a gate is determined by the capacitance of the device divided by the current through the device. To improve the speed, one should increase the current and decrease the capacitance. Increasing the current is not practical: it is already set at the highest value the power dissipation the package will allow, usually 100 to 150 mA for PDIP packages. This is the source of the well known speed-power product (actually a speed-current product) of bipolar logic. The only other possibility for increasing the speed is to decrease the capacitance by decreasing the device size. This too has a limit. The device must be a certain minimum size to support the current available to it. This minimum size defines the minimum capacitance, and therefore the speed-power product limit. Reducing the device further will reduce the capacitance, but the current must be reduced as well. As a result, bipolar devices have improved only slowly over time, from the 20+ ns delay of the 7400 in 1965 to the 5 ns delay of the 74F00 of today.

In a CMOS device, the delay of a gate is determined by the product of the channel on resistance and the gate capacitance. Decreasing the feature size to make the CMOS devices smaller reduces both the on resistance and the gate capacitance, resulting in a delay improvement at roughly the square of the rate of improvement in feature size. For example, a 10% reduction in feature size provides a 10% reduction in gate length. This causes at least a 10% reduction in on resistance and a 10% reduction in gate capacitance. As a result, a 10% reduction in feature size provides a 20% reduction in gate delay. The performance improvement in going from 3 micron CMOS to 1 micron CMOS should be of the order of a factor of 10. This is the source of the dramatic transition of CMOS from 50 ns gates in 1975 to a 4 ns gates in 1985.

CMOS is also the technology of the future. Unlike bipolar and GaAs devices, CMOS is not speed-power limited. The CMOS device is voltage driven. It only draws power when it switches. Bipolar and GaAs devices are current amplifiers, however. They must draw current when they are on in order to stay on. Bipolar and GaAs devices are capable of very high speeds when unlimited power is available, such as in single transistors and small logic devices. However as the chip size increases, package power dissipation limits convert the speed-power product into a speed-density product. The bigger you make it, the slower it gets because each gate you add must draw power even if it is not switching.

CMOS does not have the bipolar speed-power problem. Gates which are not switching draw no power. This is a significant advantage in LSI designs. Very often, a large portion of the system logic is used infrequently or switches at a low frequency. This logic can be combined into one chip with little increase in the chip power. This allows increasing integration without speed degradation.

CMOS does have a speed-power effect, however. Each gate draws a small amount of power when it switches, resulting in a power dissipation component that increases with frequency. This is equivalent to the power required to charge and discharge an effective internal capacitance. For FCT logic, this effective internal capacitance is roughly equal to the typical load capacitance seen by the device. Also, this effective internal capacitance decreases with each improvement in speed of the device.

QCMOS™ Technology

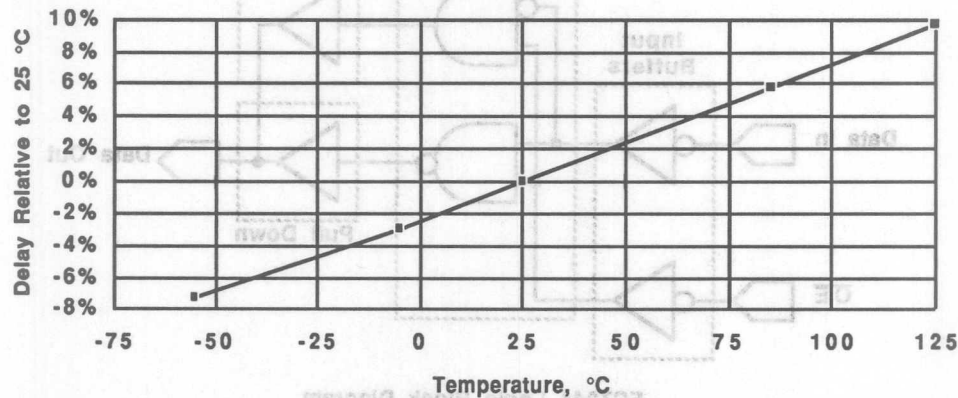
QCMOS™ is representative of the current state-of-the-art in high speed CMOS technology. QCMOS™ is currently being produced in 1.0 micron and 0.8 micron versions with a development path to 0.5 micron and below. It is a dual-well, ion-implanted technology with substrate bias to reduce body effect capacitance and prevent latchup. QCMOS™ uses shallow, ion implanted junctions for low capacitance and high speed for a given device size. QCMOS™ technology also provides lower on resistance for a given device size. The result is very high speed for a given feature size, providing almost a full generation of speed improvement.

QCMOS™ has the additional advantage that it is relatively insensitive to temperature. QCMOS™ device characteristics typically vary only 10% over the full temperature range, as compared to 30% for other high

FCT-T Family Characteristics

performance CMOS technologies. An example of the temperature characteristics of QCMOS™ is shown below in the plot of propagation delay versus temperature for the FCT373. The stable temperature characteristics of QCMOS™, coupled with 6 transistor SRAM cell technology allows manufacture of high performance devices for wide temperature range applications such as military and space equipment.

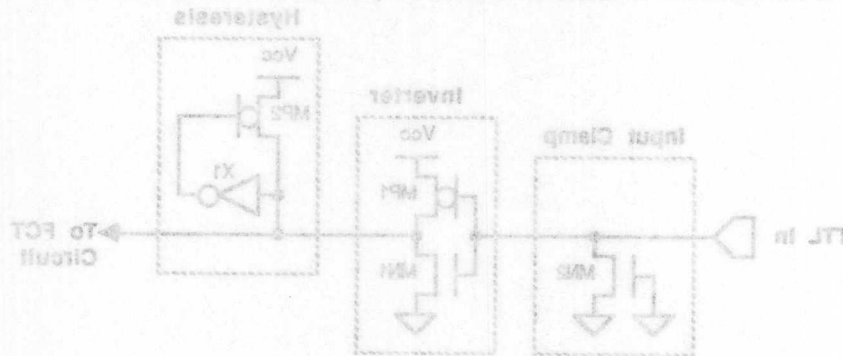
Change In Delay vs Temperature for FCT373



4

Delay versus Temperature for FCT373

The input characteristics of the FCT-T family are determined by the input buffers. A circuit diagram of an input buffer is shown below. It consists of an inverter, an input underfoot clamp and a hysteresis circuit.



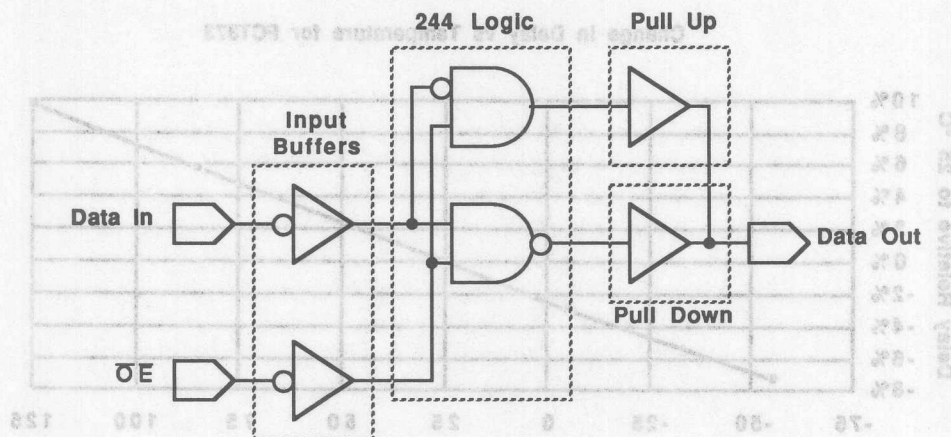
FCT-T Input Buffer Circuit Diagram

The inverter is designed to provide an input threshold of approximately 1.0 volt for TTL compatibility. This is accomplished by adjusting the size of the two transistors, MP1 and MN1. This is affected by the hysteresis circuit consisting of MP2 and X1. When the input is high and going low, the inverter output is low and the hysteresis transistor, MN2, is off and the high-to-low threshold is approximately 1.4 volts. When the input is low and going high, the inverter output is high and MP2 is on. MP2 increases the threshold by approximately 0.5 volts so that the low-to-high threshold is approximately 1.9 volts. This 500 millivolts of hysteresis reduces noise sensitivity for signals passing through the threshold region.

FCT-T Family Characteristics

FCT-T Circuitry

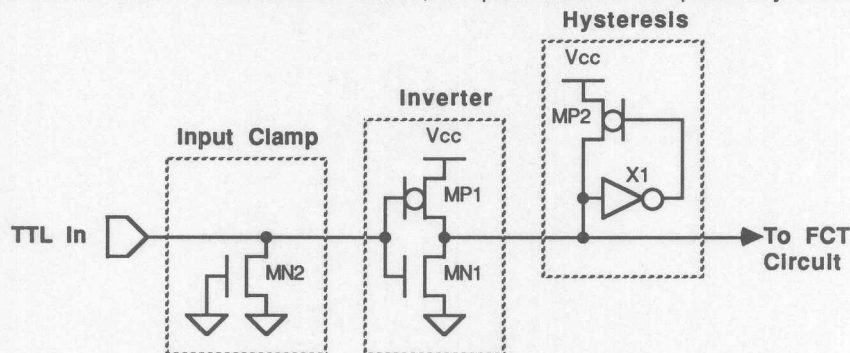
FCT-T logic consists of standard input and output circuits combined with specific logic for each member of the family. The FCT244 logic block diagram shown below is an example of a typical FCT-T design. The FCT244 is a simple buffer, consisting of input buffers, output drivers, and output enable logic.



FCT244 Logic Block Diagram

Input Characteristics

The input characteristics of the FCT-T family are determined by the input buffers. A circuit diagram of an input buffer is shown below. It consists of an inverter, an input undershoot clamp and a hysteresis circuit.

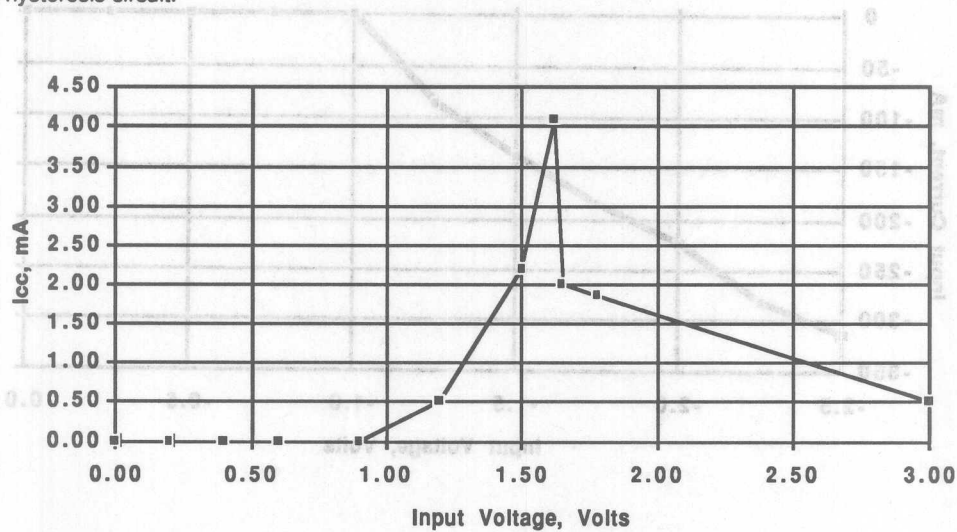


FCT-T Input Buffer Circuit Diagram

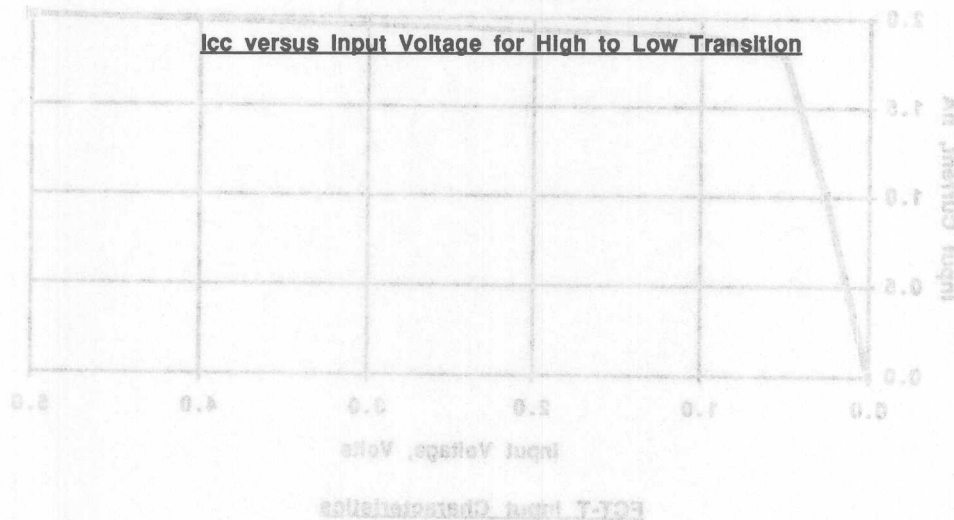
The inverter is designed to provide an input threshold of approximately 1.40 volts for TTL compatibility. This is accomplished by adjusting the sizes of the two transistors, MP1 and MN1. This is affected by the hysteresis circuit consisting of MP2 and X1. When the input is high and going low, the inverter output is low and the hysteresis transistor, MN2, is off and the high-to-low threshold is approximately 1.4 volts. When the input is low and going high, the inverter output is high and MP2 is on. MP2 increases the threshold by approximately 0.2 volts so that the low to high threshold is approximately 1.60 volts. This 200 millivolts of hysteresis reduces noise sensitivity for signals passing through the threshold region.

FCT-T Family Characteristics

The input buffer circuitry does not draw current when the input is at 0.0 volts or at V_{CC} . When the input is at 0.0 volts, MN1 is off and no current can flow from either MP1 or MP2. If the input is at V_{CC} , both MP1 and MP2 are both off, and no current flows. When the input is between 0.0 volts and V_{CC} , both MN1 and MP1 are partially on, and current flows between V_{CC} and ground. This is the source of the ΔI_{CC} specification which defines the maximum current drawn by an input buffer when the input is at the typical transition point indicated by the current peak is approximately 1.6 volts. A similar plot for a low to high transition would show a transition point of approximately 1.4 volts. Note the step in the current provided by the hysteresis circuit.



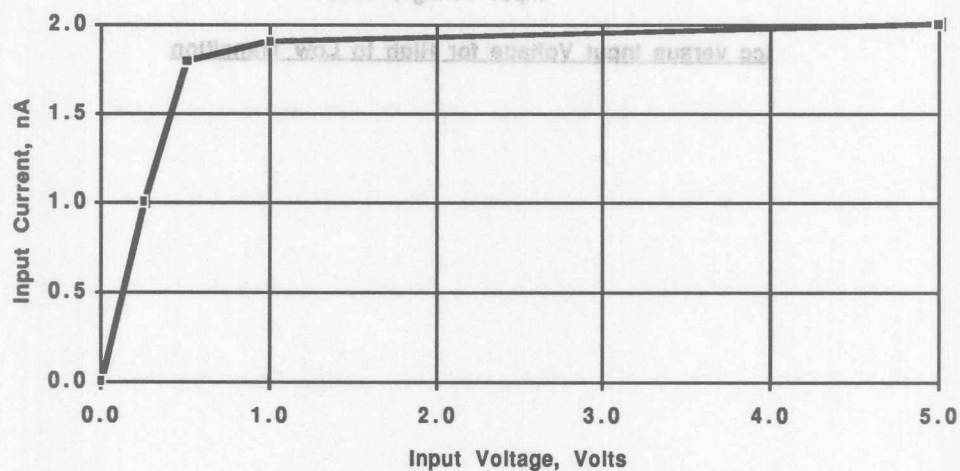
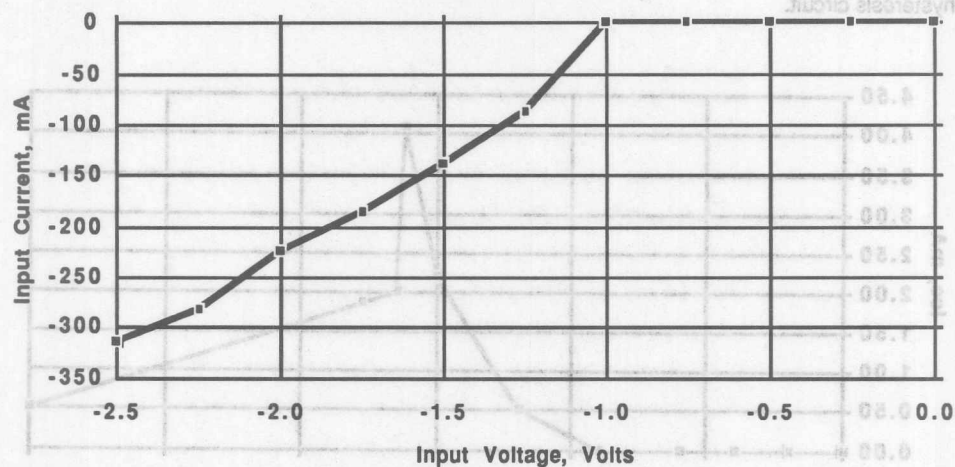
I_{CC} versus Input Voltage for High to Low Transition



FCT-T Family Characteristics

Input Clamp

The input clamp, MN2, turns on when the input goes negative, providing clamp action for negative undershoot transients and thereby reducing system noise. Note that there is no positive clamp. The input can go above V_{CC} without conducting current. In fact, actual input leakage is of the order of a few nanoamperes over the input range of 0.0 to 5.0 volts at room temperature. A graph of typical input characteristics is shown below.

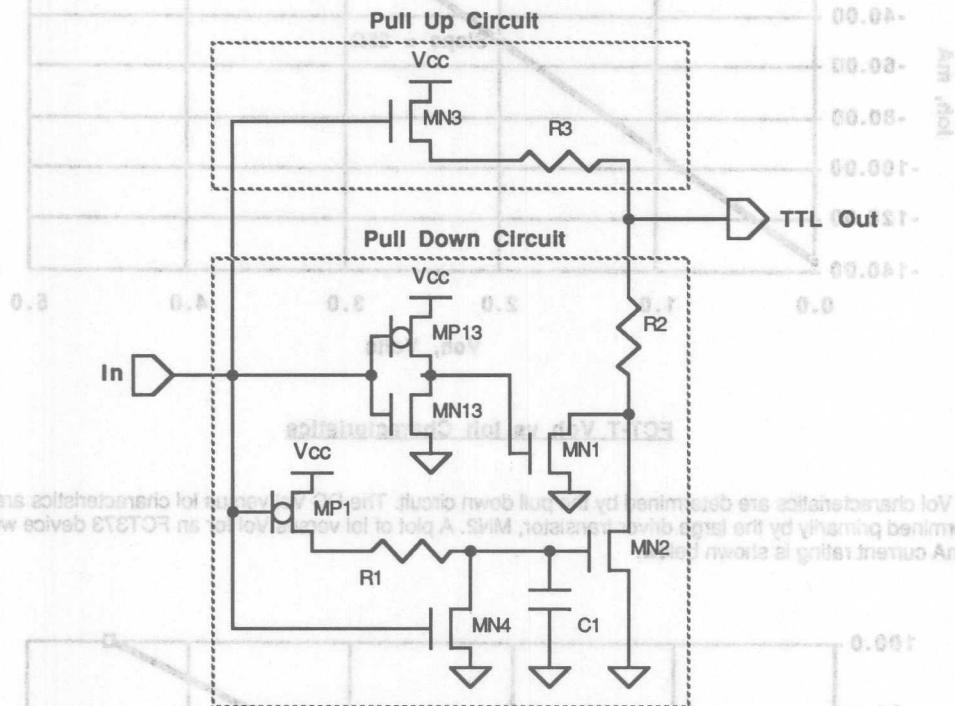


FCT-T Input Characteristics

FCT-T Family Characteristics

Output Characteristics

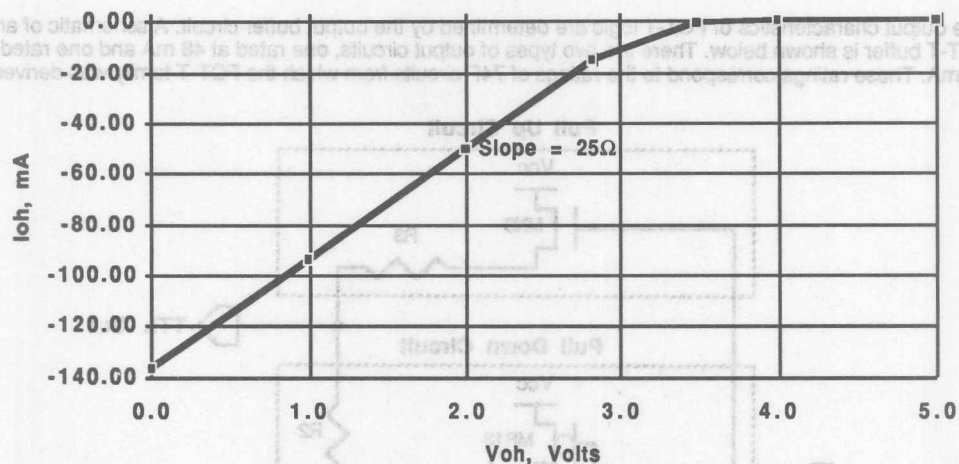
The output characteristics of FCT-T logic are determined by the output buffer circuit. A schematic of an FCT-T buffer is shown below. There are two types of output circuits, one rated at 48 mA and one rated at 64 mA. These ratings correspond to the ratings of 74F circuits from which the FCT-T family was derived.



FCT-T Output Buffer Circuit Diagram

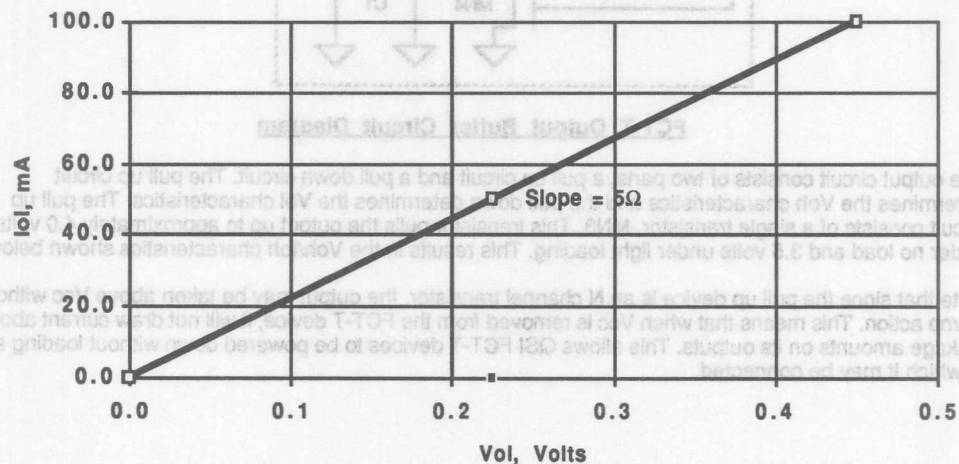
The output circuit consists of two parts, a pull up circuit and a pull down circuit. The pull up circuit determines the V_{oh} characteristics and the pull down determines the V_{ol} characteristics. The pull up circuit consists of a single transistor, MN3. This transistor pulls the output up to approximately 4.0 volts under no load and 3.5 volts under light loading. This results in the V_{oh}/I_{oh} characteristics shown below.

Note that since the pull up device is an N channel transistor, the output may be taken above V_{cc} without clamp action. This means that when V_{cc} is removed from the FCT-T device, it will not draw current above leakage amounts on its outputs. This allows QSI FCT-T devices to be powered down without loading a bus to which it may be connected.



FCT-T Voh vs Ioh Characteristics

The Vol characteristics are determined by the pull down circuit. The DC Vol versus Iol characteristics are determined primarily by the large driver transistor, MN2. A plot of Iol versus Vol for an FCT373 device with 48 mA current rating is shown below.



FCT-T Vol vs Iol Characteristics for FCT373. 48 mA Drive

FCT-T Family Characteristics

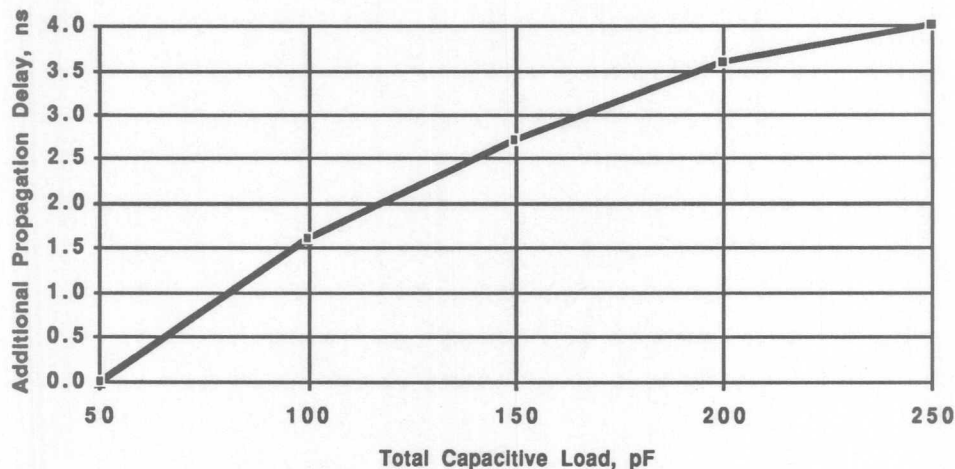
The Vol characteristics shown above are for standard output FCT-T devices. A 25 Ω resistor output option is available for all QSI FCT-T devices for system noise suppression. This option adds resistors R2 and R3, shown above in the output buffer schematic. These resistors are both shorted to zero ohms in the standard version. In the 25 Ω version, resistor R2 is 25 Ω , while resistor R3 remains at zero ohms. This results in a 28-30 ohm nominal output resistance when the output is low, consisting of 25 ohms for the resistor and 3-5 ohms typical for the output transistor, MN2. The resistor R3 is kept at zero ohms because the effective output resistance of the pull up transistor, MN3, is approximately 25 ohms in the region around the TTL threshold of 1.5 volts.

The output pull down circuit consists of two parts: an initial pull down transistor, MN1, and the main pull down transistor, MN2. This provides a two-step pull down characteristic. MN1 is turned on initially and provides a moderate pull down drive. At a later time determined by the combination of R1 and capacitor C1, the main drive transistor MN2 is turned on. The turn on time of MN2 can be adjusted by changing the value of resistor R1. This two stage turn on circuitry provides control of the output high to low transition in order to control ground bounce noise. (See Application Note AN01) Resistor R1 is adjusted to provide the best tradeoff of speed versus ground bounce noise.

When the output buffer is shut off, both the pull up and pull down transistors are shut off. The outputs may be taken above Vcc without current flow beyond a few nanoamperes of leakage. Taking an output below ground, however, will result in clamping action from the pull down transistors, MN1 and MN2, with clamp voltage and current characteristics similar to the input clamp characteristics discussed above.

Parameter Variations with Load

FCT-T propagation delay is affected by capacitive load, increasing with added load as shown below.



Change in Propagation Delay versus Capacitive Load for FCT373. Typical

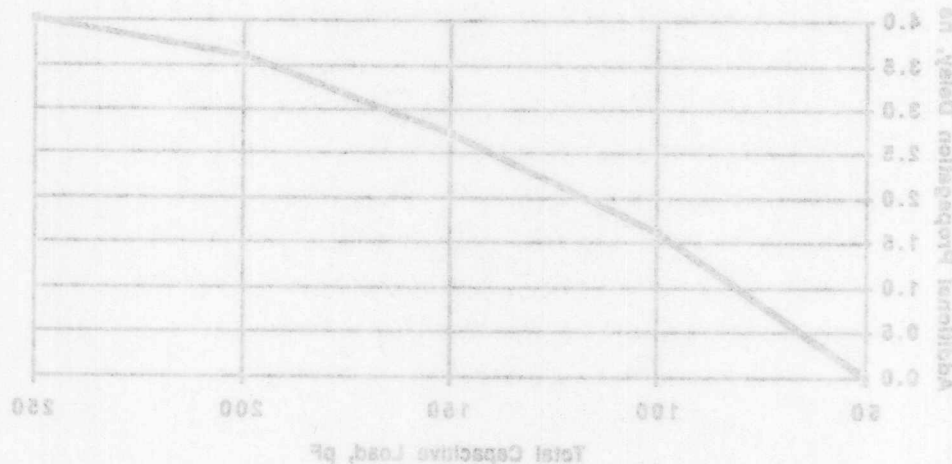
FCT-T Family Characteristics

Unit Loading & Fanout

In system designs, TTL devices drive other TTL devices. There are practical limitations on how many devices a given TTL device - such as an FCT-T device - can drive. This is defined as fanout, the number of other devices a given device can drive. Because of the high drive capability of FCT-T (48 or 64 mA minimum) and the low input current requirements of FCT-T (5 μ A, maximum) and other popular logic families, DC fanout of FCT-T is quite large, from 100 to 1000+ depending on the TTL devices being driven.

The fanout of a high performance logic family such as FCT-T determined by AC, not DC requirements. There is an effective AC fanout limit determined by the speed/fanout tradeoffs of a given design. FCT-T device AC performance is specified with a 50 pF load. For an input capacitance of 5-7 pF, this corresponds to an AC fanout of 7-10 if the data sheet specification is to be met. Loads above 50 pF will incur a propagation delay penalty of approximately 2.5 ns/100 pF of additional capacitance, as discussed in the FCT-T Family Characteristics section.

High performance logic such as FCT-T has high DC drive capability to insure that it can drive high capacitance loads. The DC drive capability of FCT-T is seldom used except for driving low impedance, resistor terminated loads such as terminated cables or backplanes. The more typical case is driving high capacitance, unterminated buses on PC cards or short backplanes. The high pull down drive specified by I_{OL} and the high pull up drive specified by I_{OH} insures that the FCT-T device can provide the current to drive high capacitive loads. For example, a 100 pF load being driven at a fall time of 5 ns required a drive current of $(3.5/5)(10) = 70$ mA. If high drive current capability were not provided, device performance would degrade rapidly with capacitive loading because of the limit on capacitive charge/discharge current.



FCT-T Family Characteristics

Parameter Variation with Multiple Outputs Switching: Ground Bounce

Ground bounce noise is a noise coupling between outputs in high speed logic and is function of package and resistor option. This is discussed in detail in application notes AN01, AN06, and AN07. Ground bounce noise is a function of ground lead inductance, which is highest in the DIP package. The ZIP package has a short ground lead, and the surface mount packages of SOIC and QSOP have shorter ground leads because their overall size is smaller. FCT2000 series resistor option devices have lower overall noise because of the damping action of the resistor; this reduces ground bounce as well. The chart below shows typical relative ground bounce values for various packages for FCT devices from the same wafer lot.

MULTIPLE OUTPUTS SWITCHING GROUND BOUNCE

Package	Ground Inductance	Relative G Bounce	FCT2000 GB Relative to Standard FCT-T
PDIP	13.7 nH	100%	60%
ZIP	5.3 nH	62%	60%
SOIC	8.5 nH	79%	60%
QSOP	3.6 nH	51%	60%

Parameter Variation with Multiple Outputs Switching: Propagation Delay

Propagation delay for TTL logic such as FCT-T is measured with one output switching. When multiple outputs switch at the same time, there is an added propagation delay called package pushout. This added delay is function of package and resistor option. Package pushout is related to ground bounce noise and is a function of ground lead inductance, which is highest in the DIP package. The ZIP package has a short ground lead, and the surface mount packages of SOIC and QSOP have shorter ground leads because their overall size is smaller. FCT2000 series resistor option devices have lower overall noise and package pushout because of the damping action of the resistor which reduces ground bounce. The chart below shows estimated package pushout values for various packages for FCT devices from the same wafer lot.

MULTIPLE OUTPUTS SWITCHING ADDED DELAY

Package	Added Delay
PDIP	0.90ns
ZIP	0.54ns
SOIC	0.72ns
QSOP	0.46 ns

Power Dissipation

The power requirements of FCT-T logic are much lower than the bipolar logic it replaces. Power requirements for QSI FCT-T logic have four sources: quiescent current, input buffer current, internal switching current, and load capacitance drive current. The quiescent current of QSI FCT-T is typically 0.5 mA which is primarily current for a substrate pump. This is specified as I_{CC} on the QSI FCT-T data sheets. The substrate pump provides bias for the substrate which reduces capacitance for increased speed.

The TTL input buffers draw current when their inputs are between approximately 0.5 volts and 4.0 volts. The input buffers do not draw current at a TTL low; however, they draw approximately 2 mA at the typical TTL high of 3.4 volts. This is specified as ΔI_{CC} on the QSI FCT-T data sheets. For an octal device such as an FCT244 with random data inputs of 50% duty cycle, this results in $(8)(2.0)(50\%) = 8 \text{ mA} = 40 \text{ mW}$ typical power to the input buffers.

CMOS logic draws internal current when it switches. When the input of a CMOS gate - such as the inverter in the TTL input buffer discussed earlier - transitions from low to high or high to low, there is a period of time when both the N channel and P channel devices are both on. During this transition time, current flows directly from V_{CC} to ground. This results in a certain amount of charge transferred equal to the average current times the transition time. The charge transfer per switching event results in a frequency dependent current, specified in mA per MHz as Q_{CCD} on the QSI FCT-T data sheets. This current represents the aggregate charge transferred by all gates in an FCT-T device when it switches. Since charge is transferred each time a gate switches, this is equivalent to charging and discharging a capacitor. For a Q_{CCD} of 0.25 mA per MHz and a V_{CC} of 5.0 volts, this is equivalent to an internal capacitance of 50 pF.

There is an additional source of device current which is not specified on TTL data sheets but is an important component of real system designs. This is the power required to charge and discharge external load capacitance. This current is a function of the V_{OH} of the device, the load capacitance and the frequency of the charge/discharge cycle. For QSI FCT-T logic with a typical V_{OH} of 3.5 volts and a load capacitance of 50 pF, this results in a current of 0.17 mA per MHz per output. For a data bus cycle time of 10 MHz (equivalent to 5 MHz square waves), an octal device such as an FCT244 would draw a load capacitance charging current of $(8)(5)(.17) = 7.0 \text{ mA}$.

MULTIPLE OUTPUTS SWITCHING ADDED DELAY

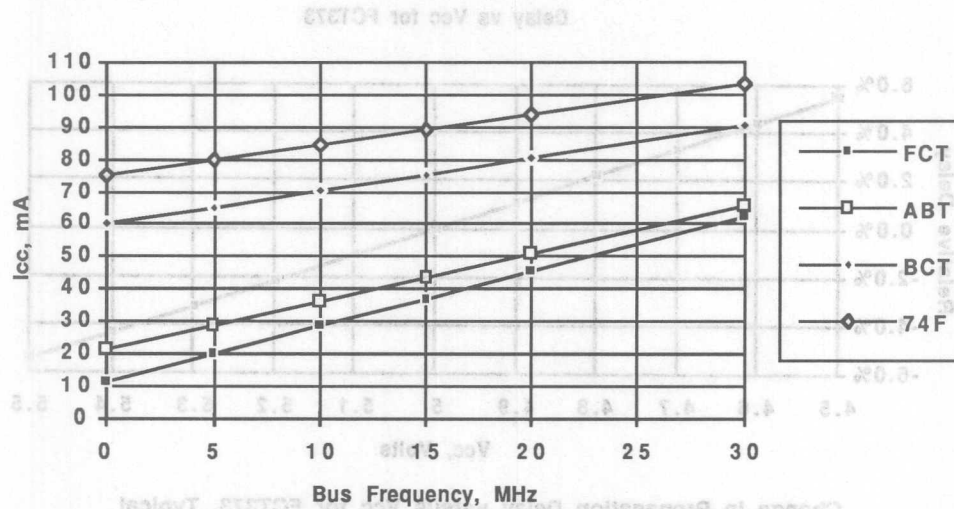
Package Added Delay

0.80ns	PDP
0.84ns	ZIP
0.72ns	SOIC
0.48 ns	QSO

FCT-T Family Characteristics

Comparison of Logic Families Based on Power Dissipation

A combined plot of current versus frequency for FCT-T versus various other logic families is shown below for a 244 device driving a bus with 50 pF load over a bus frequency range of zero to 30 MHz. Zero to 3.4 volt input swings are assumed so as to include ΔI_{CC} terms. Data for other logic families are taken from published data.



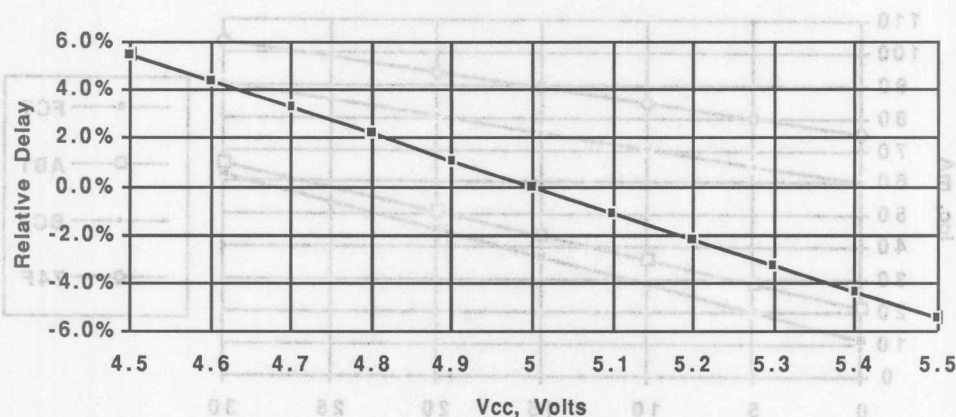
Current Consumption for 244 Buffers from Various Logic Families
8 Inputs Switching between 0 and 3.4 volts, 50 pF load

FCT-T Family Characteristics

Parameter Variations with Vcc

Propagation delay of FCT-T logic is slightly affected by changes in Vcc, as shown below. Increasing Vcc causes internal increase in transistor gate voltage. This increases lowers on resistance, decreasing internal RC time constants and total propagation delay.

Delay vs Vcc for FCT373



Change in Propagation Delay versus Vcc for FCT373, Typical

Ratings, Specifications and Waveforms

General Comments

In this section, the ratings, specifications and waveforms used in the data sheets are discussed to provide information on their meaning and how they are interpreted.

Absolute Maximum Ratings

The Absolute Maximum ratings define the limits of operation of the FCT-T devices. Operation beyond these limits may cause permanent damage to the device, i.e. it may no longer meet its specifications or may even cease to function.

The Supply Voltage rating defines the absolute maximum Vcc voltage that can be safely be applied to the device. The Supply Voltage rating of FCT-T is consistent with the equivalent ratings of other TTL devices, and system power distribution design must take these ratings into consideration for reliable operation. The Supply Voltage rating is determined by the internal breakdown voltage ratings of the device. High performance processes such as QCMOS™ strive to reduce device dimensions in order to increase speed. Reducing device dimensions also tends to reduce breakdown voltages. If Vcc to the device is taken too high, the internal device breakdown voltages may be exceeded, excessive current drawn, and devices may be permanently damaged because of the high resulting power dissipation and heat generated in the device. FCT-T devices typically have breakdown voltages well above the Supply Voltage rating listed, care must be taken that the Vcc supply does not go above this rating, even transiently.

The Output Voltage rating defines the maximum voltage that can be applied to an output when it is in its disabled state. Note that this voltage is independent of Vcc, and the output can go above Vcc. The device can be powered down and not load its outputs. This is because there is no clamp diode to Vcc or P channel pull up on the output.

The Input Voltage rating defines the maximum voltage that can be applied to an input. Note that this voltage is independent of Vcc, and the input can go above Vcc. The device can be powered down and not load its inputs. This is because there is no output clamp diode to Vcc.

The AC Input Voltage rating is an undershoot specification. Undershoot pulses of up to -3 volts can be tolerated without damage to the device. However, large undershoot pulses can cause significant clamp current and the energy of these pulses is dissipated in the device. If these pulses have a high duty cycle, the average power and the average current in the undershoot pulses can be significant and must be taken into account to insure that the DC Input Diode Current and the Maximum Power Dissipation ratings are not exceeded.

The DC Input Diode Current defines the rating of the input undershoot clamp diode. The average current from undershoot clamp pulses must be below this rating.

The DC Output Diode Current defines the rating of the output negative undershoot clamp diode. The average current from undershoot clamp pulses must be below this rating.

The DC Output Current Maximum Sink Per Pin defines the maximum DC output current that can be drawn per output to pull down an external load.

The Maximum Power Dissipation defines the maximum total power dissipation capability of the device. It represents a package power dissipation limit for the device, above which the die will overheat and be damaged. Note that the power dissipation limit includes power dissipated by the input clamp diodes as well as power from Vcc for driving internal circuitry and external capacitive loads.

FCT-T Family Characteristics

The Storage Temperature rating defines the maximum temperature that the packages may be subject to for long term storage. Long term storage above this temperature may cause degradation of the chip. This is a precautionary specification. Chips cannot be subjected to extremely high temperatures, significantly above the Storage Temperature rating, even if unpowered and be expected to work reliably thereafter.

Input and Output Capacitance

Each input and output pin has a capacitance associated with it. This capacitance is a function of the package and whether the pin in question is an input, output, or I/O pin. Pure input pins have the lowest capacitance. Output pins have higher capacitance because of the capacitance contributed by the relatively large output pull up and pull down transistors. Some devices, such as the FCT245, have pins which are termed I/O, or input/output. These pins have the same capacitance as output pins because the capacitance of the output driver transistors is present when these pins are in the input mode. Some devices, such as the FCT244, have I/O capacitance on all pins even though it has many dedicated inputs. This is because the FCT244 and FCT245 are derived from the same design, and the FCT244 inputs are actually I/O pins even though the output drivers are never enabled on these pins.

DC Electrical Characteristics

The DC Electrical Specifications define the input requirements for valid operation, output specifications during valid operation and responses to applied signals such as leakage currents, clamp voltages and output resistance.

V_{Ih} defines the minimum DC input voltage for a TTL high. Typical TTL high voltages applied to inputs are 3.5 to 5.0 volts. V_{Il} defines the maximum DC input voltage for a TTL low. Typical TTL low voltages applied to inputs are 0.0 to 0.5 volts. Note that the AC characteristics are guaranteed for input switching values of 3.0 volts for a TTL high and 0.0 volts for a TTL low.

ΔV_t defines the typical input hysteresis. This is the difference in input threshold voltages for low-to-high and high-to-low input transitions. This specification guarantees that there is some hysteresis and gives its typical value.

I_{Ih} and I_{Il} define the maximum input leakage current; I_{oz} defines the maximum output off state leakage current. The maximum input or output leakage is $\pm 5 \mu A$, and a typical value is 1-5 nanoamperes at 25 °C.

I_{os} defines the minimum output short circuit current for an output being driven to a TTL high. This is the minimum current sourced by the device when an output is grounded and insures that the device has sufficient current to charge high capacitance loads in low-to-high transitions.

I_{ors} defines the minimum output short circuit current for a resistor output being driven to a TTL low. This is the minimum pull down current by the device when an output is at 2.0 volts and insures that the device has sufficient current to charge high capacitance loads in high-to-low transitions. It also intended to indirectly guarantee that the output structure is a high current driver in series with a 25Ω resistor, rather than a weakened output which has a 25Ω resistance at low current but is unable to drive the currents required for high capacitance loads.

V_{ic} defines the input undershoot clamp voltage for a specified input current. It guarantees that the input undershoot clamp is sufficiently low impedance to provide useful clamping action.

V_{oh} defines the minimum output voltage for a TTL high. This is specified under two conditions: low current and high current. The low current specification defines the typical TTL high output level for the light loads seen in typical designs. The high current specification defines the minimum voltage under high loading, and specifications are given for military and commercial conditions.

FCT-T Family Characteristics

V_{OL} defines the maximum output voltage for a TTL low. This is specified under two conditions: standard and resistor output. The standard output specification is for conventional output, and specifications are given for military and commercial conditions. It indicates the drive capability of the output. The resistor output V_{OL} specification is for 25Ω resistor output devices under moderate DC loading.

R_{OUT} defines the range of resistance values for resistor output devices. It is guaranteed over voltage and temperature. This is an incremental resistance measured at the test current. The resistance is calculated as (V_{OUT} at 12 mA - V_{OUT} at 0 mA) divided by (12 mA - 0 mA).

Recommended Operating Conditions

The DC Electrical Characteristics define the limits of operation for the device. The recommended operating conditions are stated at the top of the DC Electrical Characteristics and Switching Characteristics specifications. The recommended operating conditions are those the parts are expected to encounter in normal operation. The switching characteristics are guaranteed under these conditions. The recommended operating conditions for FCT-T logic cover operating temperatures of 0 to 70 °C for commercial and -55 to + 125 °C for military temperature range parts and a nominal V_{CC} voltage of 5.0 volts with an operating range of within ±10% of this value (i.e. 4.5 to 5.5 volts).

Power Supply Characteristics

The Power Supply Characteristics defines the method for calculating the current drawn by the device from V_{CC} during operation. This current has several components which combine to form the total current. The Power Supply Characteristics specifies these components and how they combine to form the total.

There are four sources of power supply current, I_C, in FCT-T devices. They are: quiescent current, input buffer current, internal switching current, and load capacitance drive current.

I_{CC} is the quiescent current of QSI FCT-T and is the current drawn when the device is disabled and not switching. It is the DC standby current.

ΔI_{CC} is the current the TTL input buffers draw when their inputs are between approximately 0.5 volts and 4.0 volts. The ΔI_{CC} specification defines the maximum amount of current drawn per buffer when the buffer input is at a TTL high of 3.4 volts.

Q_{CCD} is the internal current CMOS logic draws when it switches. The charge transfer per switching event results in a frequency dependent current, specified in mA per MHz.

Note that the Q_{CCD} term does not include any current required by switching an external capacitive load. This current is a function of the V_{OH} of the device, the load capacitance and the frequency of the charge/discharge cycle. For QSI FCT-T logic with a typical V_{OH} of 3.5 volts, this term is 0.35 mA per MHz per 100 pF of load capacitance.

I_C, the total current is the sum of these components. It is calculated as shown below.

FCT-T Family Characteristics

Power Supply Current Calculation

The following shows how to calculate the worst case power supply current, I_c , for typical operating conditions:

Term	Description
$I_c = I_{cc}$	Quiescent current
$+ \Delta I_{cc} \times N \times d$	Input Buffer current for inputs at 3.4 volts
$+ Q_{ccd} \times F \times (M + 0.5 \times P)$	Internal switching current, per MHz
$+ 0.35 \times F \times C / 100 \times S$	External capacitive load current, per MHz, per pF

Where:

I_c	= Total Vcc current
I_{cc}	= Quiescent Current
ΔI_{cc}	= Input Buffer Current for Input at 3.4 Volts, per input
N	= Number of Inputs @ TTL High, 3.4 Volts
d	= Duty cycle at TTL High

Q_{ccd} = Internal Switching Current, mA per MHz

F = Switching Frequency, MHz

M = Number of non-clock inputs switching

P = Number of clock inputs switching

C = Load Capacitance in pF

S = Number of outputs switching while driving load capacitance, C

Example: FCT244, 8 inputs switching at 5 MHz (10 MHz bus data rate) @ 50% duty cycle,
8 enabled outputs, 50 pF loads

Term	Description
$I_c = (1.5)$	Quiescent current
$+ (2.5)(8)(0.5)$	Input Buffer current for inputs at 3.4 volts
$+ (0.25)(5)(8)$	Internal switching current, per MHz
$+ (0.35)(5)(50/100)(8)$	External capacitive load current, per MHz, per pF

$$I_c = 1.5 + 10 + 10 + 7$$

$$I_c = 28.5 \text{ mA Total Current}$$

Switching Characteristics

The Switching Characteristics, often called the AC Characteristics, define the propagation delay characteristics of the device. There are usually several options, called speed grades, for each device. These options are indicated by a suffix: "A", "B", "C", etc. The slowest speed grade may have no suffix letter. These specifications correspond directly to the original 74F series specifications which FCT-T logic was to meet. Higher letter suffixes refer to progressively faster speed grades, i.e. parts which have lower propagation delay.

Propagation Delay Specifications: t_{PHL} , t_{PLH}

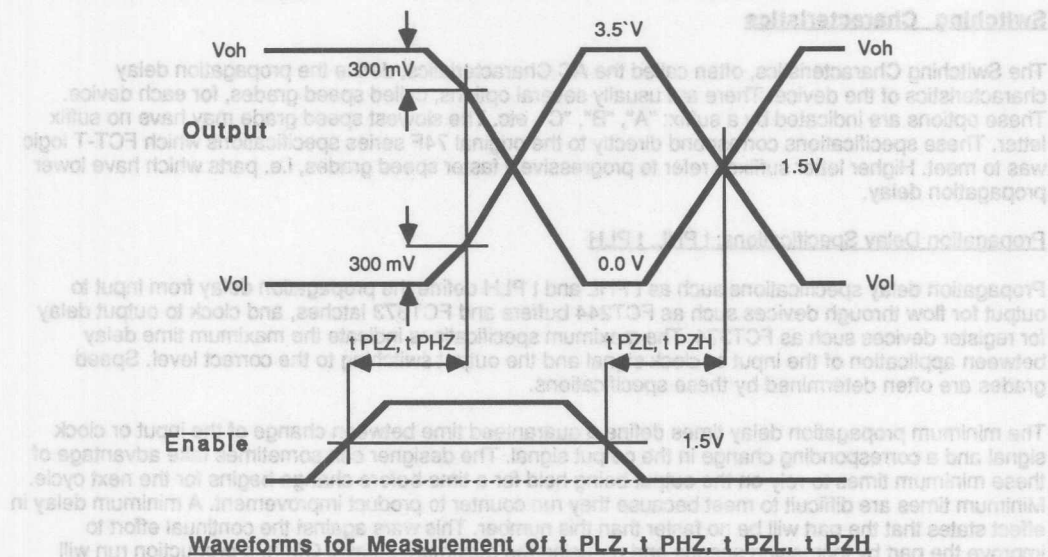
Propagation delay specifications such as t_{PHL} and t_{PLH} define the propagation delay from input to output for flow through devices such as FCT244 buffers and FCT373 latches, and clock to output delay for register devices such as FCT374. The maximum specifications indicate the maximum time delay between application of the input or clock signal and the output switching to the correct level. Speed grades are often determined by these specifications.

The minimum propagation delay times define a guaranteed time between change of the input or clock signal and a corresponding change in the output signal. The designer can sometimes take advantage of these minimum times to rely on the output being held for a time before change begins for the next cycle. Minimum times are difficult to meet because they run counter to product improvement. A minimum delay in effect states that the part will be no faster than this number. This wars against the continual effort to improve the part by increasing speeds and reducing the maximum delays. Often, a production run will produce parts faster than the required specifications. This is a benefit for guaranteed maximum specifications; it could be a problem for guaranteed minimums. As a result, minimum specifications are typically set by the fastest speed grade and applied to all slower speed grades.

Three State Propagation Delay Specifications: t_{PZH} , t_{PZL} , t_{PHZ} , t_{PLZ}

Three state specifications cover two conditions: going from the high impedance (high-Z) condition to the low impedance, on state condition, and going from the low impedance, on state condition to the high impedance (high-Z) condition. In the high-Z to low-Z case, propagation delay measurements are done in the same manner as any other: the output must settle to the correct logic high or low state before the stated maximum time, t_{PZH} or t_{PZL} .

In the low-Z to high-Z case, the output must be in the high-Z condition by the stated maximum time, t_{PHZ} or t_{PLZ} . Special measurement must be done to detect the high-Z condition. Since the high-Z condition means the output is not driven, the high-Z condition is detected by using an external resistor load network to drive the output away from the previous high or low logic state to a level determined by the load network. The output will start to move to this level when the output has turned off. This is detected by a change in the output level away from the previous high or low. The output is defined as being in the high-Z state when the output moves from its prior high or low state by 300 millivolts. This is shown in the waveform diagrams below. Note that this specification is usually guaranteed by design, verified by device characterization and not tested in production.



Waveforms for Measurement of t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}

Setup and Hold Time and Clock Pulse Width Specifications: t_S , t_H , t_W

Setup and hold times define a period during which a data or control input must be stable relative to a clock edge such as the falling (high-to-low) edge of a latch enable signal for an FCT373 latch or the rising (low-to-high) edge of a clock for an FCT374 register. Setup time, t_S , is defined as stable time before the clocking edge; hold time, t_H , is defined as the stable time after the clocking edge. During this period of setup time plus hold time, the input signal is sampled by the internal logic. The sampling point is guaranteed to be somewhere within this time period. The input signal must be stable during this period for it to be interpreted as a valid high or low. If it is not stable, the input circuitry will arbitrarily interpret it as a high or a low depending on when the signal is sampled internally.

The clock pulse width, t_W , defines the minimum high or low time of the clock signal for a counter or register. It also determines the maximum frequency of the clock as equal to the inverse of the minimum clock period which is twice t_W . For example, the 74FCT374C has a t_W of 4 ns. The minimum clock period is therefore 8 ns, and the guaranteed operating frequency is 125 MHz, minimum.

FCT-T Family Characteristics

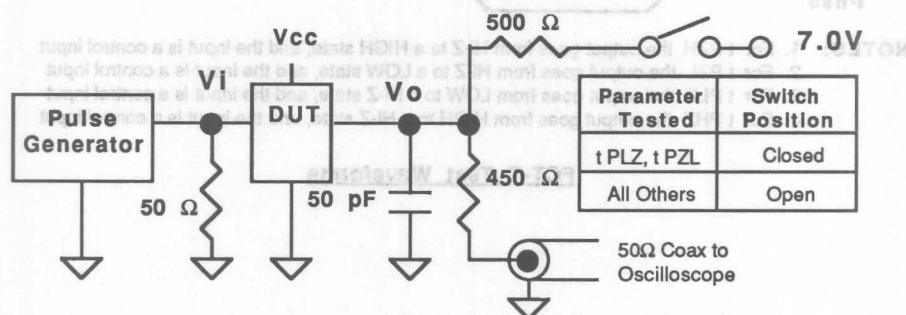
AC Test Conditions

AC test conditions are concerned with propagation delays at outputs relative to applied signals. FCT-T is tested using industry standard test signals. Input signals transition between levels of 0.0 volts for a logic low to 3.0 volts for a logic high with a transition time of 2.5 nanoseconds measured from the 10% to 90% points of the signal transition. Rise and fall times of 1 ns are used to test minimum pulse widths such as clock width, t_W . Propagation delay is measured from the time the input crosses 1.5 volts to the time the output crosses 1.5 volts. Propagation delay is tested with one output switching.

AC Test Circuitry

The AC test circuitry is shown below. This test circuitry is an industry standard for FCT-T logic and many other high performance TTL logic families. Inputs under test are driven by a pulse generator with an output impedance of 50 ohms. Outputs are loaded with 50 picofarads and 500 ohms to ground except for three state tests. The 500 ohm resistor to ground is typically used as a part of a 10:1 probe for an oscilloscope used to measure the output. The 10:1 probe consists of a 450 ohm resistor feeding into a 50 ohm coax cable to the oscilloscope. This provides a 10:1 probe with no appreciable capacitive loading by the 450 ohm resistor. This is the preferred scheme for correlation to QSI test data.

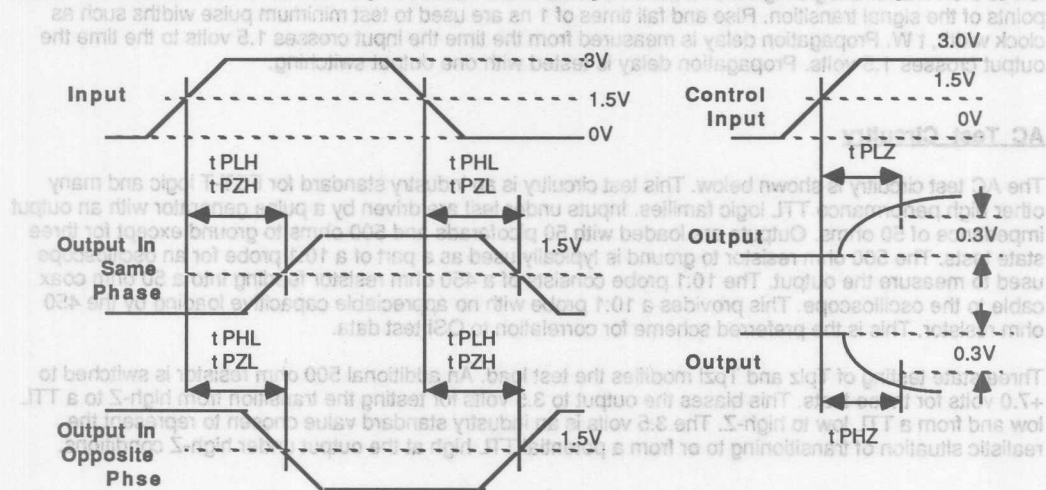
Three state testing of T_{PLZ} and T_{PZL} modifies the test load. An additional 500 ohm resistor is switched to +7.0 volts for these tests. This biases the output to 3.5 volts for testing the transition from high-Z to a TTL low and from a TTL low to high-Z. The 3.5 volts is an industry standard value chosen to represent the realistic situation of transitioning to or from a potential TTL high at the output under high-Z conditions.



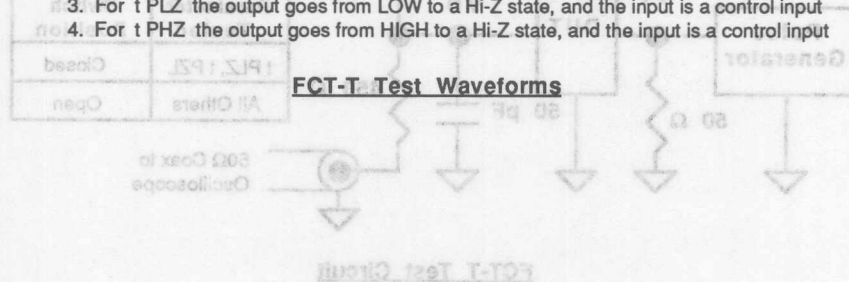
FCT-T Test Circuit

AC Test Waveforms

General waveforms are shown below for testing all input to output delays. Outputs are shown for normal and inverted signal phases, as determined by the logic function being tested. Three state disable test waveforms are also shown, indicating the 300 millivolt change in level used to detect the high-Z condition.



- NOTES:**
1. For t_{PZH} the output goes from Hi-Z to a HIGH state, and the input is a control input
 2. For t_{PZL} the output goes from Hi-Z to a LOW state, and the input is a control input
 3. For t_{PLZ} the output goes from LOW to a Hi-Z state, and the input is a control input
 4. For t_{PHZ} the output goes from HIGH to a Hi-Z state, and the input is a control input





High Speed CMOS 8-bit Bus Interface Register Transceivers

QS29FCT52T
QS29FCT53T

QS29FCT2052T
QS29FCT2053T

FEATURES/BENEFITS

- Pin and function compatible to the Am2952/3 29FCT52/3 and 29FCT52/3T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 2952T, 2953T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A, B and C speed grades with 5.5ns tPD for C
- IOL = 64 mA Com., 48 mA Mil.

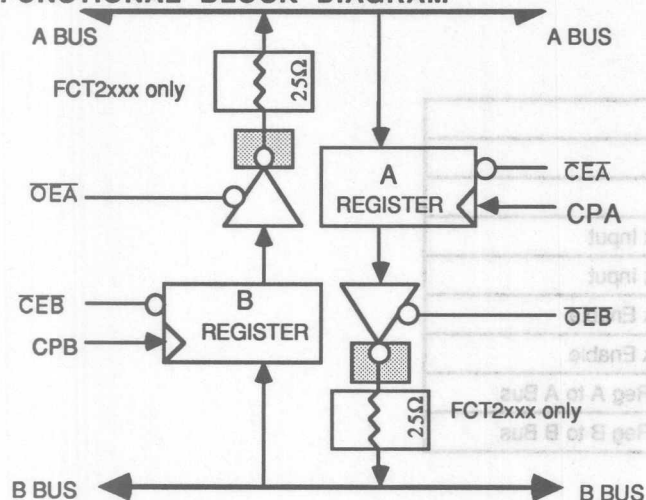
FCT-T 2052T, 2053T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B and C speed grades with 5.5ns tPD for C speed guaranteed with 50pF loads

DESCRIPTION

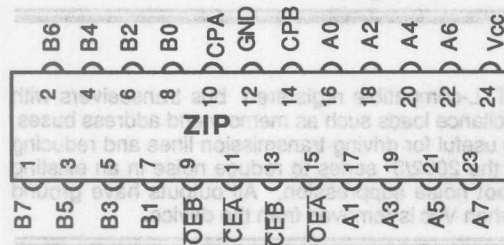
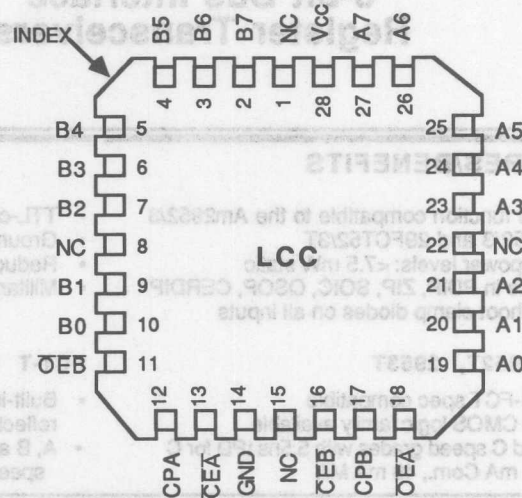
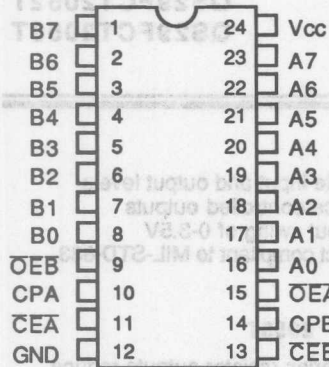
The QS29FCT52T/3T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2052/3 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2052/3 series parts can replace the 2052/3 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression, and will not load an active bus when VCC is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PINOUTS

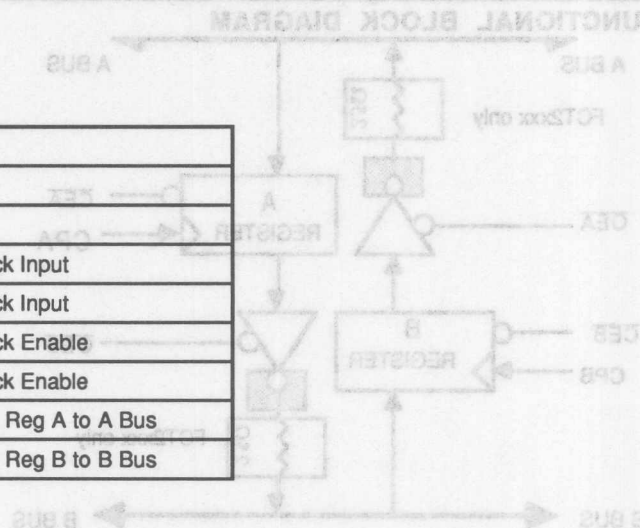
PDIP, SOIC, QSOP



ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
A7-A0	I/O	A Bus
B7-B0	I/O	B Bus
CPA	I	Register A Clock Input
CPB	I	Register B Clock Input
CEA	I	Register A Clock Enable
CEB	I	Register B Clock Enable
OEA	I	Output Enable, Reg A to A Bus
OEB	I	Output Enable, Reg B to B Bus



FUNCTION TABLES - QS29FCT52/3, 2052/3

Inputs						Outputs	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	$\overline{OEA}$	$\overline{OEB}$	A1-8	B1-8
X	X	X	X	H	L	Z	Breg
X	X	X	X	L	H	Areg	Z
X	X	X	X	H	H	Z	Z
X	X	X	X	L	L	Areg	Breg

Inputs				Registers	
CPA	CPB	$\overline{CEA}$	$\overline{CEB}$	A1-8	B1-8
X	X	H	H	Hold	Hold
↑	X	L	H	Load	Hold
X	↑	H	L	Hold	Load
X	↑	L	L	X	Load
↑	X	L	L	Load	X

↑ = Low to High Transition
 H = HIGH
 L = LOW
 Z = High Impedance
 X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
-----	4	4	5	7	pF
-----	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$, $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18\text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$ $I_{oh} = 12\text{ mA}$ (MIL) $I_{oh} = 15\text{ mA}$ (COM)	2.4 2.4	- -	- -	Volts
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$ $I_{ol} = 48\text{ mA}$ (MIL) $I_{ol} = 64\text{ mA}$ (COM)	- -	- -	0.55 0.55	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12\text{ mA}$ (MIL) $I_{ol} = 12\text{ mA}$ (COM)	- -	- -	0.50 0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12\text{ mA}$ (MIL) $I_{ol} = 12\text{ mA}$ (COM)	21 24	28 28	38 35	Ω

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}$, freq = 0 $0V \leq V_{in} \leq 0.2V$ or $V_{cc} - 0.2V \leq V_{in} \leq V_{cc}$	-	1.5	mA
ΔI_{cc}	Supply Current per Input @ TTL HIGH	$V_{cc} = \text{MAX}$, $V_{in} = 3.4V$, freq = 0 (2)	-	2.0	mA
Q_{ccd}	Supply Current per input per mHz	$V_{cc} = \text{MAX}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i = 3.4V$)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

Am	-	-	20	$V_{cc} = \text{MIN}$, $V_o = 2.0V$	Current Drive FCT3XXX (250)	for
Vic	-	-	-	$V_{cc} = \text{MIN}$, $I_{in} = 12 \text{ mA}$ (2)	Input Clamp Voltage	for
Voh	-	-	2.4	$I_{oh} = 12 \text{ mA}$ (MIL) $V_{cc} = \text{MIN}$	Output HIGH Voltage FCT3XXX & FCT3XXX	for
Vol	-	-	0.55	$I_{ol} = 12 \text{ mA}$ (COM) $V_{cc} = \text{MIN}$	Output LOW Voltage FCT3XXX	for
	0.55	-	0.55	$I_{ol} = 48 \text{ mA}$ (MIL) $V_{cc} = \text{MIN}$	Output LOW Voltage FCT3XXX	for
	0.55	-	0.55	$I_{ol} = 64 \text{ mA}$ (COM) $V_{cc} = \text{MIN}$	Output LOW Voltage FCT3XXX (250)	for
	0.55	-	0.55	$I_{ol} = 12 \text{ mA}$ (MIL) $V_{cc} = \text{MIN}$	Output LOW Voltage FCT3XXX (250)	for
	0.55	-	0.55	$I_{ol} = 12 \text{ mA}$ (COM) $V_{cc} = \text{MIN}$	Output LOW Voltage FCT3XXX (250)	for
Rout	-	-	24	$I_{ol} = 12 \text{ mA}$ (MIL) $V_{cc} = \text{MIN}$	Output Resistance FCT3XXX (250)	for
	38	38	38	$I_{ol} = 12 \text{ mA}$ (COM) $V_{cc} = \text{MIN}$	Output Resistance FCT3XXX (250)	for

- Notes:
1. Typical values indicate $V_{cc} = 2.0V$ and $T_A = 25^\circ C$.
 2. Not more than one output should be shorted and the duration is 25 seconds.
 3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 $C_{load} = 50\text{ pF}$, $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Notes (1)	2952/3A 292052A 292053A		2952/3B 292052B 292053B		2952/3C 292052C 292053C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay CP to Ai,Bi, 52/3	Com	2	10	2	6.5	2	5.8	ns
		MII	2	11	2	7.2	0	6.8	
	Propagation Delay CP to Ai,Bi, 2052/3	Com	2	10	2	6.5	2	5.8	
		MII	2	11	2	7.2	0	6.8	
t_{PZH} t_{PZL}	Output Enable Time OE to Ai,Bi, 52/3	Com	1.5	10.5	1.5	6.5	1.5	6.5	
		MII	1.5	13	1.5	7.5	1.5	7.5	
	Output Enable Time OE to Ai,Bi, 2052/3	Com	1.5	10.5	1.5	7.0	1.5	7.0	
		MII	1.5	13	1.5	7.5	1.5	7.5	
t_{PHZ} t_{PLZ}	Output Disable Time OE to Ai,Bi	Com	2	10	2	5.5	1.5	5.5	
		MII	2	11	2	6.5	1.5	6.5	
t_S	Data Setup Time Ai,Bi to CP	Com	2		2		2		
		MII	2.5		2		2		
t_H	Data Hold Time Ai,Bi to CP	Com	2		1.5		1.5		
		MII	2		1.5		1.5		
t_{SCE}	Clock Enable Setup Time, $\overline{CE}$ to CP	Com	2		2		2		
		MII	2		2		2		
t_{HCE}	Clock Enable Hold Time, $\overline{CE}$ to CP	Com	2		2		2		
		MII	2		2		2		
t_W	Clock Pulse Width HIGH or LOW	Com	3		3		3		
		MII	3		3		3		

Notes:

- 1) See Test Circuit and Waveforms. Minimums Guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V}$ Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V}$ to 10V
 Load = 50 pF, $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Notes	(1)				Unit
			Min	Max	Min	Max	
t _{PHL} t _{PLH}	Propagation Delay CP to A/B, 50%	Com	2	10	2	8.5	ns
		Min	2	11	2	7.5	
	Propagation Delay CP to A/B, 50%	Com	2	10	2	8.5	
		Min	2	11	2	7.5	
t _{PSH} t _{PSL}	Output Enable Time OE to A/B, 50%	Com	1.5	10.5	1.5	8.5	
		Min	1.5	13	1.5	7.5	
	Output Enable Time OE to A/B, 50%	Com	1.5	10.5	1.5	7.0	
		Min	1.5	13	1.5	7.5	
t _{PHZ} t _{PLZ}	Output Disable Time OE to A/B	Com	2	10	2	8.5	
		Min	2	11	2	8.5	
t _S	Data Setup Time A/B to CP	Com	2		2		
		Min	2.5		2		
t _H	Data Hold Time A/B to CP	Com	2		1.5		
		Min	2		1.5		
t _{SE}	Clock Enable Setup Time, OE to CP	Com	2		2		
		Min	2		2		
t _{HE}	Clock Enable Hold Time, OE to CP	Com	2		2		
		Min	2		2		
t _W	Clock Pulse Width HIGH or LOW	Com	3		3		
		Min	3		3		

Notes:
 (1) See Test Circuit and Waveforms. Minimums Guaranteed but not tested.
 (2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS Multilevel Pipeline Registers

QS29FCT520T
QS29FCT521T

QS29FCT2520T
QS29FCT2521T

FEATURES/BENEFITS

- Pin and function compatible to the Am29520
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip

- TTL-compatible input and output levels
- CMOS power levels: <7.5 mW static
- Undershoot clamp diodes on all inputs
- Military product compliant to MIL-STD-883

FCT-T520T/1T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A, B & C speed grades with 6ns tPD for C
- I_{OL} = 48 mA Com., 32 mA Mil.

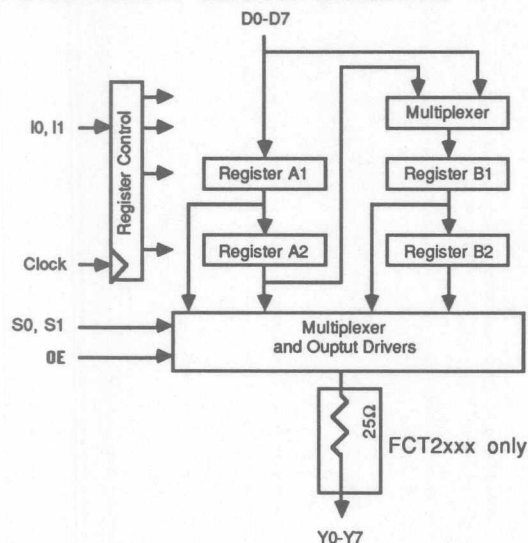
FCT-T 2520T/1T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and B speed grades with 7.5ns tPD for B
- I_{OL} = 12mA Com.

DESCRIPTION

The QS29FCT520AT/BT and QS29FCT521AT/BT provide four 8-bit registers useful for temporary storage and for stage delays in pipelined systems. The four registers may be configured as a dual 2-level or single 4-level shift register pipeline. A single 8-bit input is provided, and any of the four registers may be selected for gating to the single 8-bit output. The 520 and 521 differ only in how the registers are loaded in the dual 2-rank mode, as shown in the function tables. The QS29FCT520/1 are pin and function compatible with the Am29520/1 bipolar parts, except for higher speed and significantly lower power.

FUNCTIONAL BLOCK DIAGRAM

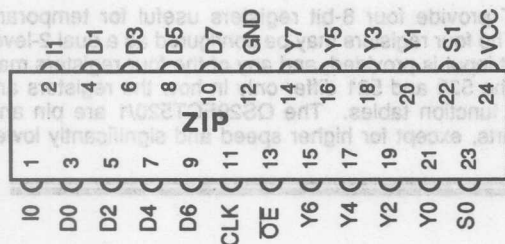
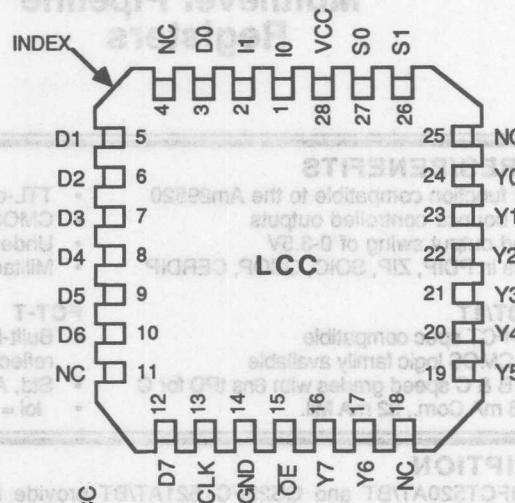
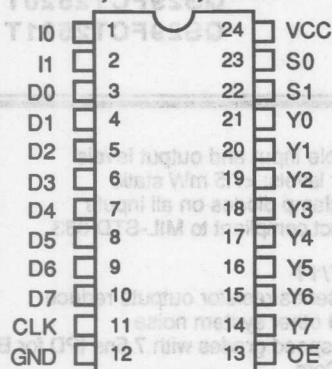


PIN DESCRIPTIONS

Name	I/O	Function
D0-D7	I	Data Input
Y0-Y7	O	Data Outputs - True State
I0, I1	I	Register Load Control
S0, S1	I	Register Output Select
CLK	I	Clock Pulse
OE	I	Output Enable

PINOUTS

PDIP, SOIC, QSOP



PIN DESCRIPTIONS

Name	I/O	Function
D0-D7	I	Data Inputs
Y0-Y7	O	Data Outputs - Three State
I0, I1	I	Register Load Control
S0, S1	I	Register Output Select
CLK	I	Clock Pulse
$\overline{OE}$	I	Output Enable

FUNCTION TABLES - QS29FCT520/1, 2520/1

REGISTER LOAD CONTROL

PART NO	Register Control Code			
	I1,0 = LL = 0	I1,0 = LH = 1	I1,0 = HL = 2	I1,0 = HH = 3
FCT520				Hold Data
FCT521				Hold Data

REGISTER OUTPUT SELECTION

S1	S0	OE	YI	Register to Y0-Y7
L	L	L	Data	B2
L	H	L	Data	B1
H	L	L	Data	A2
H	H	L	Data	A1
X	X	H	Hi-Z	Outputs Disabled

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-11, 13, 22, 23	4	4	5	7	pF
14-21	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

REGISTER OUTPUT SELECTION

Register to Y0-Y7	YI	OE	S0	S1
S2	Data	L	L	L
S1	Data	L	H	L
A2	Data	L	L	H
A1	Data	L	H	H
Outputs Disabled	H-Z	H	X	X

QSFCT29520T, 29521T, 2520T, 2521T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$, $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ i_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
i_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
i_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $i_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$i_{oh} = 12 \text{ mA (MIL)}$	2.4	-	Volts
			$i_{oh} = 15 \text{ mA (COM)}$	2.4	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$i_{ol} = 32 \text{ mA (MIL)}$	-	-	
			$i_{ol} = 48 \text{ mA (COM)}$	-	-	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$i_{ol} = 12 \text{ mA (MIL)}$	-	-	
			$i_{ol} = 12 \text{ mA (COM)}$	-	-	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$i_{ol} = 12 \text{ mA (MIL)}$	21	28	Ω
			$i_{ol} = 12 \text{ mA (COM)}$	24	28	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_I = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

V _{oh}	Output HIGH Voltage FCT3XX & FCT3XX	V _{oh} = MIN	I _{oh} = 12 mA (MIL)	2.4	-	-
			I _{oh} = 18 mA (COM)	2.4	-	-
V _{ol}	Output LOW Voltage FCT3XX	V _{ol} = MIN	I _{ol} = 32 mA (MIL)	-	-	0.50
			I _{ol} = 48 mA (COM)	-	-	0.50
V _{cc}	Output LOW Voltage FCT3XX (SSD)	V _{cc} = MIN	I _{ol} = 12 mA (MIL)	-	-	0.50
			I _{ol} = 12 mA (COM)	-	-	0.50
R _{out}	Output Resistance FCT3XX (SSD)	V _{cc} = MIN	I _{ol} = 12 mA (MIL)	2.4	2.8	3.8
			I _{ol} = 12 mA (COM)	2.4	2.8	3.8

- Notes:
1. Typical values indicate V_{cc} = 5.0V and T_A = 25°C.
 2. Not more than one output should be shorted and the duration is 21 seconds.
 3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Cload = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes (1)	29FCT 520/1A 2520/1A		29FCT 520/1B 2520/1B		29FCT 520/1C 2520/1C		Unit
			Min	Max	Min	Max	Min	Max	
t CPD	Clock to Y Delay	COM	2	14	2	7.5	2	6	ns
		MIL	2	16	2	8	2	7	
t DY	S0,1 to Y Delay	COM	5	13	2.5	7.5	2	6	
		MIL	6	15	2	8	2	7	
t DS	Data to CLK Setup Time	COM	5		2.5		2.5		
		MIL	6		2.8		2.8		
t DH	Data to CLK Hold Time	COM	2		2		2		
		MIL	2		2		2		
t IS	I0,1 to CLK Setup Time	COM	5		4		4		
		MIL	6		4.5		4.5		
t IH	I0,1 to CLK Hold Time	COM	2		2		2		
		MIL	2		2		2		
t OZ	Output Disable Time OE to Y	COM	1.5	12	1.5	7	1.5	6	
		MIL	1.5	13	1.5	7.5	1.5	6	
t OE	Output Enable Time OE to Y	COM	1.5	15	1.5	7.5	1.5	6	
		MIL	1.5	16	1.5	8	1.5	7	
t CW	CLK Pulse Width, High or Low	COM	7		5.5		5.5		
		MIL	8		6		6		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0 \pm 15\%$, Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0 \pm 10\%$
 Load = 50 pF, Rise = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	29520T 2520T		29521T 2521T		29520T 2520T		29521T 2521T		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{CPD}	Clock to Y Delay	COM	2	14	2	7.5	2	8	2	8	ns
		MIL	2	16	2	8	2	7	2	7	
t _{DY}	20.1 to Y Delay	COM	2	13	2.5	7.5	2	8	2	8	ns
		MIL	2	15	2	8	2	7	2	7	
t _{DS}	Data to CLK Setup Time	COM	2		2.5		2.5		2.5		ns
		MIL	2		2.5		2.5		2.5		
t _{DH}	Data to CLK Hold Time	COM	2		2		2		2		ns
		MIL	2		2		2		2		
t _{IS}	10.1 to CLK Setup Time	COM	2		4		4		4		ns
		MIL	2		4.5		4.5		4.5		
t _{IH}	10.1 to CLK Hold Time	COM	2		2		2		2		ns
		MIL	2		2		2		2		
t _{OZ}	Output Disable Time OE to Y	COM	1.5	12	1.5	7	1.5	8	1.5	8	ns
		MIL	1.5	13	1.5	7.5	1.5	8	1.5	8	
t _{OE}	Output Enable Time OE to Y	COM	1.5	15	1.5	7.5	1.5	8	1.5	8	ns
		MIL	1.5	16	1.5	8	1.5	7	1.5	7	
t _{OW}	CLK Pulse Width, High or Low	COM	2	7	2.5		2.5		2.5		ns
		MIL	2	8	2.5		2.5		2.5		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS 1-of-8 Decoders

QS54/74FCT138T
QS54/74FCT238T

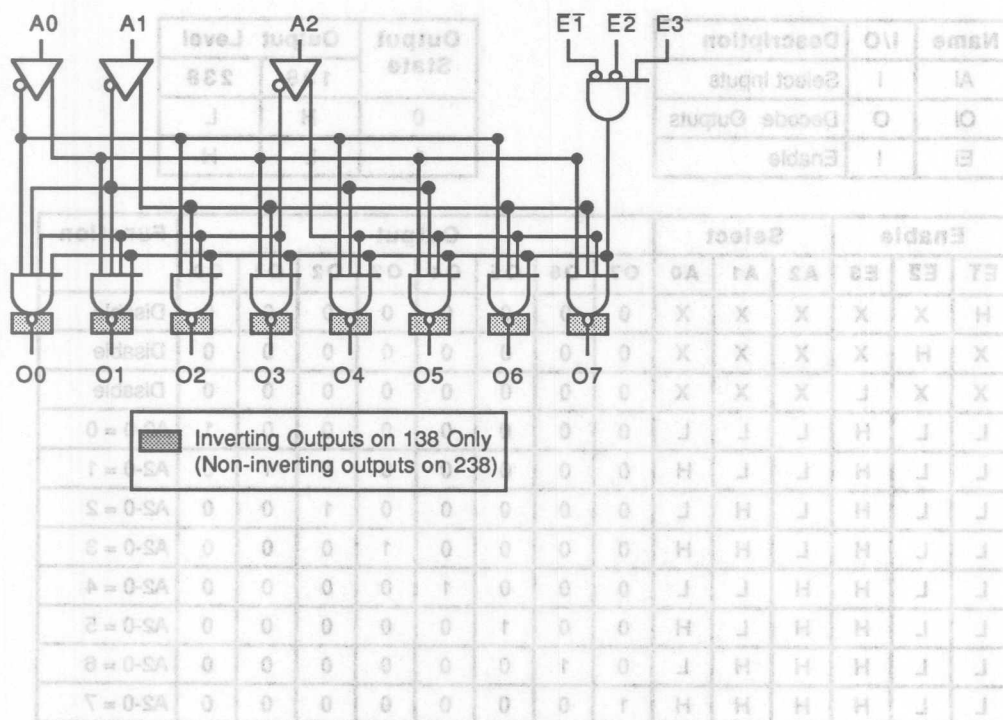
FEATURES/BENEFITS

- QSFCT138A faster than 74F
- $I_{OL}=48$ mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Mil product compliant with MIL-STD 883, Class B
- QSFCT238T has positive active outputs
- CMOS power levels < 7.5 mW static
- Available in PDIP, ZIP, SOIC, CERDIP, LCC
- JEDEC standard pinouts

DESCRIPTION

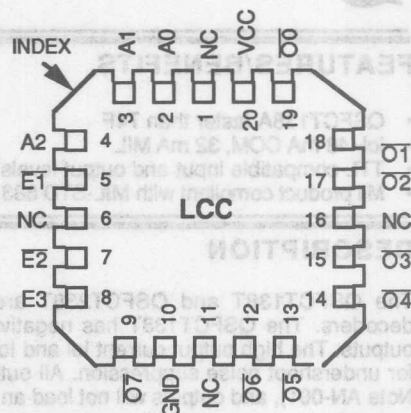
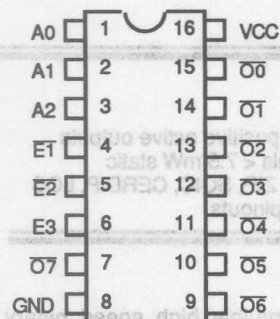
The QSFCT138T and QSFCT238T are high speed CMOS TTL-compatible high speed binary decoders. The QSFCT138T has negative active outputs, and the QSFCT238T has positive active outputs. The high output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

PDIP, SOIC



ALL PINS TOP VIEW

* For ZIP pinout contact factory.

Name	I/O	Description
Ai	I	Select Inputs
Oi	O	Decode Outputs
Ei	I	Enable

Output State	Output Level	
	138	238
0	H	L
1	L	H

Enable			Select			Output								Function
E1	E2	E3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0	
H	X	X	X	X	X	0	0	0	0	0	0	0	0	Disable
X	H	X	X	X	X	0	0	0	0	0	0	0	0	Disable
X	X	L	X	X	X	0	0	0	0	0	0	0	0	Disable
L	L	H	L	L	L	0	0	0	0	0	0	0	1	A2-0 = 0
L	L	H	L	L	H	0	0	0	0	0	0	1	0	A2-0 = 1
L	L	H	L	H	L	0	0	0	0	0	1	0	0	A2-0 = 2
L	L	H	L	H	H	0	0	0	0	1	0	0	0	A2-0 = 3
L	L	H	H	L	L	0	0	0	1	0	0	0	0	A2-0 = 4
L	L	H	H	L	H	0	0	1	0	0	0	0	0	A2-0 = 5
L	L	H	H	H	L	0	1	0	0	0	0	0	0	A2-0 = 6
L	L	H	H	H	H	1	0	0	0	0	0	0	0	A2-0 = 7

QS74FCT138T, QS74FCT238T

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V

DC Output Voltage V_O -0.5V to 7.0V

DC Input Voltage V_i -0.5V to 7.0V

AC Input Voltage (for a pulse width ≤ 20 ns).....-3.0V

DC Input Diode Current with $V_I < 0$-20 mA

DC Output Diode Current with $V_O < 0$-50 mA

DC Output Current Max. sink current/pin..... 120 mA

N=Number of Outputs, M=Number of inputs

Maximum Power Dissipation..... 0.5 watts

T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

PIns	SOIC	QSOP	PDIP,LCC	ZIP	Units
1-3	4	4	5	7	pF
7,9-12	6	6	7	9	pF
4-6,13-15	8	8	9	10	pF

Note: Capacitance is characterized but not tested

QS74FCT138T, QS74FCT238T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA (MIL)}$	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA (COM)}$	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 48 \text{ mA (COM)}$	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 12 \text{ mA (COM)}$	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	21	28	38	Ω
			$I_{ol} = 12 \text{ mA (COM)}$	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

4

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, V_{cc} = 5.0V ± 5% Military TA = -55°C to 125° C, V_{cc} = 5.0V ± 10%
C_{load} = 50 pF, R_{load} = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	138, 238		138A 238A		138C 238C		138D 238D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} t _{PLH}	Propagation Delay A _i to O _i	COM	1.5	9	1.5	5.8	1.5	5.0	1.0	4.0	ns
		MIL	1.5	12	1.5	7.8	1.5	7.0			
t _{PHLE} t _{PLHE}	Propagation Delay E _i to O _i	COM	1.5	8	1.5	5.9	1.5	5.0	1.0	4.0	
		MIL	1.5	12	1.5	8.0	1.5	7.0			

Notes:

1. See test circuits and wave forms.
2. This parameter is guaranteed but not tested.

QS74FCT138T, QS74FCT238T

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, I _{in} = 0 0V _{in} /12.0V or V _{cc} = 0.2V _{in} /2V _{cc}	-	1.5	mA
I _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4V, I _{in} = 0 (2)	-	5.0	mA
I _{cc}	Supply Current per Input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. For TTL driven input (V_{in} = 3.4V).
3. For I_{cc} per mHz is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. It can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, V_{cc} = 5.0V±5% Military TA = -55°C to 125°C, V_{cc} = 5.0V±10%
 Load = 50 pF, R_{load} = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	138A, 238A	138B, 238B	138C, 238C	138D, 238D	Unit
t _{PHL} A to Q	Propagation Delay	COM	1.5	1.5	1.5	1.5	ns
			1.5	1.5	1.5	1.5	ns
t _{PLH} Q to A	Propagation Delay	COM	1.5	1.5	1.5	1.5	ns
			1.5	1.5	1.5	1.5	ns
t _{PHL} B to Q	Propagation Delay	COM	1.5	1.5	1.5	1.5	ns
			1.5	1.5	1.5	1.5	ns
t _{PLH} Q to B	Propagation Delay	COM	1.5	1.5	1.5	1.5	ns
			1.5	1.5	1.5	1.5	ns

- Notes:
 1. See test circuits and wave forms.
 2. This parameter is guaranteed but not tested.

Q

High Speed CMOS Dual Binary 1-of-4 Decoders

QS54/74FCT139T
QS54/74FCT239T

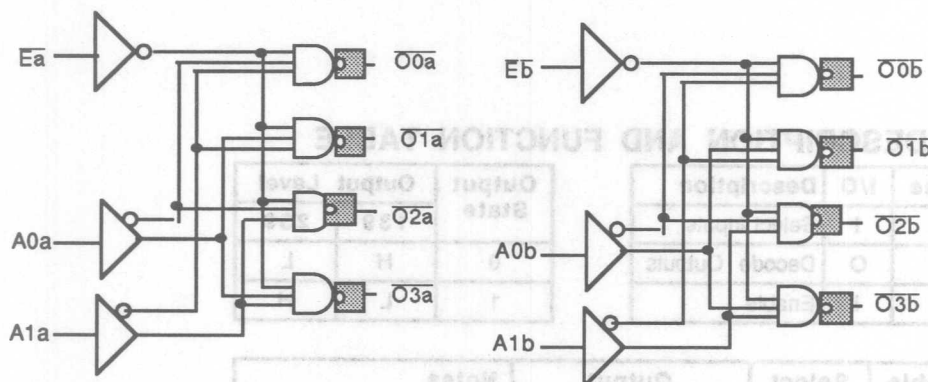
FEATURES/BENEFITS

- QSFCT139D with 4.0 ns prop. delay
- $I_{OL}=48$ mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Mil product compliant with MIL-STD 883, Class B
- QSFCT239T has positive active outputs
- CMOS power levels < 7.5 mW static
- Available in PDIP, ZIP, SOIC, Cerdip, LCC
- JEDEC standard pinouts

DESCRIPTION

The QSFCT139T and QSFCT239T are high speed CMOS TTL-compatible high speed binary decoders. The QSFCT139T has negative active outputs, and the QSFCT239T has positive active outputs. The high output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

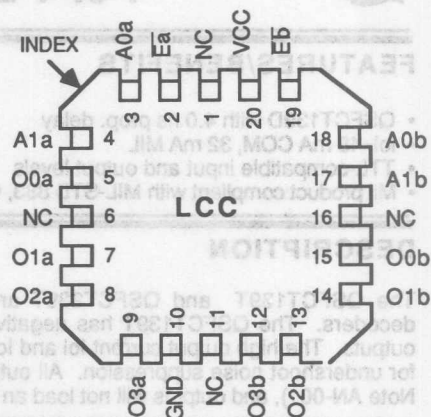
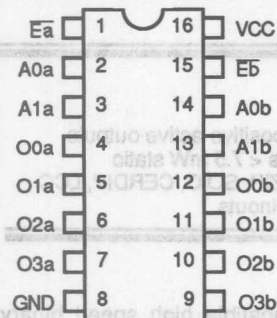
FUNCTIONAL BLOCK DIAGRAM



■ Inverting Outputs on 139 Only
(Non-inverting outputs on 239)

PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ALL PINS TOP VIEW

* For ZIP pinout call factory

PIN DESCRIPTION AND FUNCTION TABLE

Name	I/O	Description
Ai	I	Select Inputs
Oi	O	Decode Outputs
Ei	I	Enable

Output State	Output Level	
	139	239
0	H	L
1	L	H

Enable	Select		Output				Notes
Ea, Eб	A1	A0	O3	O2	O1	O0	
H	X	X	0	0	0	0	Disable Decode
L	L	L	0	0	0	1	A1-0 = 0
L	L	H	0	0	1	0	A1-0 = 1
L	H	L	0	1	0	0	A1-0 = 2
L	H	H	1	0	0	0	A1-0 = 3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-3	4	4	5	7	pF
7,9-12	6	6	7	9	pF
4-6,13-15	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^\circ\text{C}$.	
		Test Conditions	Typical Value
R_{out}	Output Resistance (25°C)	$V_{CC} = \text{MIN}$ $I_{OL} = 12\text{ mA (MIL)}$	38
		$I_{OL} = 12\text{ mA (COM)}$	38
V_{OL}	Output LOW Voltage (25°C)	$V_{CC} = \text{MIN}$ $I_{OL} = 12\text{ mA (MIL)}$	0.50
		$I_{OL} = 12\text{ mA (COM)}$	0.50
		$V_{CC} = \text{MIN}$ $I_{OL} = 32\text{ mA (MIL)}$	0.50
		$I_{OL} = 32\text{ mA (COM)}$	0.50
V_{OH}	Output HIGH Voltage (25°C)	$V_{CC} = \text{MIN}$ $I_{OH} = 12\text{ mA (MIL)}$	5.4
		$I_{OH} = 12\text{ mA (COM)}$	5.4

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^\circ\text{C}$.
2. Not more than one output should be shown and the duration is 21 seconds.
3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

- Notes:
1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
 2. Not more than one output should be shorted and the duration is ≤ 1 second.
 3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V ≤ Vin ≤ 0.2V or Vcc - 0.2V ≤ Vin ≤ Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin = 3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

4

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	139, 239		139A 239A		139C 239C		139D 239D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t PHL t PLH	Propagation Delay Ai to Oi	COM	1.5	9	1.5	5.8	1.5	5.0	1.0	4.0	ns
		MIL	1.5	12	1.5	7.8	1.5	7.0			
t PHLE t PLHE	Propagation Delay Ei to Oi	COM	1.5	9	1.5	5.9	1.5	5.0	1.0	4.0	
		MIL	1.5	12	1.5	8.0	1.5	7.0			

Notes:

1. See test circuits and wave forms.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, I _{in} = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} = 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4V, I _{in} = 0 (2)	-	5.0	mA
I _{cc} (Q)	Supply Current per Input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
 2. Per TTL driven input (VI=3.4V).
 3. For flip-flop I_{cc}(Q) is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or test capacitance. This parameter is guaranteed by design but not tested.
 4. It can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, V_{cc} = 5.0V ± 5%, Military TA = -55°C to 125°C, V_{cc} = 5.0V ± 10%,
 Load = 50 pF, Rise/Fall = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	139, 239		139A, 239A		139C, 239C		139D, 239D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	COM	1.5	9	1.5	8.8	1.5	8.0	1.0	4.0	ns
t _{PLH}	AI to OI	WIL	1.5	15	1.5	7.8	1.5	7.0			
t _{PHL}	Propagation Delay	COM	1.5	9	1.5	8.9	1.5	8.0	1.0	4.0	
t _{PLH}	EO to OI	WIL	1.5	15	1.5	8.0	1.5	7.0			

Notes:
 1. See test circuits and wave forms.

Q

High-Speed CMOS 8 Input Multiplexers

QS54/74FCT151T
QS54/74FCT251T

QS54/74FCT2151T
QS54/74FCT2251T

FEATURES/BENEFITS

- Pin and function compatible to the 74F151/251 and 74FCT151T/251T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 151T, 251T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Standard and A speed grades with 5.2ns tPD for A
- IOL = 48 mA Com., 32 mA Mil.

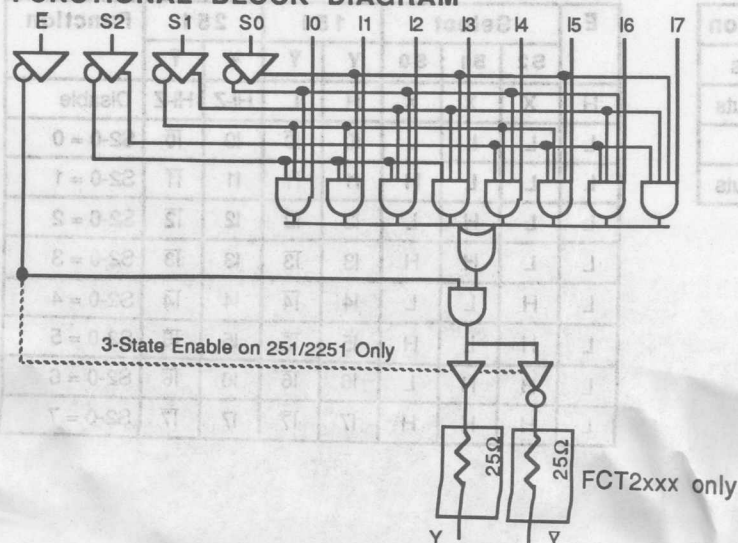
FCT-T 2151T, 2251T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.2ns tPD for A
- IOL = 12mA Com.

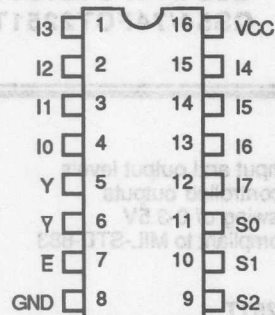
DESCRIPTION

The QSFCT151T and QSFCT251T are high speed CMOS TTL-compatible 8-input multiplexers. The 151 has TTL outputs; the 251 has 3-state outputs. The QSFCT2151T and QSFCT2251T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when VCC is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

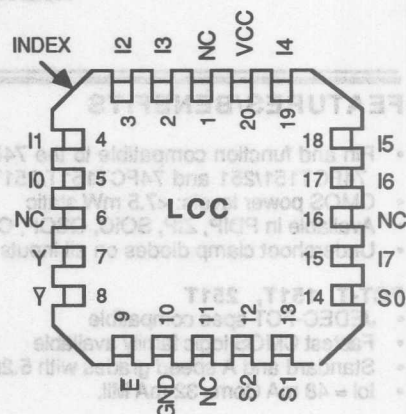


PDIP, SOIC, QSOP



ALL PINS TOP VIEW

* For ZIP pinout call factory



QSFACT151T, 251T, 2152T, 2251T

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_O < 0$	-20 mA
DC Output Diode Max. sink current/pin	-50 mA
N=Number of Outputs, M=Number of inputs	120 mA
Maximum Power Dissipation	0.5 watts
Storage Temperature	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-3, 10, 11, 13-15	4	4	5	7	pF
4-7, 9, 12	6	6	7	9	pF
	8	8	9	10	pF

Note: Capacitance is characterized but not tested

QSFCT151T, 251T, 2152T, 2251T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qocd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

QSFCT151T, 251T, 2152T, 2251T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
 Clload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	151 251 2151 2251		151A 251A 2151A 2251A		Unit
			Min	Max	Min	Max	
t _{IY}	Propagation Delay In to Y or Ȳ, 151/251	COM	1.5	7	1.5	5.2	ns
		MIL	1.5	8	1.5	5.8	
	Propagation Delay In to Y or Ȳ, 2151/2251	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
t _{SY}	Propagation Delay Sn to Y or Ȳ, 151/251	COM	1.5	9	1.5	6.6	
		MIL	1.5	9.5	1.5	7.4	
	Propagation Delay Sn to Y or Ȳ, 2151/2251	COM	1.5	9	1.5	6.6	
		MIL	1.5	9.5	1.5	7.4	
t _{OE} t _{OEL}	Output Enable Time E to Yi, 151	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
	Output Enable Time E to Yi, 2151	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
t _{PZH} t _{PZL}	Output Enable Time E to Yi, 151/251	COM	1.5	9	1.5	6.0	
		MIL	1.5	10	1.5	6.4	
	Output Enable Time E to Yi, 2151/2251	COM	1.5	9	1.5	6.0	
		MIL	1.5	10	1.5	6.4	
t _{PHZ} t _{PLZ}	Output Disable Time E to Yi, 251/2251	COM	2	1.5	7	6	
		MIL	2	1.5	7	6.3	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High-Speed CMOS Dual 4 Input Multiplexers

QS54/74FCT153T
QS54/74FCT253T

QS54/74FCT2153T
QS54/74FCT2253T

FEATURES/BENEFITS

- Pin and function compatible to the 74F153/253 74FCT153/253 and 74FCT153T/253T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs

FCT-T 153T, 253T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Standard and A speed grades with 5.2 ns tPD for A
- IOL = 48 mA Com., 32 mA Mil.

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

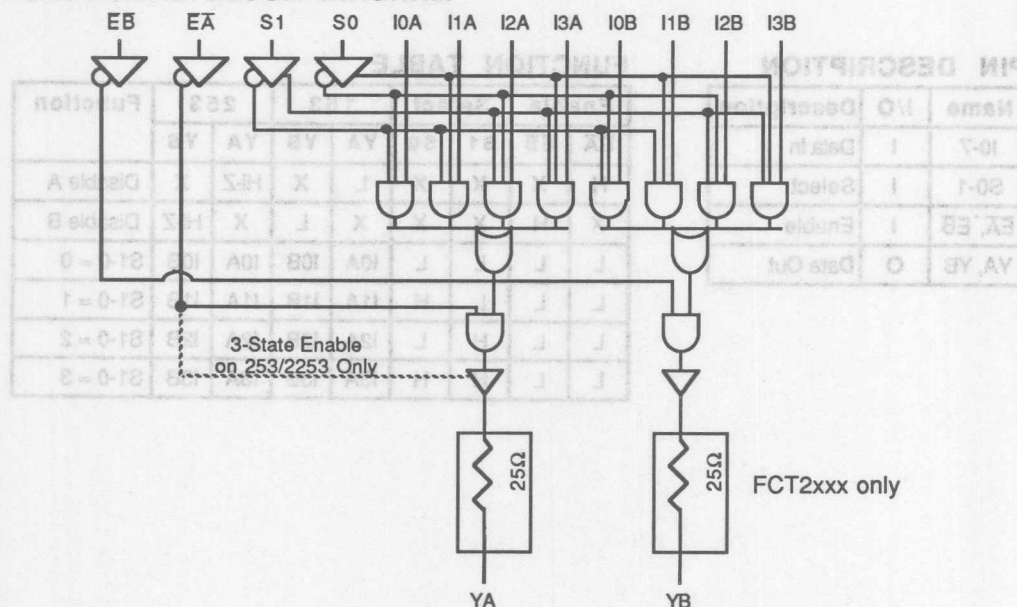
FCT-T 2153T, 2253T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.2 ns tPD for A
- IOL = 12mA Com.

DESCRIPTION

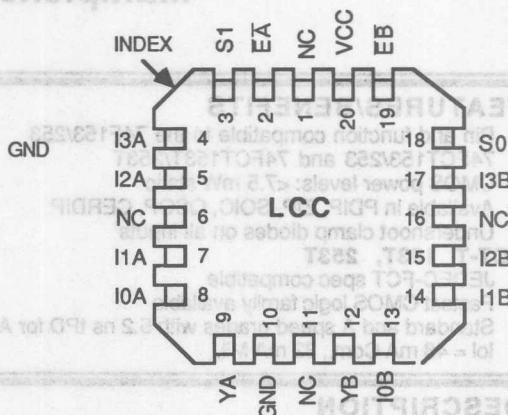
The QSFCT153T and QSFCT253T are high speed CMOS TTL-compatible dual 4-input multiplexers. The 153 has TTL outputs; the 253 has 3-state outputs. The QSFCT2153T and QSFCT2253T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ALL PINS TOP VIEW

* For ZIP pinout call factory

PIN DESCRIPTION

Name	I/O	Description
I0-7	I	Data In
S0-1	I	Select
EA, EB	I	Enable
YA, YB	O	Data Out

FUNCTION TABLE

Enable		Select		153		253		Function
EA	EB	S1	S0	YA	YB	YA	YB	
H	X	X	X	L	X	Hi-Z	X	Disable A
X	H	X	X	X	L	X	Hi-Z	Disable B
L	L	L	L	I0A	I0B	I0A	I0B	S1-0 = 0
L	L	L	H	I1A	I1B	I1A	I1B	S1-0 = 1
L	L	H	L	I2A	I2B	I2A	I2B	S1-0 = 2
L	L	H	H	I3A	I3B	I3A	I3B	S1-0 = 3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Am	Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
	1-6,10-15	4	4	5	7	pF
Am	7,9	6	6	7	9	pF
		8	8	9	10	pF

Note: Capacitance is characterized but not tested

Voh	Output HIGH Voltage		Voc = MIN		Voh	
	FCTXX & FCTXX	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)
Vol	Output LOW Voltage		Voc = MIN		Vol	
	FCTXX	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)
Rout	Output Resistance		Voc = MIN		Rout	
	FCTXX (250)	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)	lot = 12 mA (COM)	lot = 12 mA (MIL)

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 2 seconds.
3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysteresis	VtLh - VtLl for All Inputs		-	0.2	-	
Iih Iil	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	μA
Ioz	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-	mA
Ior	Current Drive FCT2XXX	Vcc = Min, Vo =2.0V		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 32 mA (MIL)	-	-	0.50	
			Iol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	21	28	38	Ω
			Iol = 12 mA (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qocd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

QSFCT153T, 253T, 2153T, 2253T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	153 253 2153 2253		153A 253A 2153A 2253A		Unit
			Min	Max	Min	Max	
t _{IY}	Propagation Delay In to Y, 153/253	COM	1.5	7	1.5	5.2	ns
		MIL	1.5	8	1.5	5.8	
	Propagation Delay In to Y, 2153/2253	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
t _{SY}	Propagation Delay Sn to Y, 153/253	COM	1.5	9	1.5	6.6	
		MIL	1.5	9.5	1.5	7.4	
	Propagation Delay Sn to Y, 2153/2253	COM	1.5	9	1.5	6.6	
		MIL	1.5	9.5	1.5	7.4	
t _{OE} t _{OEL}	Output Enable Time E to Yi, 153	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
	Output Enable Time E to Yi, 2153	COM	1.5	7	1.5	5.2	
		MIL	1.5	8	1.5	5.8	
t _{PZH} t _{PZL}	Output Enable Time E to Yi, 253	COM	1.5	9	1.5	6.0	
		MIL	1.5	10	1.5	6.4	
	Output Enable Time E to Yi, 2253	COM	1.5	9	1.5	6.0	
		MIL	1.5	10	1.5	6.4	
t _{PHZ} t _{PLZ}	Output Disable Time E to Yi, 253/2253	COM	2	1.5	7	1.5	6
		MIL	2	1.5	7	1.5	6.3

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High-Speed CMOS Quad 2 Input Multiplexers

QS54/74FCT157T
QS54/74FCT158T
QS54/74FCT257T
QS54/74FCT258T

QS54/74FCT2157T
QS54/74FCT2158T
QS54/74FCT2257T
QS54/74FCT2258T

FEATURES/BENEFITS

- Pin and function compatible to the 74F1/257/8 74FCT 1/257/8 and 74FCT1/257/8T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 157T, 158T, 257T, 258T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 4.3 ns for C
- I_{OL} = 48 mA Com., 32 mA Mil.

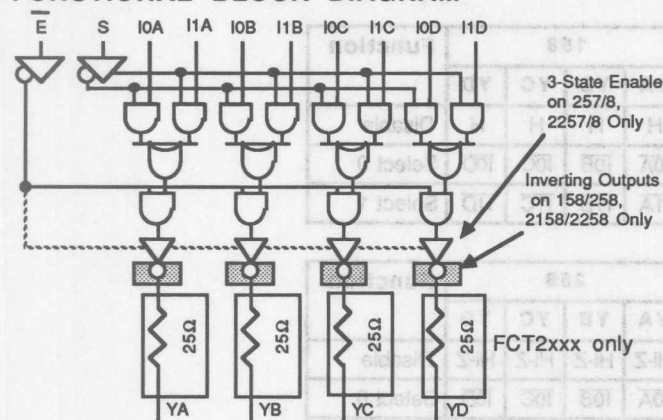
FCT-T 2157T, 2158T, 2257T, 2258T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.0 ns for A
- I_{OL} = 12mA Com.

DESCRIPTION

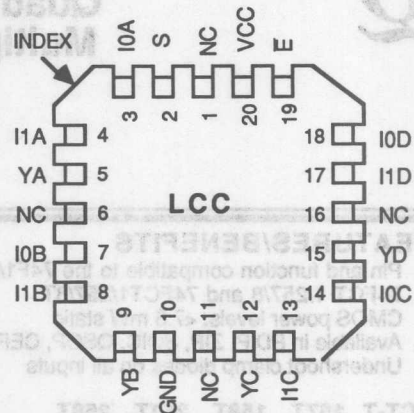
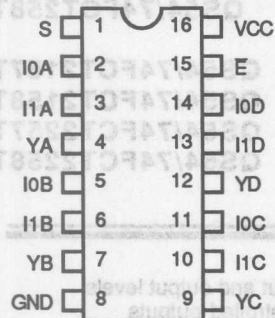
The QSFCT157/8T and QSFCT257/8T are high speed CMOS TTL-compatible 8-input multiplexers. The 157/257 parts are non-inverting; the 158/258 are inverting. The 157/8 has TTL outputs; the 257/8 has 3-state outputs. The QSFCT2157/8T and QSFCT2257/8T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ALL PINS TOP VIEW

* For ZIP pinout call factory

PIN DESCRIPTION

Name	I/O	Description
Ixx	I	Data Inputs
S	I	Select Input
E	I	Enable Input
YA-YD	O	Data Outputs

FUNCTION TABLES

E	S	157				158				Function
		YA	YB	YC	YD	YA	YB	YC	YD	
H	X	L	L	L	L	H	H	H	H	Disable
L	L	I0A	I0B	I0C	I0D	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	I1A	I1B	I1C	I1D	Select 1

E	S	257				258				Function
		YA	YB	YC	YD	YA	YB	YC	YD	
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	I0A	I0B	I0C	I0D	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	I1A	I1B	I1C	I1D	Select 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pin	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-3,5,6,10,11,13-15	4	4	5	7	pF
4,7,9,12	6	6	7	9	pF
8	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	SOIC	QSOP	PDIP, LCC	ZIP
V_{OH}	Output HIGH Voltage FCTXXX & FCTXXX	$I_{OH} = 15\text{ mA (MIL)}$ $I_{OH} = 15\text{ mA (COM)}$	$I_{OH} = 15\text{ mA (MIL)}$ $I_{OH} = 15\text{ mA (COM)}$	$I_{OH} = 15\text{ mA (MIL)}$ $I_{OH} = 15\text{ mA (COM)}$	$I_{OH} = 15\text{ mA (MIL)}$ $I_{OH} = 15\text{ mA (COM)}$
V_{OL}	Output LOW Voltage FCTXXX	$I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$	$I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$	$I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$	$I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$
R_{out}	Output Resistance FCTXXX (25°)	$I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	$I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	$I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	$I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$

Notes:
1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is 2 seconds.
3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{thl} - V_{thl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qocd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125°C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	157/8 257/8 2157/8 2257/8		157/8A 257/8A 2157/8A 2257/8A		157/8C 257/8C		Unit
			Min	Max	Min	Max	Min	Max	
t _{IY}	Propagation Delay In to Y, 157/8/257/8	COM	1.5	6.0	1.5	5.0	1.5	4.3	ns
		MIL	1.5	7.0	1.5	5.8	1.5	5.0	
	Propagation Delay In to Y, 2157/8/2257/8	COM	1.5	6.0	1.5	5.0			
		MIL	1.5	7.0	1.5	5.8			
t _{SY}	Propagation Delay S to Y, 157/8/257/8	COM	1.5	10.5	1.5	7.0	1.5	5.2	
		MIL	1.5	12	1.5	8.1	1.5	6.0	
	Propagation Delay S to Y, 2157/8/2257/8	COM	1.5	10.5	1.5	7.0			
		MIL	1.5	12	1.5	8.1			
t _{OE} t _{OEL}	Output Enable Time E to Yi, 157/8	COM	1.5	10.5	1.5	6.0	1.5	4.8	
		MIL	1.5	12	1.5	7.4	1.5	5.9	
	Output Enable Time E to Yi, 2157/8	COM	1.5	10.5	1.5	6.0			
		MIL	1.5	12	1.5	7.4			
t _{PZH} t _{PZL}	Output Enable Time E to Yi, 257/8	COM	1.5	8.5	1.5	7.0	1.5	6.0	
		MIL	1.5	10	1.5	8.0	1.5	6.8	
	Output Enable Time E to Yi, 2257/8	COM	1.5	8.5	1.5	7.0			
		MIL	1.5	10	1.5	8.0			
t _{PHZ} t _{PLZ}	Output Disable Time E to Yi, 257/8/2257/8	COM	2	1.5	6.0	1.5	5.5	1.5	5.0
		MIL	2	1.5	8.0	1.5	5.8	1.5	5.3

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QS54/74FCT161T
QS54/74FCT163T
QS54/74FCT2161T
QS54/74FCT2163T

- Pin and function compatible to the 74F161/3
- 74FCT 161/3 and 74FCT161T/3T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A and C speed grades with 5.6 ns tPD for C
- I_{OL} = 48 mA Com., 32 mA Mil.

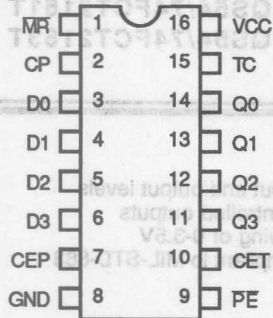
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 6.2 ns tPD for A
- I_{OL} = 12mA Com.

The QSFCT161T and QSFCT163T are high speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. The 216 and 2163 are 25Ω resistor output versions of the 161 and 163, respectively, and are useful for driving transmission lines and reducing system noise. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

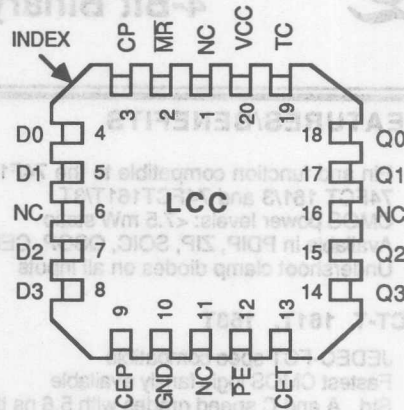
PIN CONFIGURATIONS

PDIP, SOIC, QSOP



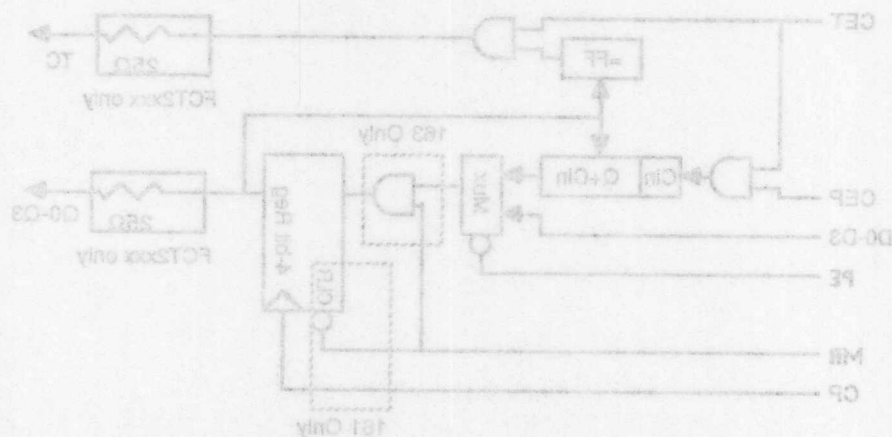
ALL PINS TOP VIEW

* For ZIP pinout call factory



The QSFACT161T and QSFACT2163T are high speed CMOS synchronous presetable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. The 2161 and 2163 are 25Ω resistor output versions of the 161 and 163, respectively, and are useful for driving transmission lines and reducing system noise. Data is presetable and the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see OSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM



QSFCT161T, 2161T, 163T, 2163T

PIN DESCRIPTION

Name	I/O	Description
D0-3	I	Data Inputs
Q0-3	O	Data Outputs
CP	I	Clock
MR	I	Master Reset

Name	I/O	Description
CEP	I	Count Enable
CET	I	Count and TC Enable
TC	O	Terminal Count
PE	I	Parallel Load Enable

FUNCTION TABLE

Inputs						Outputs			Function
MR	PE	CP	CEP	CET	Di	Q0-3		TC	
						161	163		
L	X	X	X	X	X	L	-	L	Clear 161
L	X	↑	X	X	X	-	L	L	Clear 163
H	L	↑	X	X	D0-3	D0-3	D0-3	X	Load Data
H	H	↑	H	H	X	Q+1	Q+1	X	Count
H	H	↑	L	X	X	Q	Q	X	Count Inhibit P
H	H	↑	X	L	X	Q	Q	X	Count Inhibit T
H	H	X	X	H	X	F	F	H	Count = 1111
H	H	X	X	H	X	0-E	0-E	L	Count ≠ 1111
H	H	X	X	L	X	X	X	L	TC Inhibit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-7,9,10	4	4	5	7	pF
11-15	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{ilh} - V_{il}$ for All Inputs	-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$ $I_{oh} = 12 \text{ mA (MIL)}$ $I_{oh} = 15 \text{ mA (COM)}$	2.4 2.4	- -	- -	Volts
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$ $I_{ol} = 32 \text{ mA (MIL)}$ $I_{ol} = 48 \text{ mA (COM)}$	- -	- -	0.50 0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	- -	- -	0.50 0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	21 24	28 28	38 35	Ω

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}$, $\text{freq} = 0$ $0V \leq V_{in} \leq 0.2V$ or $V_{cc} - 0.2V \leq V_{in} \leq V_{cc}$	-	1.5	mA
ΔI_{cc}	Supply Current per Input @ TTL HIGH	$V_{cc} = \text{MAX}$, $V_{in} = 3.4V$, $\text{freq} = 0$ (2)	-	2.0	mA
Q_{ccd}	Supply Current per input per mHz	$V_{cc} = \text{MAX}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{cc} (3,4)	-	0.25	mA/MHz

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i = 3.4V$)
- For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_c can be computed using the above parameters as explained in the Technical Overview section.

I_{cc}	-	-	50	$V_{cc} = \text{MAX}$, $V_{in} = 0.2V$	Current Drive	mA
V_{ic}	-0.7	-	-	$V_{cc} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	Input Clamp Voltage	V
V_{oh}	-	-	2.4	$I_{oh} = 12 \text{ mA}$ (MIL)	Output HIGH Voltage	V
	-	-	2.4	$I_{oh} = 12 \text{ mA}$ (COM)	$V_{cc} = \text{MIN}$ FCT500X & FCT500X	
V_{ol}	0.50	-	-	$I_{ol} = 32 \text{ mA}$ (MIL)	Output LOW Voltage	V
	0.50	-	-	$I_{ol} = 48 \text{ mA}$ (COM)	$V_{cc} = \text{MIN}$ FCT500X	
	0.50	-	-	$I_{ol} = 12 \text{ mA}$ (MIL)	Output LOW Voltage	V
	0.50	-	-	$I_{ol} = 12 \text{ mA}$ (COM)	$V_{cc} = \text{MIN}$ FCT500X (250)	
R_{out}	38	38	21	$I_{ol} = 12 \text{ mA}$ (MIL)	Output Resistance	Ω
	35	38	24	$I_{ol} = 12 \text{ mA}$ (COM)	$V_{cc} = \text{MIN}$ FCT500X (250)	

- Notes:
- Typical values indicate $V_{CC} = 2.0V$ and $T_A = 25^\circ C$.
 - Not more than one output should be shorted and the duration is 21 seconds.
 - These parameters are guaranteed by design but not tested.

QSFCT161T, 2161T, 163T, 2163T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, V_{CC} = 5.0V±5%, Military TA = -55°C to 125°C, V_{CC} = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes (1)	161 163 2161 2163		161A 163A 2161A 2163A		161C 163C		Unit
				Min	Max	Min	Max	Min	Max	
† CPQ	Propagation Delay CP to Qi, 161/3	COM		2	9.5	2	6.2	2	5.6	ns
		MIL		2	10	2	6.5	2	6.1	
	Propagation Delay CP to Qi, 2161/3	COM		2	9.5	2	6.2			
		MIL		2	10	2	6.5			
† MRQ	Propagation Delay MR to Qi, 161	COM		2	13	2	8.5	2	7.8	
		MIL		2	14	2	9.1	2	8.3	
	Propagation Delay MR to Qi, 2161	COM		2	14	2	9.1			
		MIL		2	13	2	8.5			
† CPTC	Propagation Delay CP to TC	COM		2	15	2	9.8	2	8.8	
		MIL		2	16.5	2	10.8	2	9.8	
† CETC	Propagation Delay CET to TC	COM		1.5	8.5	1.5	5.5	1.5	5.0	
		MIL		1.5	9	1.5	5.9	1.5	5.4	
† MRTC	Propagation Delay MR to TC	COM		1.5	11.5	1.5	7.5	1.5	6.8	
		MIL		1.5	12.5	1.5	8.2	1.5	7.4	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QSFACT161T, 2161T, 163T, 2163T

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	161		161A		161C		Unit
			(1)		2161A		163C		
			163	2161	163A	2161A	163C	2163A	
			Min	Max	Min	Max	Min	Max	
t DS	Data Setup Time Di to CP	COM	5		4		3.5		ns
		MIL	5.5		4.5		4.0		
t DH	Data Hold Time Di to CP	COM	1.5		1.5		1.5		
		MIL	2		2		2		
t CS	Count Enab. Setup Time CEP, CET to CP	COM	11.5		9.5		8.5		
		MIL	13		11		10		
t CH	Count Enable Hold Time CEP, CET to CP	COM	0		0		0		
		MIL	0		0		0		
t MRS t PES	Control Setup Time MR, PE to CP	COM	11.5		9.5		8.5		
		MIL	13.5		11.5		10.5		
t MRH t PEH	Control Hold Time MR, PE to CP	COM	1.5		1.5		1.5		
		MIL	1.5		1.5		1.5		
t CPW	Clock Pulse Width HIGH or LOW	COM	2	5	4		3		
		MIL	2	5	4		3		
t MRW	MR Reset Pulse Width 161, 2161	COM	2	5	4		3		
		MIL	2	5	4		3		
t MRW	Reset Recovery Time MR to CP, 161, 2161	COM	2	6	5		4		
		MIL	2	6	5		4		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High-Speed CMOS Presettable Synchronous 4-Bit Binary Counters

QS54/74FCT191T
QS54/74FCT2191T

Input and output levels
Controlled outputs
Voltage of 0-3.5V
Compliant to MIL-STD-883

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

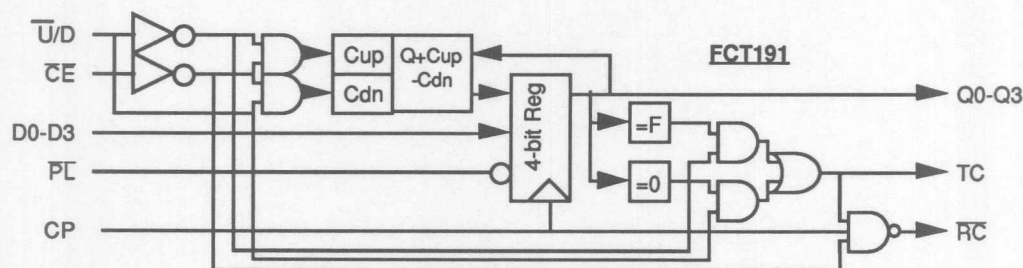
FCT-T 2191T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 7.8ns tPD for A
- IOL = 12mA Com.

4

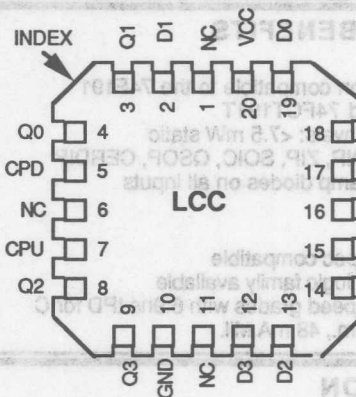
The QSFCT191T is a high speed CMOS 4-bit binary up/down counter. It has a single clock with clock enable and up/down control inputs and ripple carry output. The '191 has asynchronous preload inputs which override the count inputs. The '2191 is a 25Ω resistor output version of the '191 and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM



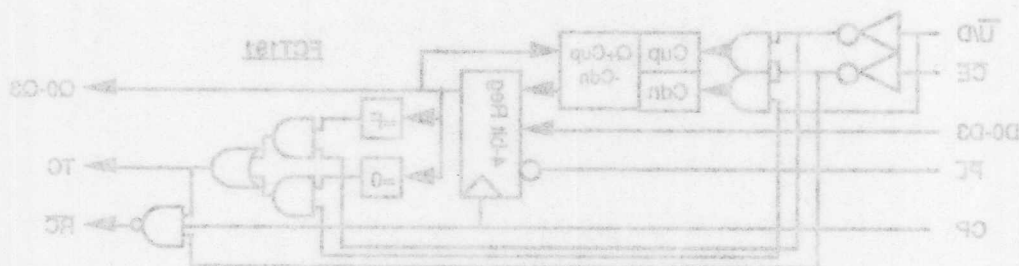
PIN CONFIGURATIONS

PDIP, SOIC



The QS74FCT191T is a high speed CMOS 4-bit binary up/down counter. It has a single clock with clock enable and up/down control inputs and ripple carry output. The '191' has synchronous parallel inputs which override the count inputs. The '2191' is a 285 resistor output version of the '191' which driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see * For ZIP pinout contact factory).

FUNCTIONAL BLOCK DIAGRAM



QS74FCT191T, QS74FCT2191T

PIN DESCRIPTION

Name	I/O	Description
D0-3	I	Data Inputs
Q0-3	O	Data Outputs
PL	I	Pre Load
U/D	I	Up/Down Select
CE	I	Count Enable
CP	I	Count Clock
TC	O	Terminal Count
RC	O	Ripple Clock

FUNCTION TABLE

Inputs				Outputs				Function
PL	U/D	CP	CE	Di	Q0-3	TC	RC	
L	X	X	X	D0-3	D0-3	X	X	Load Data
H	L	↑	L	X	Q+1	X	X	Count Up
H	H	↑	L	X	Q-1	X	X	Count Down
H	X	X	H	X	Q	X	X	Count Inhibit
H	L	X	X	X	F	H	H	Count Up = 1111
H	L		L	X	F	H		
H	L	X	X	X	0-E	L	H	Count Up ≠ 1111
H	H	X	X	X	0	H	H	Count Dn = 0000
H	H		L	X	0	H		
H	H	X	X	X	1-F	L	H	Count Dn ≠ 0000

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,4,5,9-11,14,15	4	4	5	7	pF
2,3,6,7,12,13	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

QS74FCT191T, QS74FCT2191T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, VCC = 5.0V±5% Military TA = -55°C to 125° C, VCC = 5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysteresis	VtH - VtL for All Inputs		-	0.2	-	
I _{ih} I _{il}	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	μA
I _{oz}	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-	mA
Ior	Current Drive FCT2XXX	Vcc = Min, Vo =2.0V		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 32 mA (MIL)	-	-	0.50	
			Iol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	21	28	38	Ω
			Iol = 12 mA (COM)	24	28	35	

Notes:

1. Typical values indicate VCC=5.0V and TA=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

QS74FCT191T, QS74FCT2191T

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled. One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input (V_i = 3.4V)
- For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_{cc} can be computed using the above parameters as explained in the Technical Overview section.

V _{OL}	FCT200X	Output LOW Voltage	V _{cc} = MIN, I _{OL} = 15 mA (MIL)	0.5	-	-
		FCT200X & FCT200X	I _{OL} = 15 mA (MIL)	0.5	-	-
			I _{OL} = 15 mA (COM)	0.5	-	-
	FCT200X	Output LOW Voltage	V _{cc} = MIN, I _{OL} = 35 mA (MIL)	0.5	-	-
			I _{OL} = 35 mA (MIL)	0.5	-	-
			I _{OL} = 35 mA (COM)	0.5	-	-
V _{OH}	FCT200X (50%)	Output HIGH Voltage	V _{cc} = MIN, I _{OH} = 15 mA (MIL)	0.5	-	-
			I _{OH} = 15 mA (COM)	0.5	-	-
R _{out}	FCT200X (50%)	Output Resistance	V _{cc} = MIN, I _{OL} = 15 mA (MIL)	30	30	30
			I _{OL} = 15 mA (COM)	30	30	30

- Notes:
- Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
 - Not more than one output should be shorted and the duration is ≤ 2 seconds.
 - These parameters are guaranteed by design but not tested.

QS74FCT191T, QS74FCT2191T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	191 2191		191A 2191A		191C		Unit
			Min	Max	Min	Max	Min	Max	
tCPQ	Propagation Delay CP to Qi	COM	2.5	12	2.5	7.8	2	6.9	ns
		MIL	1.5	16	1.5	10.5	1.5	9	
tCPTC	Propagation Delay CP to TC	COM	3.0	14	3.0	11.8	2.5	10.2	
		MIL	2.0	16	2.0	12.2	2.0	11.5	
tCPRC	Propagation Delay CP to RC	COM	2.5	8.5	2.5	8.5	2.0	8	
		MIL	1.5	12.5	1.5	10.0	1.5	9.2	
tCERC	Propagation Delay CE to RC	COM	2	8	2	7.2	2	6.8	
		MIL	2	8.5	2	8	2	7.4	
tUDRC	Propagation Delay U/D to RC	COM	4	15	2	9.8	2	9.0	
		MIL	4	16.5	2	10.8	2	10.0	
tUDTC	Propagation Delay U/D to TC	COM	3	11	3	7.2	2	6.8	
		MIL	3	13	3	8.5	2	7.9	
tPQ	Propagation Delay Pi to Qi	COM	2	14	2	9.1	2	8.5	
		MIL	1.5	16	1.5	10.4	1.5	9.8	
tPLQ	Propagation Delay PL to Qi	COM	3	13	3	8.5	2	7.8	
		MIL	3	14	3	9.1	2	8.5	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QS74FCT191T, QS74FCT2191T

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	191 2191		191A 2191A		191C		Unit
			Min	Max	Min	Max	Min	Max	
tPPLS	Pi to PL setup	COM	5		4		4		
		MIL	6		5		5		
tPPLH	Pi to PL hold	COM	1.5		1.5		1.5		
		MIL	1.5		1.5		1.5		
tCS	CE to CP setup	COM	10		9		9		
		MIL	10.5		9.5		9.5		
tCH	CE to CP hold	COM	0		0		0		
		MIL	0		0		0		
tUDCPS	U/D to CP setup	COM	12		10		10		
		MIL	12		10		10		
tUDCPH	U/D to CP hold	COM	0		0		0		
		MIL	0		0		0		
tCPW	Clock Pulse Width HIGH or LOW	COM	5		4		4		
		MIL	7		6		6		
tPL	PL low	COM	6		5.5		5.5		
		MIL	8.5		8		8		
tPLCPR	PL to CP recovery	COM	6		5		5		
		MIL	7.5		6.5		6.5		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High-Speed CMOS Presettable Synchronous 4-Bit Binary Counters

QS54/74FCT193T
QS54/74FCT2193T

FEATURES/BENEFITS

- Pin and function compatible to the 74F193, 74FCT193 and 74FCT193T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 193T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Standard and A speed grades with 6.5ns tPD for A
- I_{OL} = 64 mA Com., 48 mA Mil.

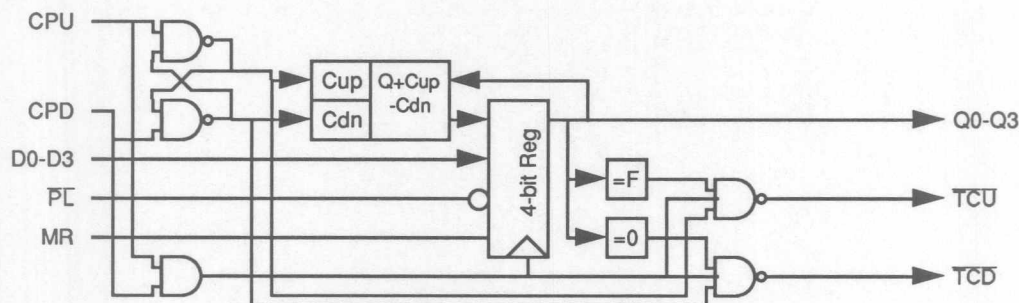
FCT-T 2193T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 6.5ns tPD for A
- I_{OL} = 12mA Com.

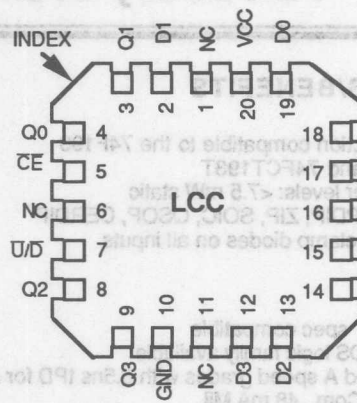
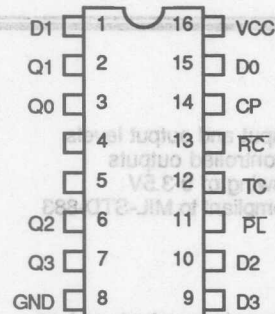
DESCRIPTION

The QSFCT193 is a high speed CMOS 4-bit binary up/down counter. It has separate up and down clock inputs, up/down ripple clock outputs and an asynchronous clear input. The '193 has asynchronous preload inputs which override the count inputs. The '2193 is a 25Ω resistor output version of the 193, and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

PDIP, SOIC

ALL PINS TOP VIEW

* For ZIP pinout contact factory

PIN DESCRIPTION

Name	I/O	Description
D0-3	I	Data Inputs
Q0-3	O	Data Outputs
PL	I	Pre Load
MR	I	Master Reset
CPU	I	Count Up Clock
CPD	I	Count Down Clock
TCU	O	Terminal Count Up
TCD	O	Terminal Count Down

FUNCTION TABLE

Inputs					Outputs			Function
PL	MR	CPU	CPD	Di	Q0-3	TCU	TCD	
X	H	X	X	X	0000	X	X	Reset
L	L	X	X	D0-3	D0-3	X	X	Load Data
H	L	↑	H	X	Q+1	X	X	Count Up
H	L	H	↑	X	Q-1	X	X	Count Down
H	L	L	H	X	F	L	H	Count Up = 1111
H	L	H	H	X	0-E	H	H	Count Up ≠ 1111
H	L	H	L	X	0	H	L	Count Dn = 0000
H	L	H	H	X	1-F	H	H	Count Dn ≠ 0000

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,4,5,9-11,14,15	4	4	5	7	pF
2,3,6,7,12,13	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load Data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Count Up	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Count Down	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Count Up = 1111	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
Count Up = 1111	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
Count On = 0000	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Count On = 0000	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, VCC = 5.0V±5% Military TA = -55°C to 125°C, VCC = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔVt	Input Hysteresis	VtH - VtL for All Inputs	-	0.2	-	
Iih Iil	Input Current Input HIGH or LOW	VCC = MAX, 0 ≤ Vin < VCC	-	-	5	μA
Ioz	Off State Output Current (Hi-Z)	VCC = MAX, 0 ≤ Vin ≤ VCC	-	-	5	
Ios	Short Circuit Current FCTXXX	VCC = MAX, Vo = GND (2,3)	-60	-	-	mA
Ior	Current Drive FCT2XXX	VCC = MIN, Vo = 2.0V	50	-	-	mA
Vic	Input Clamp Voltage	VCC = MIN, Iin = 18 mA (3)	-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	VCC = MIN Ioh = 12 mA (MIL) Ioh = 15 mA (COM)	2.4 2.4	- -	- -	Volts
Vol	Output LOW Voltage FCTXXX	VCC = MIN Iol = 32 mA (MIL) Iol = 48 mA (COM)	- -	- -	0.50 0.50	
	Output LOW Voltage FCT2XXX (25Ω)	VCC = MIN Iol = 12 mA (MIL) Iol = 12 mA (COM)	- -	- -	0.50 0.50	
Rout	Output Resistance FCT2XXX (25Ω)	VCC = MIN Iol = 12 mA (MIL) Iol = 12 mA (COM)	21 24	28 28	38 35	Ω

Notes:

1. Typical values indicate VCC=5.0V and TA=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4V, freq = 0 (2)	-	2.0	μA
Q _{cc}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{cc} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

V _{ic}	Input Clamp Voltage	V _{cc} = MIN, I _{in} = 18 mA (2)	-	-0.7	-1.5	Volts
V _{oh}	Output HIGH Voltage	V _{cc} = MIN I _{oh} = 12 mA (MIL) I _{oh} = 12 mA (COM)	2.4	-	-	Volts
V _{ol}	Output LOW Voltage	V _{cc} = MIN I _{ol} = 32 mA (MIL) I _{ol} = 48 mA (COM)	-	-	0.50	Volts
V _{oh}	Output LOW Voltage (FCTXXX (SE))	V _{cc} = MIN I _{ol} = 12 mA (MIL) I _{ol} = 12 mA (COM)	-	-	0.50	Volts
R _{out}	Output Resistance (FCTXXX (SE))	V _{cc} = MIN I _{ol} = 12 mA (MIL) I _{ol} = 12 mA (COM)	2.4	2.8	3.8	Ω

- Notes:
1. Typical values indicate V_{cc} = 5.0V and T_a = 25°C.
 2. Not more than one output should be shorted and the duration is ≤ 1 second.
 3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
 Load = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	193 2193		193A 2193A		Unit
			Min	Max	Min	Max	
tCPTC	Propagation Delay CPU/D to TCU/TCU	COM	2.0	10	2.0	6.5	ns
		MIL	2.0	10.5	2.0	6.9	
tCPQ	Propagation Delay CPU/D to Qi	COM	2.0	13.5	2.0	8.8	
		MIL	2.0	14.0	2.0	9.1	
tDQ	Propagation Delay Di to Qi	COM	2.0	15.5	2.0	10.1	
		MIL	1.5	16.5	2.0	10.8	
tPLQ	Propagation Delay PL to Qi	COM	2.0	14.0	2.0	8.8	
		MIL	2.0	13.5	2.0	9.1	
tMRQ	Propagation Delay MR to Qi	COM	3.0	15.5	3.0	10.1	
		MIL	3.0	16.0	3.0	10.4	
tMRTCU	Propagation Delay MR to TCU	COM	3.0	14.5	3.0	9.4	
		MIL	3.0	15.0	3.0	9.8	
tMRTCD	Propagation Delay MR to TCD	COM	3.0	15.5	3.0	10.1	
		MIL	3.0	16.0	3.0	10.4	
tPLTC	Propagation Delay PL to TCU/D	COM	3.0	16.5	3.0	10.8	
		MIL	3.0	18.5	3.0	12.0	
tDTC	Propagation Delay Di to TCU/D	COM	3.0	15.5	3.0	10.1	
		MIL	3.0	16.5	3.0	10.8	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QSFCT193T, 2193T

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	Unit			
			193 2193		193A 2193A	
			Min	Max	Min	Max
tDPLS	Di to $\overline{PL}$ setup	COM	5.0		4.0	
		MIL	6.0		5.0	
tDPLH	Di to $\overline{PL}$ hold	COM	2.0		1.5	
		MIL	2.0		1.5	
tPLW	$\overline{PL}$ low time	COM	6.0		5.0	
		MIL	7.5		6.5	
tCP	$\overline{CPU}/\overline{D}$ pulse width high and low	COM 2	5.0		4.0	
		MIL 2	7.0		6.0	
tCPL	$\overline{CPU}/\overline{D}$ pulse width low (change of direction)	COM 2	10.0		8.0	
		MIL 2	12.0		10.0	
tMRH	MR high time	COM 2	6.0		5.0	
		MIL 2	6.0		5.0	
tRPLCP	$\overline{PL}$ to $\overline{CPU}/\overline{D}$ recovery	COM 2	6.0		5.0	
		MIL 2	8.0		7.0	
tRMRCP	MR to $\overline{CPU}/\overline{D}$ recovery	COM 2	4.0		3.0	
		MIL 2	4.5		3.5	

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS 8-Bit Buffers/Line Drivers

QS54/74FCT240T
QS54/74FCT241T
QS54/74FCT244T

QS54/74FCT2240T
QS54/74FCT2241T
QS54/74FCT2244T

FEATURES/BENEFITS

- Pin and function compatible to the 74F240/1/4
- 74FCT 240/1/4 and 74FCT240T/1T/4T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 240T, 241T, 244T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, C, & D speed grades with 3.8 ns tPD for D
- IOL = 64 mA Com., 48 mA Mil.

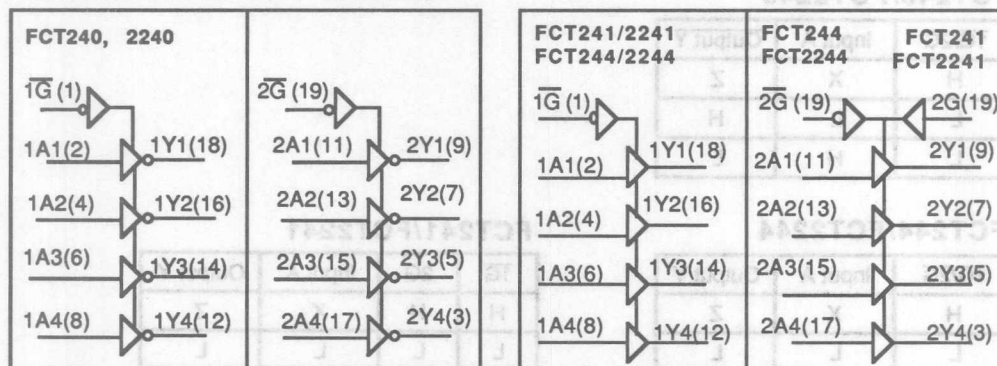
FCT-T 2240T, 2241T, 2244T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, & C speed grades with 4.1 ns tPD for C
- IOL = 12mA Com

DESCRIPTION

The FCT240T, FCT241T and FCT244T are 8-bit buffers/line drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2240T, FCT2241T and FCT2244T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2240, 2241, 2244 series parts can replace the 240 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

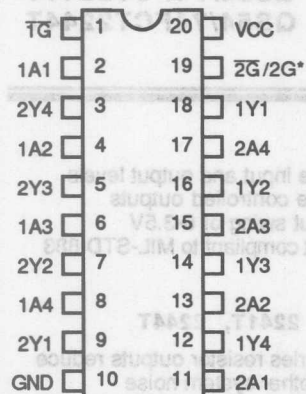


Note that pin 19 is 2G-bar on the FCT244 and 2G for the FCT241

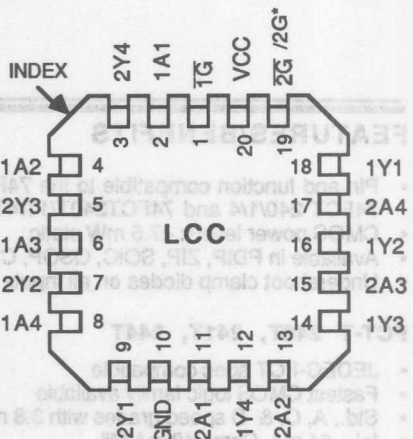
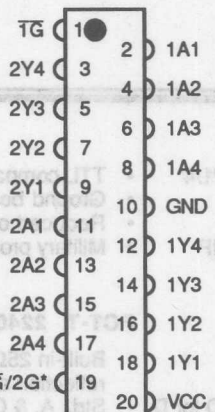
PINOUTS

FCT240/241/244
FCT2240/2241/2244

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

*Note: Pin 19 is 2G for the 240/244 and is 2G for the 241

FUNCTION TABLES

FCT240/FCT2240

TG/2G	Input A	Output Y
H	X	Z
L	L	H
L	H	L

FCT244/FCT2244

TG/2G	Input A	Output Y
H	X	Z
L	L	L
L	H	H

FCT241/FCT2241

TG	2G	Input A	Output Y
H	H	X	Z
L	L	L	L
L	L	H	H

H=High, L=Low, Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,19	4	4	5	7	pF
-----	6	6	7	9	pF
2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Test Conditions	Typical Value	Min	Max
V_{IC}	Input Clamping Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 10\text{ mA}$ (C)	-0.7	-	-
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = 12\text{ mA}$ (MIL)	2.4	-	-
	FCT2XX & FCT2XX	$V_{CC} = \text{MIN}$, $I_{OH} = 12\text{ mA}$ (COM)	2.4	-	-
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 48\text{ mA}$ (MIL)	0.35	-	-
	FCT2XX	$V_{CC} = \text{MIN}$, $I_{OL} = 48\text{ mA}$ (COM)	0.35	-	-
	Output LOW Voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 12\text{ mA}$ (MIL)	0.30	-	-
	FCT2XX (250)	$V_{CC} = \text{MIN}$, $I_{OL} = 12\text{ mA}$ (COM)	0.30	-	-
R_{OUT}	Output Resistance	$V_{CC} = \text{MIN}$, $I_{OL} = 12\text{ mA}$ (MIL)	38	38	38
	FCT2XX (250)	$V_{CC} = \text{MIN}$, $I_{OL} = 12\text{ mA}$ (COM)	38	38	38

Notes:
 1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
 2. Not more than one output should be shorted and the duration is 2 seconds.
 3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 48 \text{ mA}$ (MIL)	-	-	0.55	
			$I_{ol} = 64 \text{ mA}$ (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{cc}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input (V_i = 3.4V)
- For flipflops Q_{cc} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_c can be computed using the above parameters as explained in the Technical Overview section.

Symbol	Description	Notes	(1)				240T, 241T, 244T				2240T, 2241T, 2244T				Unit			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t _{PHL} t _{PLH}	Propagation Delay A to Y, F0T240T	COM	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns	
		WIL	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	ns	
	Propagation Delay A to Y, F0T241T	COM	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns	
		WIL	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	ns	
t _{RZH} t _{RFL}	Output Enable Time OE to Y, F0T240T	COM	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	ns	
		WIL	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns	
	Output Enable Time OE to Y, F0T241T	COM	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	1.5	8	ns	
		WIL	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns	
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y	COM	1.5	7	1.5	7	1.5	7	1.5	7	1.5	7	1.5	7	1.5	7	ns	
		WIL	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	ns	

Notes:
1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$; Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$
 Cload = 50 pF, Rload = 500 Ω unless otherwise noted

FCT240, FCT2240

Symbol	Description	Notes (1)	240, 2240		240A, 2240A		240C, 2240C		240D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPHL tPLH	Propagation Delay Ai to Yi, FCT240	Com	1.5	8	1.5	4.8	1.5	4.1	1.5	3.8	ns
		MII	1.5	9	1.5	5.1					
	Propagation Delay Ai to Yi, FCT2240	Com	1.5	8	1.5	4.8	1.5	4.1			
		MII	1.5	9	1.5	5.1					
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Yi, FCT240	Com	1.5	10	1.5	6.2	1.5	5.8	1.5	5.6	
		MII	1.5	10.5	1.5	6.5					
	Output Enable Time $\overline{\text{OE}}$ to Yi, FCT2240	Com	1.5	10	1.5	6.2	1.5	5.8			
		MII	1.5	10.5	1.5	6.5					
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Yi	Com	2	1.5	9.5	1.5	5.6	1.5	5.2	1.5	5.2
		MII	2	1.5	10.0	1.5	5.9				

FCT241, FCT244, FCT2241, FCT2244

Symbol	Description	Notes (1)	241/4, 2241/4		241/4A, 2241/4A		241/4C, 2241/4C		244D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPHL tPLH	Propagation Delay Ai to Yi, FCT241/4	COM	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.8	ns
		MIL	1.5	7.5	1.5	5.1					
	Propagation Delay Ai to Yi, FCT2241/4	COM	1.5	6.5	1.5	4.8					
		MIL	1.5	7.5	1.5	5.1					
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Yi, FCT241/4	COM	1.5	8	1.5	6.2	1.5	5.8	1.5	5.6	
		MIL	1.5	8.5	1.5	6.5					
	Output Enable Time $\overline{\text{OE}}$ to Yi, FCT2241/4	COM	1.5	8	1.5	6.2					
		MIL	1.5	8.5	1.5	6.5					
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Yi	COM	2	1.5	7	1.5	5.6	1.5	5.2	1.5	5.2
		MIL	2	1.5	7.5	1.5	5.9				

Notes:

1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

Q

High Speed CMOS 8-Bit Transceivers

QS54/74FCT245T
QS54/74FCT640T

QS54/74FCT2245T
QS54/74FCT2640T

FEATURES/BENEFITS

- Pin and function compatible to the 74F245/640, 74FCT245/640 and 74FCT245T/640T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 245T, 640T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, C, and D speed grades; 3.8 ns tPD for D
- I_{OL} = 64 mA Com., 48 mA Mil.

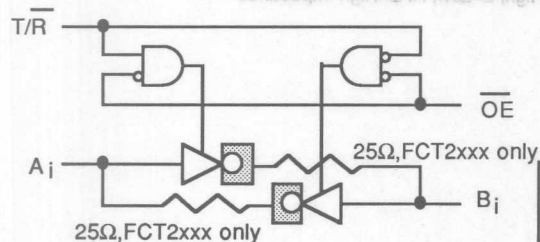
FCT-T 2245T, 2640T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades; 4.1 ns tPD for C
- I_{OL} = 12mA Com.

DESCRIPTION

The QS54/74FCT245AT/CT and QS54/74FCT2245AT/CT are 8-bit non-inverting transceivers that have three-state outputs which are useful for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow, either from A to B or B to A, and the Output Enable ($\overline{OE}$) input enables the selected port for output. The FCT245AT/CT and FCT2640AT/CT are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2245 parts can replace the 245 series to reduce noise in an existing design. All inputs have clamp diode for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

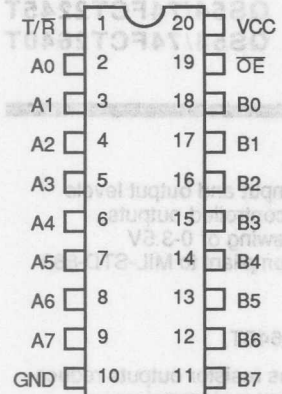


 Inverting Drivers on 640/2640 Only
(245/2245 have Non-Inverting Drivers)

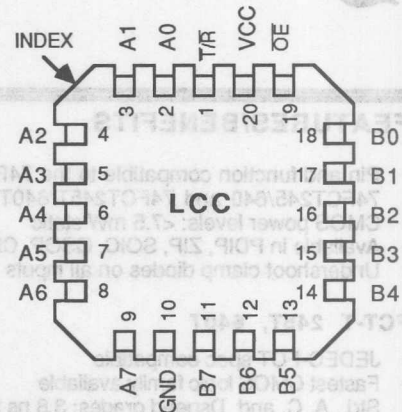
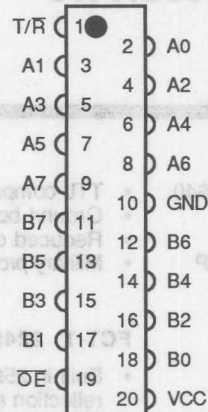
QSFCT245T, 640T, 2245T, 2640T

PINOUTS

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

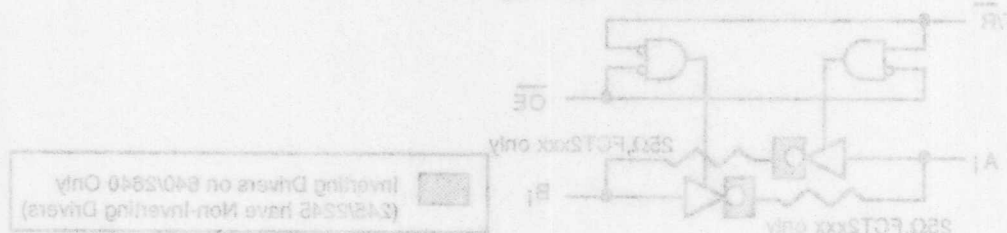
PIN DESCRIPTION

Name	I/O	Description
Ai	I/O	Data Bus A
Bi	I/O	Data Bus B
T/R	I	Direction
OE	I	Output Enable

FUNCTION TABLE

OE	T/R	A	B	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	Output	Input	Bus B to Bus A
L	H	Input	Output	Bus A to Bus B

H=High, L=Low, Hi-Z=High Impedance



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

	Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
	1,19	4	4	5	7	pF
	-----	6	6	7	9	pF
	2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	SOIC		QSOP		PDIP, LCC		ZIP	
		Min	Max	Min	Max	Min	Max	Min	Max
V_{OH}	Output HIGH Voltage (PCTXXX & FCTXXX)	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4
V_{OL}	Output LOW Voltage (PCTXXX)	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
R_{out}	Output Resistance (PCTXXX)	38	38	38	38	38	38	38	38

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be switched and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

QSFCT245T, 640T, 2245T, 2640T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{tH} - V_{tL}$ for All Inputs		-	0.2	-	
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{OZ} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$		-	-	5	
Ios	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$		-60	-	-	mA
Ior	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}, V_o = 2.0\text{V}$		50	-	-	mA
Vic	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	Iol = 12 mA (MIL)	21	28	38	Ω
			Iol = 12 mA (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

4

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: Ta = 0 °C to 70 °C, V_{cc} = 5.0V ±5% Military: Ta = -55 °C to +125 °C, V_{cc} = 5.0V ±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted.

Symbol	Description	Notes (1)	245, 640, 2245, 2640		245A, 640A, 2245A, 2640A		245C, 2245C		245D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} t _{PLH}	Propagation Delay A _i to/from B _i , 245,640	COM	1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	ns
		MIL	1.5	7.5	1.5	4.9					
	Propagation Delay A _i to/from B _i , 2245,2640	COM	1.5	7	1.5	4.6	1.5	4.1			
		MIL	1.5	7.5	1.5	4.9					
t _{PZH} t _{PZL}	Output Enable Time OE, T/R to A/B, 245,640	COM	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.6	
		MIL	1.5	10	1.5	6.5					
	Output Enable Time OE, T/R to A/B, 2245,2640	COM	1.5	9.5	1.5	6.2	1.5	5.8			
		MIL	1.5	10	1.5	6.5					
t _{PHZ} t _{PLZ}	Output Disable Time OE, T/R to A/B	COM	2	1.5	7.5	1.5	5	1.5	4.5	1.5	4.5
		MIL	2	1.5	10	1.5	6				

Notes:

1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, I _{in} = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
I _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, I _{in} = 0 (2)	-	5.0	mA
I _{cc}	Supply Current per Input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mW/mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{in} = 3.4V).
3. For flipflops I_{cc} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or faster capacitance. This parameter is guaranteed by design but not tested.
4. I_{cc} can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_a = 0°C to 70°C, V_{cc} = 5.0V ± 5%, Military: T_a = -55°C to +125°C, V_{cc} = 5.0V ± 10%
 C_{load} = 50 pF, R_{load} = 500Ω unless otherwise noted.

Symbol	Description	Notes (1)	245, 240, 2245, 2640				245A, 240A, 2245A, 2640A				245C, 2245C				245D				Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} t _{PLH}	Propagation Delay At t _{form} 0V, 245, 240	COM	1.5	7	1.5	4.5	1.5	4.5	1.5	4.1	1.5	4.1	1.5	3.8	1.5	3.8	1.5	3.8	ns
		MIL	1.5	7.5	1.5	4.5	1.5	4.5	1.5	4.1	1.5	4.1	1.5	3.8	1.5	3.8	1.5	3.8	
	Propagation Delay At t _{form} 0V, 2245, 2640	COM	1.5	7	1.5	4.5	1.5	4.5	1.5	4.1	1.5	4.1	1.5	3.8	1.5	3.8	1.5	3.8	
		MIL	1.5	7.5	1.5	4.5	1.5	4.5	1.5	4.1	1.5	4.1	1.5	3.8	1.5	3.8	1.5	3.8	
t _{PLZ} t _{PHZ}	Output Enable Time OE, TR to AV, 245, 240	COM	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns
		MIL	1.5	10	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	
	Output Enable Time OE, TR to AV, 2245, 2640	COM	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	
		MIL	1.5	10	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	
t _{PLZ} t _{PHZ}	Output Disable Time OE, TR to AV	COM	1.5	7.5	1.5	8	1.5	8	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	ns
		MIL	1.5	10	1.5	8	1.5	8	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	

- Notes:
1. Minimum propagation delay values are guaranteed but not tested.
 2. This parameter is guaranteed but not tested.



High-Speed CMOS 8-Bit Register with Asynchronous Reset

QS54/74FCT273T

QS54/74FCT2273T

FEATURES/BENEFITS

- Pin and function compatible to the 74F273 74FCT 273 and 74FCT273T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 273T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 5.2ns tPD for C
- Iol = 48 mA Com., 32 mA Mil.

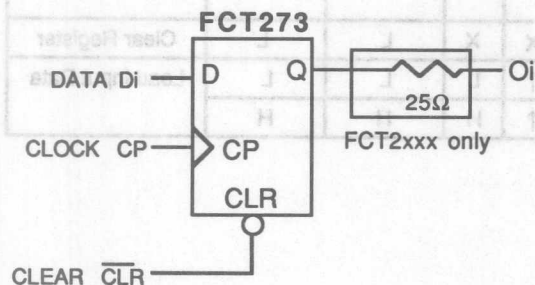
FCT-T 2273T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and C speed grades with 5.2ns tPD for C
- Iol = 12mA Com.

DESCRIPTION

The QSFCT273T and QSFCT2273T are high speed CMOS TTL-compatible registers with an asynchronous reset input. They are eight -bit registers with a buffered common clock and a buffered output drive. The QSFCT2273T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock. The high output current Iol and Ioh drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

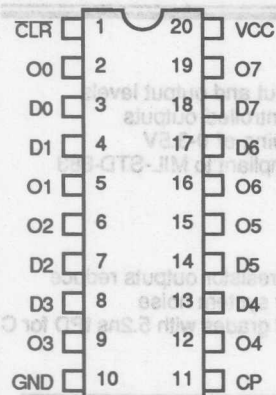


Name	I/O	Description
Q	O	Data Output
CP	I	Clock Input
CLR	I	Clear Input

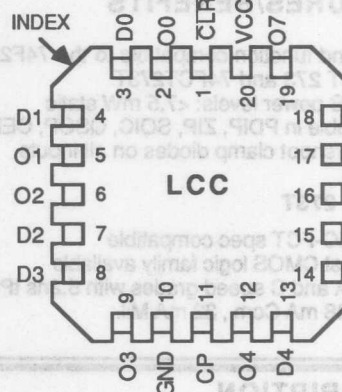
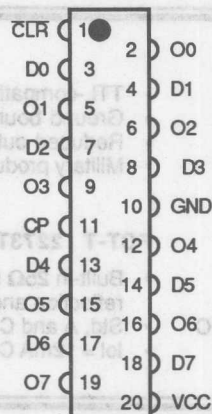
PIN CONFIGURATIONS

FCT273, 2273

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

PIN DESCRIPTION AND FUNCTION TABLE

FCT273, 2273

Name	I/O	Description
Di	I	Data Inputs
O _i	O	Data Outputs
CP	I	Clock Input
CLR	I	Clear Input

Inputs			Internal Q Value	Outputs	Function
CLR	CP	Di		O _i	
L	X	X	L	L	Clear Register
H	↑	L	L	L	Load Input Data
H	↑	H	H	H	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Unit
V_{IH}	Input High Voltage	V
V_{IL}	Input Low Voltage	V
ΔV_I	Input Hysteresis	V
I_{IH}	Input Current	mA
I_{IL}	Input Current	mA
I_{OH}	Output Current	mA
I_{OL}	Output Current	mA
V_{OC}	Output Voltage	V
R_{OH}	Output Resistance	Ω
R_{OL}	Output Resistance	Ω

Notes:
1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is 21 second.
3. These parameters are guaranteed by design but not tested.

QS273T, 2273T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{cc}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_I = 3.4V)
3. For flipflops Q_{cc} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	273, 2273		273A, 2273A		273C, 2273C		Unit
			Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay CP, CLR to Oi, 273	Com	2	13	2	7.2	2	5.2	ns
t _{PLH}		MII	2	15	2	8.3			
	Propagation Delay CP, CLR to Oi, 2273	Com	2	13	2	7.2	2	5.2	
		MII	2	15	2	8.3			
t _S	Data Setup Time Di to CP	Com	3		2		1.5		
		MII	3.5		2				
t _H	Data Hold Time Di to CP	Com	2		1.5		1		
		MII	2		1.5				
t _{WCP}	Clock Pulse Width HIGH or LOW	Com	2	7	6		4		
		MII		7	6				
t _{WCLR}	CLR Pulse Width HIGH or LOW	Com	2	7	6		5		
		MII		7	6				
t _{REC}	CLR Recovery Time CLR to CP	Com	2	4	2		1.5		
		MII		5	2.5				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High Speed CMOS 9-Bit Parity Generator/Checker

QS54/74FCT280T

QS54/74FCT1280T

FEATURES/BENEFITS

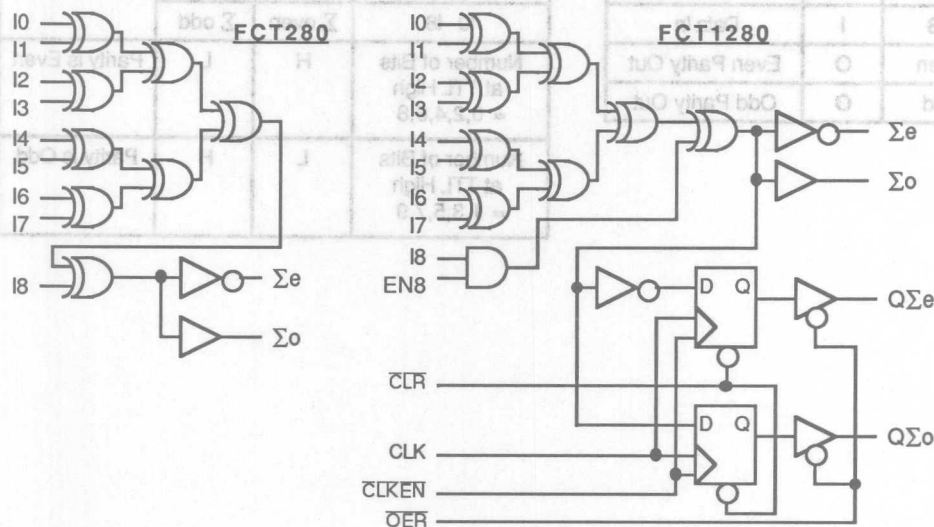
- QSFCT280BT faster than FAST™
- QSFCT1280T has I8 enable, registered outputs
- I_{OL}=48 mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Military product compliant with MIL-STD 883
- 6.3 ns delay, I_x to Σ_e for QSFCT280BT
- 2 ns setup, I_x to reg clock for QSFCT1280BT
- CMOS power levels < 7.5 mW static
- Available in PDIP, ZIP, SOIC, CERDIP, LCC, QSOP
- JEDEC standard pinouts

DESCRIPTION

The QSFCT280/AT/BT and QSFCT1280/AT/BT are high speed CMOS TTL-compatible 9-bit parity generator-checkers. Both odd and even parity outputs are available for generating or checking odd or even parity. The 1280 has I8 enable for parity bit generation and registered odd and even outputs for parity check on the following cycle. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

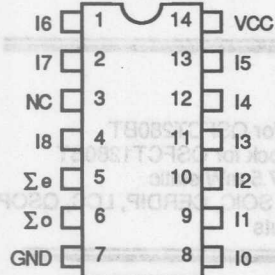
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FUNCTIONAL BLOCK DIAGRAM

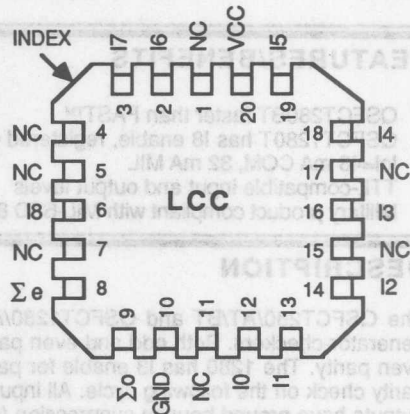
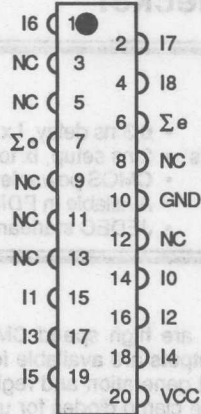


FCT280 PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ZIP



PIN DESCRIPTION

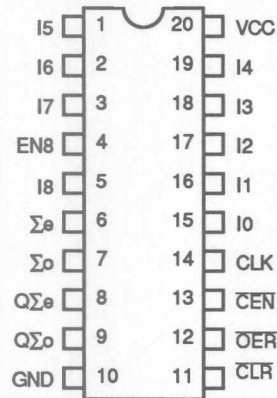
Pin	Name	I/O	Description
10 - 18	I	I	Data In
Σ even	O	O	Even Parity Out
Σ odd	O	O	Odd Parity Out

FUNCTION TABLE

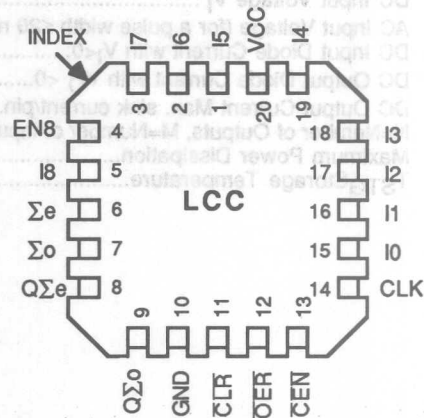
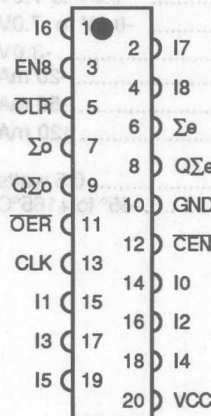
Inputs	Outputs		Function
	Σ even	Σ odd	
Number of Bits at TTL High = 0,2,4,6,8	H	L	Parity is Even
Number of Bits at TTL High = 1,3,5,7,9	L	H	Parity is Odd

FCT1280 PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
I0 - I8	I	Data In
EN8	I	Enable I8
CLK	I	Clock
CEN	I	Clock Enable
CLR	I	Clear
OER	I	Reg Out Enable
Σe	O	Even Parity Out
Σo	O	Odd Parity Out
QΣe	O	Reg even Parity
QΣo	O	Reg odd Parity

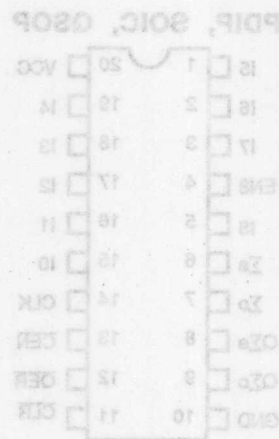
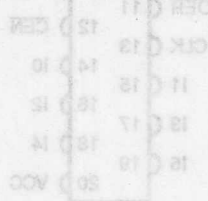
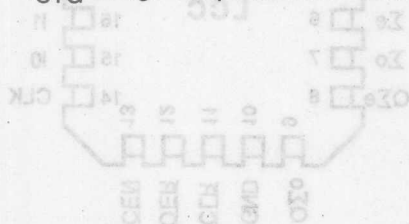
FUNCTION TABLE

Inputs			Outputs	
I0 - I7	I8	EN8	Σe	Σo
Number of Bits at TTL High = 0,2,4,6,8	X	L	H	L
	L	H	H	L
	H	H	L	H
Number of Bits at TTL High = 1,3,5,7	X	L	L	H
	L	H	L	H
	H	H	H	L

Inputs				Outputs		Function
OER	CEN	CLR	CLK	QΣe	QΣo	
H	X	X	X	Hi-Z	Hi-Z	Disable
L	X	L	X	L	L	Clear
L	H	H	↑	QΣen-1	QΣon-1	No Change
L	L	H	↑	Σen-1	Σon-1	Load Σe, Σo

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C



ALL PINS TOP VIEW

FUNCTION TABLE

Inputs		Outputs	
10-17	18-19	20-21	22-23
Number of Bits at TTL High = 0,2,4,8,8	X	L	H
	L	H	L
	H	H	L
Number of Bits at TTL High = 1,3,5,7	X	L	H
	L	H	L
	H	H	L

Inputs		Outputs		Function
24-25	26-27	28-29	30-31	
H	X	X	X	Disable
L	X	L	X	Clear
L	H	H	H	No Change
L	L	H	H	Load 28, 30

PIN DESCRIPTION

Name	I/O	Description
10-18	I	Data In
ENB	I	Enable B
CLK	I	Clock
CEN	I	Clock Enable
CLR	I	Clear
OE	I	Reg Out Enable
2e	O	Even Parity Out
2o	O	Odd Parity Out
Q2e	O	Reg even Parity
Q2o	O	Reg odd Parity

CAPACITANCE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
FCT280						
TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V						
Pin	SOIC	QSOP	PDIP,LCC	ZIP	Unit	
1,2,4,8-13	4	4	5	7	pF	
5,6	6	6	7	9	pF	
8	8	8	9	10	pF	

Note: Capacitance is characterized but not tested

FCT1280

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pin	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-5,11-19	4	4	5	7	pF
6-9	6	6	7	9	pF
8	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
FCT280 (S20)						
Voc = MIN						
Pin	SOIC	QSOP	PDIP,LCC	ZIP	Unit	
1,2,4,8-13	4	4	5	7	pF	
5,6	6	6	7	9	pF	
8	8	8	9	10	pF	

Notes:
1. Typical values indicate Voc = 5.0V and TA = 25°C.
2. Not more than one output should be shorted and the duration is 21 second.
3. These parameters are guaranteed by design but not tested.

QS280T, 1280T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA (MIL)}$	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA (COM)}$	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 48 \text{ mA (COM)}$	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 12 \text{ mA (COM)}$	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	21	28	38	Ω
			$I_{ol} = 12 \text{ mA (COM)}$	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or: V _{CC} - 0.2V ≤ V _{in} ≤ V _{CC}	-	1.5	mA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{CCd}	Supply Current per input per mHz	V _{CC} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{CC} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qcqd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

QS280T, 1280T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes (1)	280T 1280T		280AT 1280AT		280BT 1280BT		Unit
				Min	Max	Min	Max	Min	Max	
† PHLE † PLHE	Propagation Delay I0 - I8 to Σ even	Com		-	10	-	7.5	-	6.3	ns
		Mil		-	11	-	9	-		
† PHLO † PLHO	Propagation Delay I0 - I8 to Σ odd	Com		-	10	-	7.5	-	6.3	
		Mil		-	11	-	9	-		
1280 Only										
† OE	Output Enable Time ROE to Q Σ e, Q Σ o	Com		1.5	12.5	-	1.5	-	7.5	ns
		Mil		1.5	14	-	1.5	-		
† OZ	Output Disable Time ROE Q Σ e, Q Σ o	Com	2	1.5	8	-	1.5	-	6.5	
		Mil	2	1.5	8	-	1.5	-		
† CPQ	Clock to Output Q Σ e, Q Σ o	Com		-	10	-	9	-	7.5	
		Mil		-	11	-	10	-		
† CLR	CLR to Output Q Σ e, Q Σ o	Com		-	13	-	11	-	8	
		Mil		-	15	-	13	-		
† CS	CEN Setup Time CEN to CLK	Com		2.5	-	2	-	2	-	
		Mil			-		-			
† CH	CEN Hold Time CEN to CLK	Com		3	-	2.5	-	2	-	
		Mil			-		-			
† S	Data Setup Time I _x to CLK	Com		2.5	-	2	-	2	-	
		Mil			-		-		-	
† H	Data Hold Time I _x to CLK	Com		3	-	2.5	-	2	-	
		Mil			-		-		-	
† W	Clock Pulse Width High or Low	Com	2	7	-	7	-	5	-	
		Mil	2	7	-	7	-	6	-	

Notes:

1. See test circuits and wave forms.
2. This parameter guaranteed by design but not tested.



High-Speed CMOS 8-bit Universal Shift Register

QS54/74FCT299T

QS54/74FCT2299T

FEATURES/BENEFITS

- Pin and function compatible to the 74F299
- 74FCT 299 and 74FCT299T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 299T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Standard and A speed grades with 9.5ns tPD for A
- IOL = 48 mA Com., 32 mA Mil.

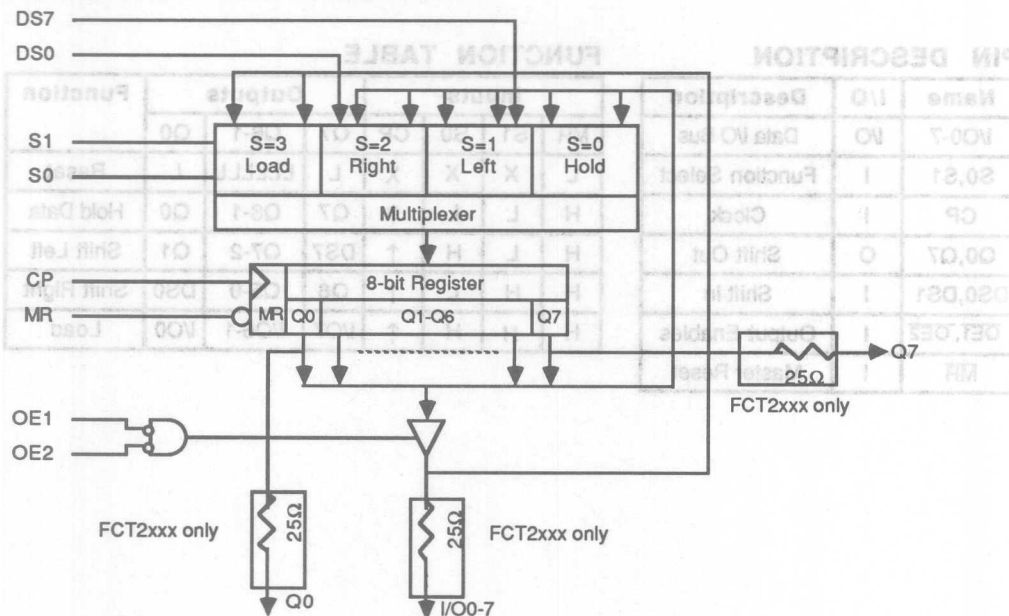
FCT-T 2299T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 9.5ns tPD for A
- IOL = 12mA Com.

DESCRIPTION

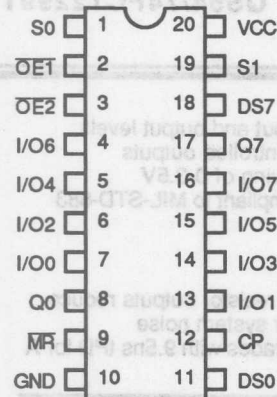
The QSFCT299T and QSFCT2299T are high speed CMOS 8-bit universal shift registers. The contents of the 8-bit register may be loaded from a bus, shifted left or right, or gated to the bus. The 2191 is a 25Ω resistor output version of the 299, and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM

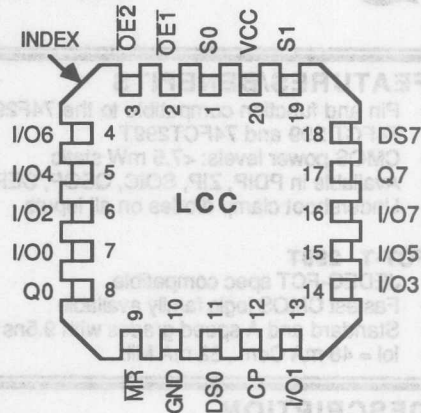
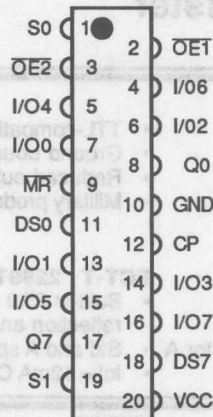


PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

The QS299T and QS2299T are high speed CMOS 8-bit universal shift registers. The contents of the 8-bit register may be loaded from a bus, shifted left or right or gated to the bus. The QS299T is a 250 resistor output version of the QS99, and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QS1 Application Note AN-001).

PIN DESCRIPTION

Name	I/O	Description
I/O0-7	I/O	Data I/O Bus
S0,S1	I	Function Select
CP	I	Clock
Q0,Q7	O	Shift Out
DS0,DS1	I	Shift In
OE1,OE2	I	Output Enables
MR	I	Master Reset

FUNCTION TABLE

Inputs				Outputs			Function
MR	S1	S0	CP	Q7	Q6-1	Q0	
L	X	X	X	L	LLLLLL	L	Reset
H	L	L	↑	Q7	Q6-1	Q0	Hold Data
H	L	H	↑	DS7	Q7-2	Q1	Shift Left
H	H	L	↑	Q6	Q5-0	DS0	Shift Right
H	H	H	↑	I/O7	I/O6-1	I/O0	Load

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-3,9,11,12,18,19	4	4	5	7	pF
8,17	6	6	7	9	pF
4-7,13-16	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Test Conditions	Typical Value	Unit
V_{IH}	Input High Voltage	$V_{CC} = \text{MAX}$, $I_{IH} \leq 1\text{ mA}$	2.0	V
V_{IL}	Input Low Voltage	$V_{CC} = \text{MAX}$, $I_{IL} \leq 1\text{ mA}$	0.8	V
ΔV_I	Input Hysteresis	$V_{CC} = \text{MAX}$, $I_{IH} \leq 1\text{ mA}$	0.1	V
I_{IH}	Input Current (HIGH)	$V_I = V_{CC}$, $V_O = 0\text{V}$	1.0	mA
I_{IL}	Input Current (LOW)	$V_I = 0\text{V}$, $V_O = V_{CC}$	1.0	mA
I_{OH}	Output Current (HIGH)	$V_O = V_{CC} - 0.1\text{V}$, $I_{IH} \leq 1\text{ mA}$	120	mA
I_{OL}	Output Current (LOW)	$V_O = 0.1\text{V}$, $I_{IL} \leq 1\text{ mA}$	120	mA
$R_{DS(on)}$	Output Resistance	$V_{GS} = 10\text{V}$, $V_{DS} = 0.1\text{V}$	0.1	Ω

Notes:
 1. Typical values indicate $V_{CC} = 5\text{V}$ and $T = 25^\circ\text{C}$.
 2. Not more than one output should be shorted and the duration is 10 seconds.
 3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$ $I_{oh} = 12 \text{ mA}$ (MIL) $I_{oh} = 15 \text{ mA}$ (COM)	2.4 2.4	- -	- -	Volts
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$ $I_{ol} = 32 \text{ mA}$ (MIL) $I_{ol} = 48 \text{ mA}$ (COM)	- -	- -	0.50 0.50	
		$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA}$ (MIL) $I_{ol} = 12 \text{ mA}$ (COM)	- -	- -	0.50 0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA}$ (MIL) $I_{ol} = 12 \text{ mA}$ (COM)	- -	- -	0.50 0.50	
		$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA}$ (MIL) $I_{ol} = 12 \text{ mA}$ (COM)	21 24	28 28	38 35	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA}$ (MIL) $I_{ol} = 12 \text{ mA}$ (COM)	21 24	28 28	38 35	Ω

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%

Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	299 2299		299A 2299A		Unit
			Min	Max	Min	Max	
t CPQ	Propagation Delay CP to Qi	COM	2	10	2	7.2	ns
		MIL	2	14	2	9.5	
tCPI	Propagation Delay CP to I/O	COM	2	12	2	7.2	
		MIL	2	12	2	9.5	
t MRQ	Propagation Delay MR to Qi	COM	2	10	2	7.2	
		MIL	2	10.5	2	9.5	
tMRI	Propagation Delay MR to I/O	COM	2	15	2	8.7	
		MIL	2	15	2	11.5	
t PZH/L	Output Enable Time OE to I/O	COM	1.5	11	1.5	6.5	
		MIL	1.5	15	1.5	7.5	
tPHZ,LZ	Output Disable Time OE to I/O	COM	1.5	7	1.5	5.5	
		MIL	1.5	9	1.5	6.5	
t S4	Setup Time SO, SI to CP	COM	7.5		3.5		
		MIL	7.5		4.0		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High-Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT373T
QS54/74FCT533T

QS54/74FCT2373T
QS54/74FCT2533T

FEATURES/BENEFITS

- Pin and function compatible to the 74F373/533 and 74FCT373T/533T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 373T, 533T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. , A , C, and D speed grades with 4.2ns for D
- I_{OL} = 48 mA Com., 32 mA Mil.

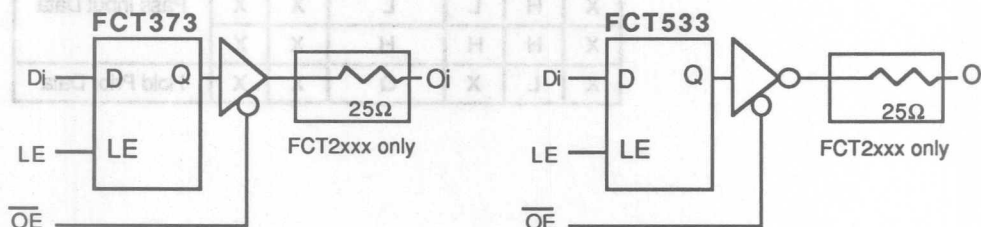
FCT-T 2373T, 2533T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. , A , C, & D speed grades with 4.2ns for D
- I_{OL} = 12mA Com.

DESCRIPTION

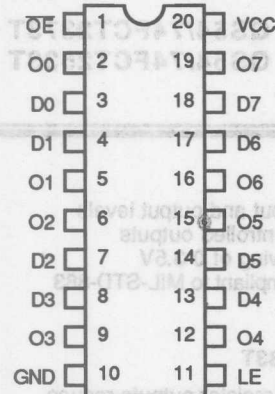
The QSFCT373T and QSFCT533T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2373/533 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2373 and 2533 series parts can replace the 373 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

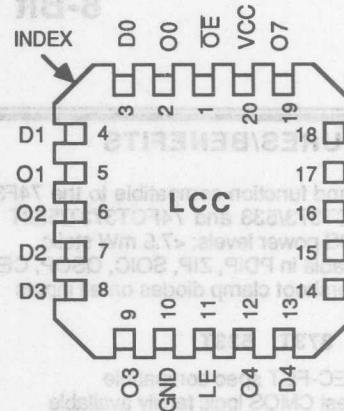
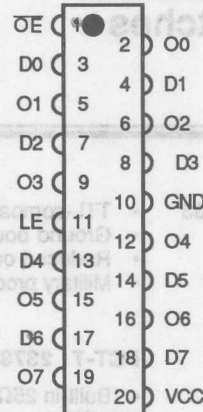


PINOUTS

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

PIN DESCRIPTION AND FUNCTION TABLE

FCT373, 2373

Name	I/O	Description	Inputs			Internal Q Value	Outputs		Function
			OE	LE	Di		373	533	
Di	I	Data Inputs					Oi	Oī	
Oi	O	Data Outputs							
LE	I/O	Latch Enable							
OE	I/O	Output Enable							
			H	X	X	X	Z	Z	Disable Outputs
			L	X	X	H	H	L	Enable Outputs
			L	X	X	L	L	H	
			X	H	L	L	X	X	Pass Input Data
			X	H	H	H	X	X	
			X	L	X	Q	X	X	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T _{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Test Conditions	Typical Value	Unit
V_{IH}	Input High Voltage	$V_{CC} = 5V, V_{OL} = 0V$	1.5	V
V_{IL}	Input Low Voltage	$V_{CC} = 5V, V_{OL} = 0V$	0.5	V
ΔV_I	Input Hysteresis	$V_{CC} = 5V, V_{OL} = 0V$	0.1	V
I_{IH}	Input Current (HIGH)	$V_I = 5V, V_{CC} = 5V$	1	mA
I_{IL}	Input Current (LOW)	$V_I = 0V, V_{CC} = 5V$	1	mA
I_{OZ}	Output Current (Z)	$V_O = 0V, V_{CC} = 5V$	1	mA
C_{in}	Input Capacitance	$V_I = 0V, V_{CC} = 5V$	5	pF
C_{out}	Output Capacitance	$V_O = 0V, V_{CC} = 5V$	5	pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18\text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12\text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15\text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32\text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48\text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12\text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12\text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12\text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12\text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.

2. Not more than one output should be shorted and the duration is ≤ 1 second.

3. These parameters are guaranteed by design but not tested.

QS373T, 533T, 2373T, 2533T

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

1. For conditions shown a MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

QS373T, 533T, 2373T, 2533T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Clload = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes	373		373A		373C,		373D		Unit
			2373	533	2373A	533A	2373C	533C	2373D	533D	
		(1)	2533		2533A		2533C				
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Oi, 373	COM	1.5	8	1.5	5.2	1.5	4.7	1.5	4.2	ns
		MIL	2	8.5	1.5	5.6					
	Propagation Delay Data to Oi, 2373	COM	1.5	8	1.5	5.2	1.5	4.7	1.5	4.2	
		MIL	2	8.5	1.5	5.6					
t_{PHLE} t_{PLHE}	Propagation Delay LE high to Oi, 373	COM	2	13	2	8.5	2	6.9	1.5	6.3	
		MIL	2	14	2	9.8					
	Propagation Delay LE high to Oi, 2373	COM	2	13	2	8.5	2	6.9	1.5	6.3	
		MIL	2	14	2	9.8					
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi, 373	COM	1.5	11	1.5	6.5	1.5	5.5	1.5	5.5	
		MIL	1.5	12.5	1.5	7.5					
	Output Enable Time $\overline{OE}$ to Yi, 2373	COM	1.5	11	1.5	6.5	1.5	6.2	1.5	6.2	
		MIL	1.5	12.5	1.5	7.5					
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	COM	2	1.5	7	1.5	5.5	1.5	5.0	1.5	5.0
		MIL	2	1.5	8.5	1.5	6.5				
t_S	Data Setup Time Di to LE hi to low	COM	2		2		2		2		
		MIL	2		2						
t_H	Data Hold Time Di to LE hi to low	COM	1.5		1.5		1.5		1.5		
		MIL	1.5		1.5						
t_W	LE Pulse Width HIGH or LOW	COM	2	6	5		4		4		
		MIL	2	6	6						

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High-Speed CMOS Bus Interface 8-Bit Registers

QS54/74FCT374T

QS54/74FCT534T

QS54/74FCT2374T

QS54/74FCT2534T

FEATURES/BENEFITS

- Pin and function compatible to the 74F374/534 and 74FCT374T/534T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 374T, 534T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A, C, & D speed grades with 4.5 ns tPD for D
- Iol = 48 mA Com., 32 mA Mil.

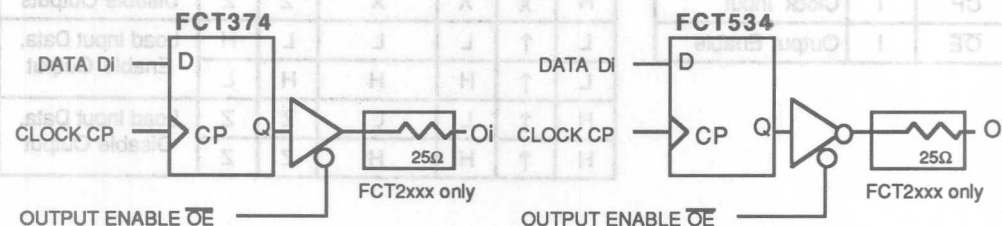
FCT-T 2374T, 2534T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and C speed grades with 5.2 ns tPD for C
- Iol = 12mA Com.

DESCRIPTION

The QSFCT374T and QSFCT534T are high speed CMOS TTL-compatible buffered registers. They are eight-bit registers with a buffered common clock and a buffered output enable control. The QSFCT2374T and QSFCT2534T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock. The FCT374 is a non-inverting device, and the FCT534 is an inverting device. The high output current Iol and Ioh drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

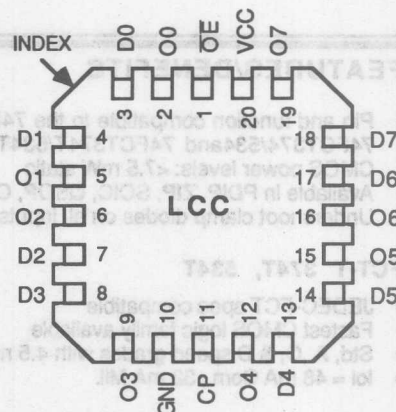
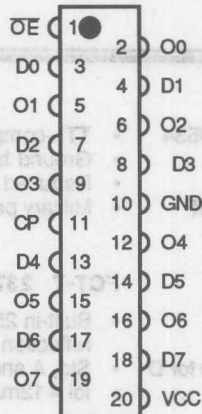
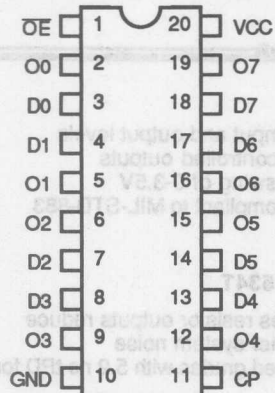


PIN CONFIGURATIONS

FCT374, 534, 2374, 2534

PDIP, SOIC, QSOP

ZIP



ALL PINS TOP VIEW

PIN DESCRIPTION AND FUNCTION TABLE

FCT374, 534, 2374, 2534

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CP	I	Clock Input
OE	I	Output Enable

Inputs			Internal Q Value	Outputs		Function
OE	CP	Di		374 Oi	534 Oi	
H	X	X	X	Z	Z	Disable Outputs
L	↑	L	L	L	H	Load Input Data, Enable Output
L	↑	H	H	H	L	
H	↑	L	L	Z	Z	Load Input Data, Disable Output
H	↑	H	H	Z	Z	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
_____	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Pin	Output HIGH Voltage			Output LOW Voltage		
	V_{OH}	V_{OL}	V_{OL}	V_{OH}	V_{OL}	V_{OL}
1,3,4,7,8,11,13,14,17,18	2.4	0.20	0.20	2.4	0.20	0.20
2,5,6,9,12,15,16,19	2.4	0.20	0.20	2.4	0.20	0.20
_____	2.4	0.20	0.20	2.4	0.20	0.20

Notes:
1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be loaded and the duration is 21 seconds.
3. These parameters are guaranteed by design but not tested.

QS374T, 534T, 2374T, 2534T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

QS374T, 534T, 2374T, 2534T

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown a MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

(3) This parameter is guaranteed by design but not tested.

QS374T, 534T, 2374T, 2534T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Load = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	374 534 2374 2534		374A 534A 2374A 2534A		374C 534C 2374C 2534C		374D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t PHL t PLH	Propagation Delay CP to Oi, 374/534	COM	2	10	2	6.5	2	5.2	1.5	4.5	ns
		MIL	2	11	2	7.2					
	Propagation Delay CP to Oi, 2374/2534	COM	2	10	2	6.5	2	5.2			
		MIL	2	11	2	7.2					
t PZH t PZL	Output Enable Time OE to Yi, 374/534	COM	1.5	12.5	1.5	6.5	1.5	5.5	1.5	5.5	
		MIL	1.5	14	1.5	7.5					
	Output Enable Time OE to Yi, 2374/2534	COM	1.5	12.5	1.5	6.5	1.5	6.2			
		MIL	1.5	14	1.5	7.5					
t PHZ t PLZ	Output Disable Time OE to Yi	COM	2	1.5	8	1.5	5.5	1.5	5	1.5	5
		MIL	2	1.5	8	1.5	6.5				
t S	Data Setup Time Di to CP	COM	2		2		1.5		1.5		
		MIL	2		2						
t H	Data Hold Time Di to CP	COM	1.5		1.5		1		1		
		MIL	1.5		1.5						
t W	Clock Pulse Width HIGH or LOW	COM	2	7	5		4		4		
		MIL	2	7	6						

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High-Speed CMOS 8-Bit Register with Clock Enable

QS54/74FCT377T

QS54/74FCT2377T

FEATURES/BENEFITS

- Pin and function compatible to the 74F377 74FCT377 and 74FCT377T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 377T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 5.2ns tPD for C
- Iol = 48 mA Com., 32 mA Mil.

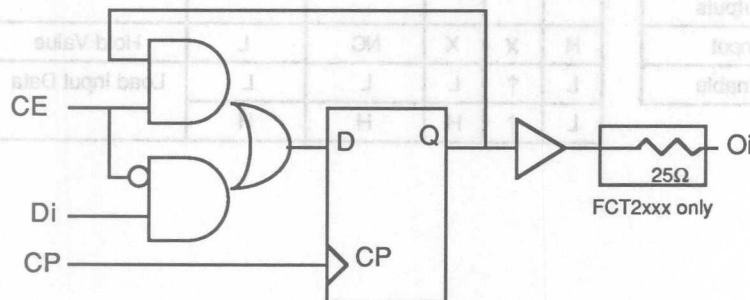
FCT-T 2377T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A & C speed grades with 5.2ns tPD for C
- Iol = 12mA Com.

DESCRIPTION

The QSFCT377T and QSFCT2377T are high speed CMOS TTL-compatible registers. They are eight-bit registers with a buffered common clock, a buffered output drive and a synchronous clock enable. The QSFCT2377T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock if the clock enable input is active. The high output current Iol and Ioh drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

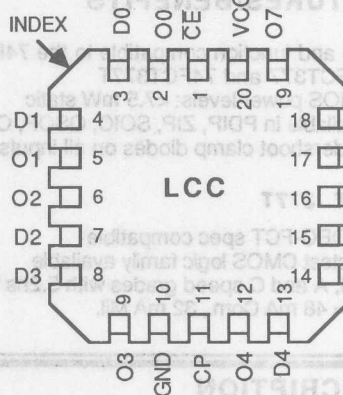
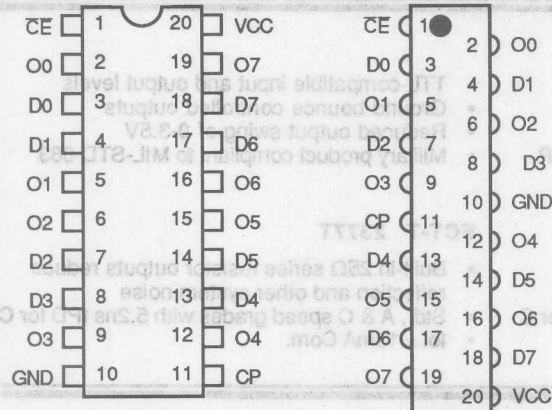


PIN CONFIGURATIONS

FCT377, 2377

PDIP, SOIC, QSOP

ZIP



ALL PINS TOP VIEW

The QS377T and QS2377T are high speed CMOS 1T-compatible registers. They are eight-bit registers with a buffered common clock, a buffered output drive and a synchronous clock enable. The QS2377T is a 520 resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock if the clock enable input is active. The high output current and low drive high capacitance loads. All inputs have clamping diodes for undershoot noise suppression. All outputs have a high impedance state when the clock enable is low and outputs will not load an output driver. Note AN-001, and outputs will not load an output driver.

PIN DESCRIPTION AND FUNCTION TABLE

FCT377, 2377

Name	I/O	Description
Di	I	Data Inputs
O _i	O	Data Outputs
CP	I	Clock Input
CE	I	Clock Enable

Inputs			Internal Q Value	Outputs	Function
CE	CP	Di		O _i	
H	X	X	NC	L	Hold Value
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1,3,4,7,8,11,13,14,17,18	4	4	5	7	pF
2,5,6,9,12,15,16,19	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Pin	Output Resistance (25°C)			Output LOW Voltage (25°C)			Output HIGH Voltage (25°C)		
	$I_{OL} = 12\text{ mA}$ (Min)	$I_{OL} = 12\text{ mA}$ (Typ)	$I_{OL} = 12\text{ mA}$ (Max)	$I_{OL} = 12\text{ mA}$ (Min)	$I_{OL} = 12\text{ mA}$ (Typ)	$I_{OL} = 12\text{ mA}$ (Max)	$I_{OH} = 12\text{ mA}$ (Min)	$I_{OH} = 12\text{ mA}$ (Typ)	$I_{OH} = 12\text{ mA}$ (Max)
1,3,4,7,8,11,13,14,17,18	24	28	32	0.05	0.08	0.10	0.90	0.92	0.95
2,5,6,9,12,15,16,19	24	28	32	0.05	0.08	0.10	0.90	0.92	0.95

Notes:
1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is 21 seconds.
3. These parameters are guaranteed by design but not tested.

QS377T, 2377T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ i_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	μA
i_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
i_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $i_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$i_{oh} = 12 \text{ mA (MIL)}$	2.4	-	-	Volts
			$i_{oh} = 15 \text{ mA (COM)}$	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$i_{ol} = 32 \text{ mA (MIL)}$	-	-	0.50	
			$i_{ol} = 48 \text{ mA (COM)}$	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$i_{ol} = 12 \text{ mA (MIL)}$	-	-	0.50	
			$i_{ol} = 12 \text{ mA (COM)}$	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$i_{ol} = 12 \text{ mA (MIL)}$	21	28	38	Ω
			$i_{ol} = 12 \text{ mA (COM)}$	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

1.5C	Clock Enable Setup Time, CE to CP	COM	3	5	1.5
		MIT	3	5	
1HC	Clock Enable Hold Time, CE to CP	COM	1.5	1.5	1
		MIT	1.5	1.5	
1WCP	Clock Pulse Width, HIGH or LOW	COM	5	7	4
		MIT	7	8	

Notes:
 (1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
 (2) This parameter is guaranteed by design but not tested.

QS377T, 2377T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	377 2377		377A 2377A		377C 2377C		Unit
			Min	Max	Min	Max	Min	Max	
t PHL	Propagation Delay CP to Oi, 377	COM	2	13	2	7.2	2	5.2	ns
t PLH		MIL	2	15	2	8.3			
	Propagation Delay CP to Oi, 2377	COM	2	13	2	7.2	2	5.2	
		MIL	2	15	2	8.3			
t S	Data Setup Times Di to CP	COM	2.5		2		1.5		
		MIL	3		2				
t H	Data Hold Time Di to CP	COM	2		1.5		1		
		MIL	2.5		1.5				
t SC	Clock Enable Setup Time, CE to CP	COM	3		2		1.5		
		MIL	3		2				
t HC	Clock Enable Hold Time CE to CP	COM	1.5		1.5		1		
		MIL	1.5		1.5				
t WCP	Clock Pulse Width HIGH or LOW	COM	2	7	6		4		
		MIL		7	6				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS 8-bit Identity Comparator

QS54/74FCT521T

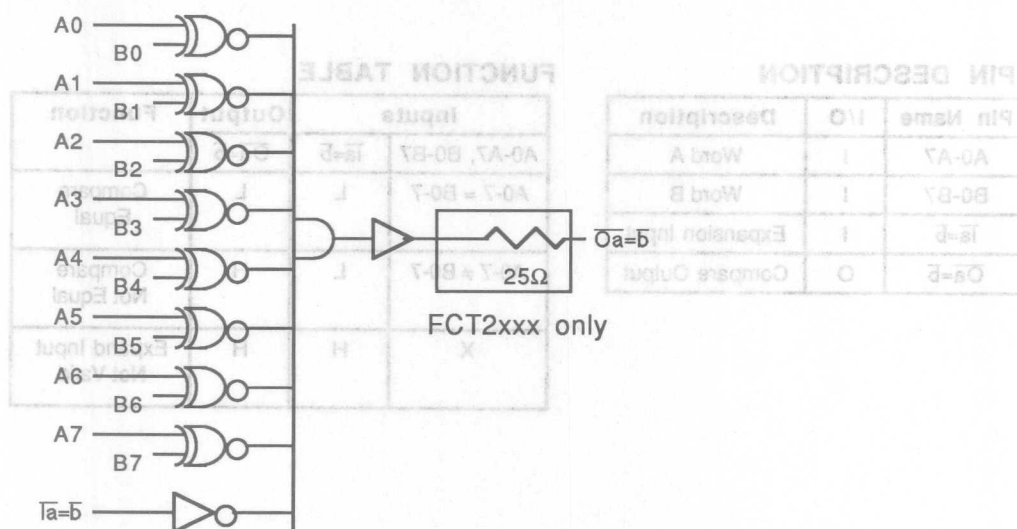
FEATURES/BENEFITS

- QSFCT521B faster than 74F
- $I_{OL}=48$ mA COM, 32 mA MIL
- TTL-compatible input and output levels
- Mil product compliant with MIL-STD 883, Class B
- 4.1ns delay A or B to $\overline{Oa}=b$ for QSFCT521D
- CMOS power levels < 7.5 mW static
- Available in PDIP, ZIP, SOIC, Cerdip, LCC
- JEDEC standard pinouts

DESCRIPTION

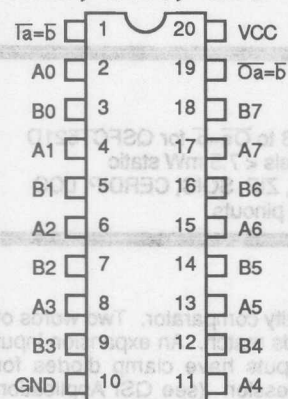
The QSFCT521AT/BT is a high-speed CMOS TTL-compatible 8-bit identity comparator. Two words of up to eight bits are compared and a low output is provided when the words match. An expansion input allows the comparison to be extended over multiple words. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM

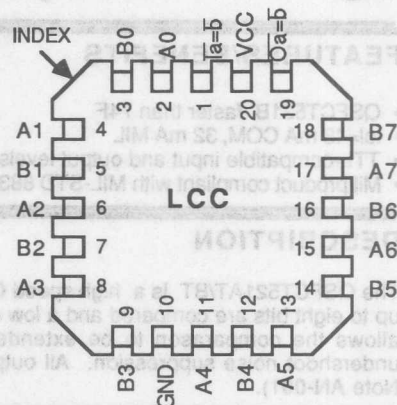
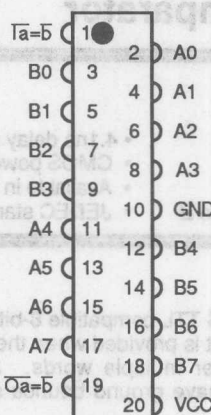


PIN CONFIGURATIONS

PDIP, SOIC, QSOP



ZIP



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
A0-A7	I	Word A
B0-B7	I	Word B
Ta=b	I	Expansion Input
Oa=b	O	Compare Output

FUNCTION TABLE

Inputs		Output	Function
A0-A7, B0-B7	Ta=b	Oa=b	
A0-7 = B0-7	L	L	Compare Equal
A0-7 ≠ B0-7	L	H	Compare Not Equal
X	H	H	Expand Input Not Valid

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pin	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-9, 11-18	4	4	5	7	pF
19	6	6	7	9	pF
20	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Pin	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-9, 11-18	4	4	5	7	pF
19	6	6	7	9	pF
20	8	8	9	10	pF

Notes:
1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is 21 second.
3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	Volts
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	Volts
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	μA
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$ $I_{oh} = 12 \text{ mA (MIL)}$ $I_{oh} = 15 \text{ mA (COM)}$	2.4 2.4	- -	- -	Volts
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$ $I_{ol} = 32 \text{ mA (MIL)}$ $I_{ol} = 48 \text{ mA (COM)}$	- -	- -	0.50 0.50	Volts
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	- -	- -	0.50 0.50	Volts
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	21 24	28 28	38 35	Ω

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70° C, Vcc = 5.0V±5% Military TA = -55° C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted. Units are nanoseconds unless otherwise noted.

Symbol	Description		521		521A		521B		521C		521D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t PHL	Propagation Delay Ai =Bi to Oa=b	Com	1.5	11	1.5	7.2	1.5	5.5	1.5	4.5	1.5	4.1	ns
t PLH		Mil	1.5	15	1.5	9.5	1.5	7.3	1.5	5.1			
t PHLX	Propagation Delay Ia=b to Oa=b	Com	1.5	10	1.5	6	1.5	4.6	1.5	4.1	1.5	3.9	
t PLHX		Mil	1.5	9	1.5	7.8	1.5	6.0	1.5	4.5			

Notes:

1. See test circuits and wave forms.

Q

High Speed CMOS 8-Bit Buffers/Line Drivers

QS54/74FCT540T

QS54/74FCT541T

QS54/74FCT2540T

QS54/74FCT2541T

FEATURES/BENEFITS

- Pin and function compatible to the 74F540/1, 74FCT540/1 and 74FCT540T/1T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T540T/1T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Standard and A speed grades with 5.1ns tPD for A
- Iol = 64 mA Com., 48mA Mil.

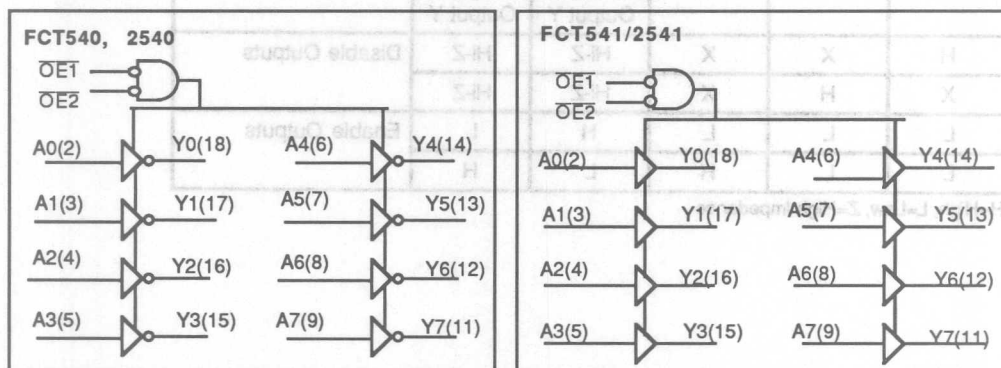
FCT-T 2540T/1T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.1ns tPD for A
- Iol = 12mA Com.

DESCRIPTION

The QSFCT540T and QSFCT541T are 8-bit buffers/line drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2540 series parts can replace the 540 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



QSFCT540T, 541T, 2540T, 2541T

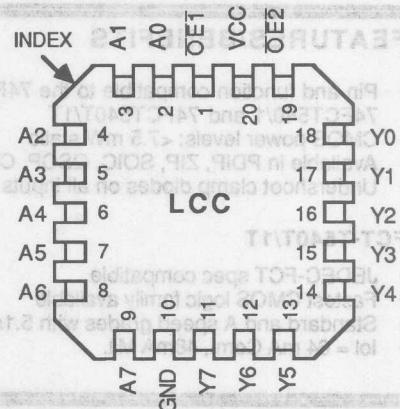
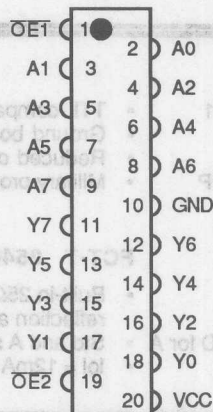
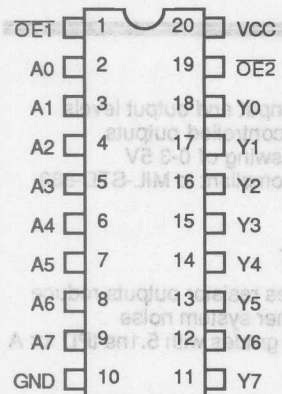
PINOUTS

FCT540/541

FCT2540/2541

PDIP, SOIC, QSOP

ZIP



ALL PINS TOP VIEW

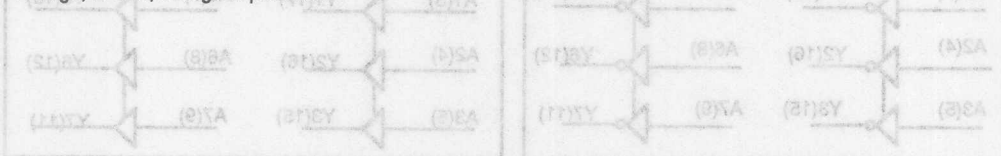
The QSFCT540T and QSFCT541T are 8-bit bufferline drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 8-bit bufferline drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 8-bit bufferline drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The FCT2540 and FCT2541 are 8-bit bufferline drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses.

FUNCTION TABLES

FCT540/2540, FCT541/2541

OE1	OE2	Input A	540	541	Function
			Output Y	Output Y	
H	X	X	Hi-Z	Hi-Z	Disable Outputs
X	H	X	Hi-Z	Hi-Z	
L	L	L	H	L	Enable Outputs
L	L	H	L	H	

H=High, L=Low, Z=High Impedance



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Input Diode Current with $V_I > V_{CC}$	20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Diode Current with $V_O > V_{CC}$	50 mA
DC Output Current Max. sink current/pin.....	70 mA
DC Output Current Max. source current/pin.....	30 mA
Total DC Ground Current.....	($N \times I_{OL} + M \times I_{CC}$) mA
Total DC VCC Power Supply Current.....	($N \times I_{OH} + M \times I_{CC}$) mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

	Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
	1,19	4	4	5	7	pF
		6	6	7	9	pF
	2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

V _{OL}	0.25	-	-	I _{OL} = 48 mA (MIL)	V _{CC} = MIN	Output LOW Voltage
	0.55	-	-	I _{OL} = 84 mA (COM)	V _{CC} = MIN	Output LOW Voltage
	0.50	-	-	I _{OL} = 12 mA (MIL)	V _{CC} = MIN	Output LOW Voltage
	0.50	-	-	I _{OL} = 12 mA (COM)	V _{CC} = MIN	Output LOW Voltage
R _{OUT}	88	88	88	I _{OL} = 12 mA (MIL)	V _{CC} = MIN	Output Resistance
	38	38	38	I _{OL} = 12 mA (COM)	V _{CC} = MIN	Output Resistance

- Notes:
1. Typical values indicate $V_{CC} = 5.0V$ and $T_A = 25^\circ\text{C}$.
 2. Not more than one output should be shorted and the duration is 21 second.
 3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$				Volts
		$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	
		$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$				
		$I_{ol} = 48 \text{ mA}$ (MIL)	-	-	0.55	
		$I_{ol} = 64 \text{ mA}$ (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$				
		$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
		$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$				Ω
		$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	
		$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

Symbol	Description	Notes (1)	541, 541T				2541, 2541T				Unit
			Com		Min		Com		Min		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay A to Y, FCT541	1.5	8	1.5	9	1.5	4.8	1.5	4.8	1.5	ns
t _{PLH}	Propagation Delay A to Y, FCT541	1.5	8	1.5	9	1.5	4.8	1.5	4.8	1.5	ns
t _{PSH}	Output Enable Time OE to Y, FCT541	1.5	10	1.5	10.5	1.5	8.5	1.5	8.5	1.5	ns
t _{PZL}	Output Enable Time OE to Y, FCT541	1.5	10	1.5	10.5	1.5	8.5	1.5	8.5	1.5	ns
t _{PZH}	Output Disable Time OE to Y	1.5	8.5	1.5	12.5	1.5	8.5	1.5	8.5	1.5	ns

Notes:
1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Clod = 50 pF, Rload = 500 Ω unless otherwise noted

FCT540/A, FCT2540/A

Symbol	Description	Notes (1)	540, 2540				540A, 2540A				Unit
			Com		MII		Com		MII		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPHL tPLH	Propagation Delay Ai to Yi, 540		1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	ns
	Propagation Delay Ai to Yi, 2540		1.5	8	1.5	9	1.5	4.8	1.5	5.1	
tPZH tPZL	Output Enable Time OE to Yi, 540		1.5	10	1.5	10.5	1.5	6.2	1.5	6.5	
	Output Enable Time OE to Yi, 2540		1.5	10	1.5	10.5	1.5	6.2	1.5	6.5	
tPHZ tPLZ	Output Disable Time OE to Yi	2	1.5	9.5	1.5	12.5	1.5	5.6	1.5	5.9	

Notes: 1. Minimum propagation delay values are guaranteed but not tested.
 2. This parameter is guaranteed but not tested.

FCT541/A, FCT2541/A

Symbol	Description	Notes (1)	541, 2541				541A, 2541A				Unit
			Com		MII		Com		MII		
			Min	Max	Min	Max	Min	Max	Min	Max	
† PHL † PLH	Propagation Delay Ai to Yi, FCT541		1.5	8	1.5	9	1.5	4.8	1.5	5.1	ns
	Propagation Delay Ai to Yi, FCT2541		1.5	8	1.5	9	1.5	4.8	1.5	5.1	
† PZH † PZL	Output Enable Time OE to Yi, FCT541		1.5	10	1.5	10.5	1.5	6.2	1.5	6.5	
	Output Enable Time OE to Yi, FCT2541		1.5	10	1.5	10.5	1.5	6.2	1.5	6.5	
† PHZ † PLZ	Output Disable Time OE to Yi	2	1.5	9.5	1.5	12.5	1.5	5.6	1.5	5.9	

Notes:
 1. Minimum propagation delay values are guaranteed but not tested.
 2. This parameter is guaranteed but not tested.



High Speed CMOS 8-bit Bus Interface Latch Transceivers

QS54/74FCT543T
QS54/74FCT544T

QS54/74FCT2543T
QS54/74FCT2544T

FEATURES/BENEFITS

- Pin and function compatible to the 74F543/4 and 74FCT543T/4T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 543T/4T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A and C speed grades with 5.5ns tPD for C
- I_{OL} = 64 mA Com., 48mA Mil.

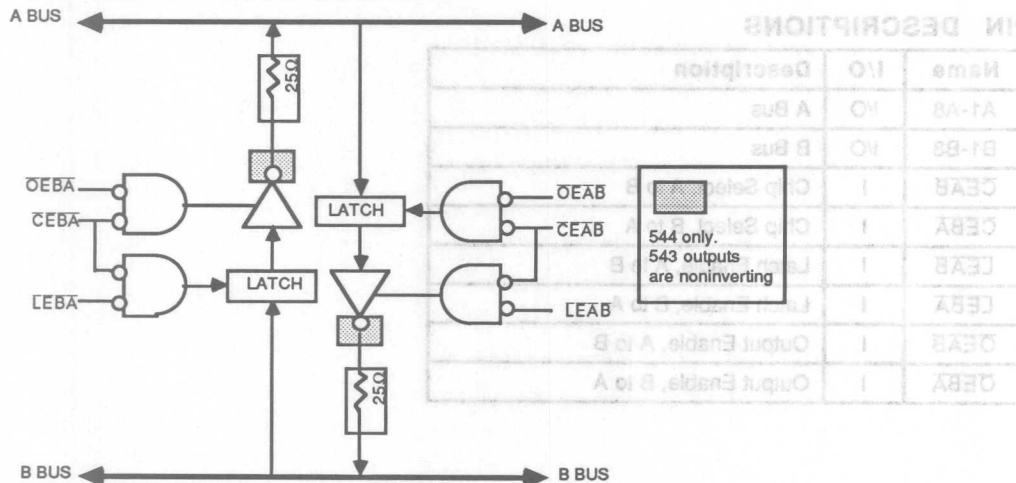
FCT-T 2543T/4T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 6.5ns tPD for A
- I_{OL} = 12mA Com.

DESCRIPTION

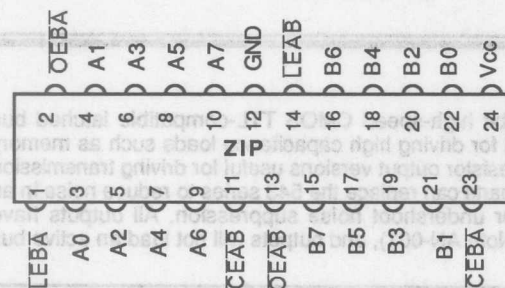
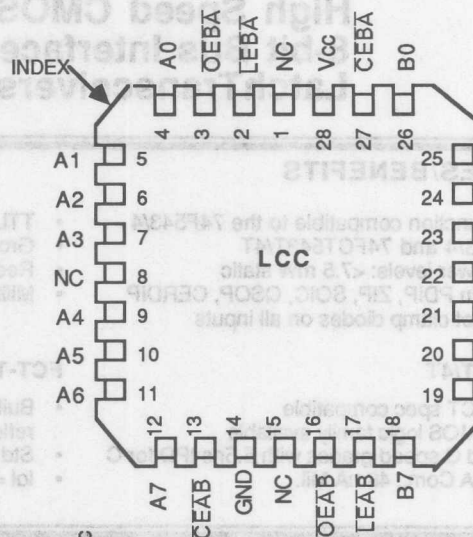
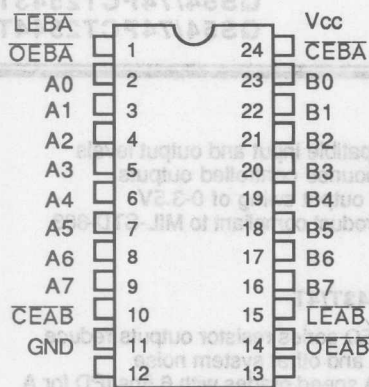
The QSFCT543T/4T and QSFCT543T/4T are 8-bit high-speed CMOS TTL-compatible latched bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2543/4 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2543 series parts can replace the 543 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PINOUTS

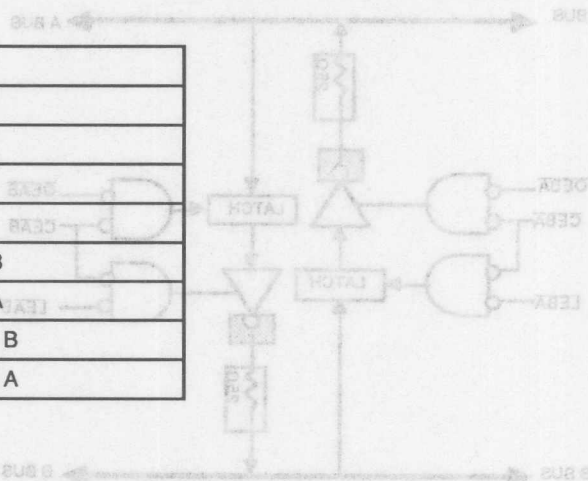
PDIP, SOIC, QSOP



ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
A1-A8	I/O	A Bus
B1-B8	I/O	B Bus
CEAB	I	Chip Select, A to B
CEBA	I	Chip Select, B to A
LEAB	I	Latch Enable, A to B
LEBA	I	Latch Enable, B to A
OEAB	I	Output Enable, A to B
OEBA	I	Output Enable, B to A



QSFCT543T, 544T, 2543T, 2544T

FUNCTION TABLES - QSFCT543/4, 2543/4

Inputs						Outputs		Function	
CEAB	CEBA	LEAB	LEBA	OEAB	OEBA	A1-8	B1-8	543/2543	544/2544
H	H	-	-	-	-	Z	Z	Disabled, Hold	Disabled, Hold
-	-	-	-	H	H	Z	Z	Disabled	Disabled
-	-	H	H	-	-	NC	NC	Hold	Hold
-	-	L	H	-	-	-	-	A->B Latch Open	A->B Latch Open
-	-	H	L	-	-	-	-	B->A Latch Open	B->A Latch Open
-	-	-	-	L	H	-	-	A Latch -> B Bus	A Latch-> B Bus
-	-	-	-	H	L	-	-	B Latch -> A Bus	B Latch-> A Bus

H = HIGH
L = LOW
NC = No Change
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
-----	4	4	5	7	pF
-----	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	μA
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 48 \text{ mA}$ (MIL)	-	-	0.55	
			$I_{ol} = 64 \text{ mA}$ (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}$, freq = 0 $0V \leq V_{in} \leq 0.2V$ or $V_{cc} - 0.2V \leq V_{in} \leq V_{cc}$	-	1.5	mA
ΔI_{cc}	Supply Current per Input @ TTL HIGH	$V_{cc} = \text{MAX}$, $V_{in} = 3.4V$, freq = 0 (2)	-	2.0	
Q_{ccd}	Supply Current per input per mHz	$V_{cc} = \text{MAX}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i = 3.4V$)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

Am	-	-	50	$V_{cc} = \text{MIN}$, $V_o = 0V$	Output Drive (250)
V_{ic}	-	-	-	$V_{cc} = \text{MIN}$, $I_{in} = 10 \text{ mA}$ (2)	Input Clamp Voltage
V_{oh}	-	-	2.4	$I_{oh} = 12 \text{ mA}$ (MIL)	Output HIGH Voltage
	-	-	2.4	$I_{oh} = 18 \text{ mA}$ (COM)	FCT500X & FCT500X
V_{ol}	-	-	0.55	$I_{ol} = 48 \text{ mA}$ (MIL)	Output LOW Voltage
	-	-	0.55	$I_{ol} = 64 \text{ mA}$ (COM)	FCT500X
	-	-	0.55	$I_{ol} = 12 \text{ mA}$ (MIL)	Output LOW Voltage
	-	-	0.50	$I_{ol} = 12 \text{ mA}$ (COM)	FCT500X (250)
R_{out}	-	-	38	$I_{ol} = 12 \text{ mA}$ (MIL)	Output Resistance
	-	-	38	$I_{ol} = 12 \text{ mA}$ (COM)	FCT500X (250)

- Notes:
1. Typical values indicate $V_{cc} = 5.0V$ and $T_A = 25^\circ C$.
 2. Not more than one output should be loaded and the duration is 50 seconds.
 3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Cload = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description		Notes	543/4, 2543/4				543/4A, 2543/4A				543C				
				Com		MII		Com		MII		Com		MII		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t PHLB t PLHB	Bus to Bus Delay Latches Open (Transparent)	543		2.5	8.5	2.5	10	2.5	6.5	2.5	7.5	2.5	5.5			ns
		544		2.5	8.5	2.5	10	2.5	6.5	2.5	7.5					
		2543		2.5	8.5	2.5	10									
		2544		2.5	8.5	2.5	10									
t PHLL t PLHL	Latch Enable to Data Delay LEAB, LEBA to A, B Bus	543		2.5	12.5	2.5	14	2.5	8	2.5	9	2.5	7.0			
		544		2.5	12.5	2.5	14	2.5	8	2.5	9					
		2543		2.5	12.5	2.5	14									
		2544		2.5	12.5	2.5	14									
tPZH tPZL	Output Enable Time OEAB, OEBA CEAB, CEBA to A, B Bus	543		2	12	2	14	2	9	2	10	2.0	8.0			
		544		2	12	2	14	2	9	2	10					
		2543		2	12	2	14									
		2544		2	12	2	14									
tPHZ tPLZ	Output Disable Time	2	2	9	2	13	2	7.5	2	8.5	2	6.5				
t S	Setup Time An to LEAB, Bn to LEBA		3		3		2		2		2					
t H	Hold Time An to LEAB, Bn to LEBA		2		2		2		2		2					
tW	Pulse Width Low LEAB or LEBA		5.0		5.0		5.0		5.0		5.0					

Notes:

- 1) See Test Circuit and Waveforms. Minimums Guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE
 Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V}$ to 5.5V , Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V}$ to 5.5V
 Load = 50 pF , $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Section	QSFCT543T, 544T, 2543T, 2544T											
			QSFCT543T, 544T				2543T, 2544T				QSFCT543T, 544T			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t _{PHL}	Bus to Bus	543	2.5	8.5	2.5	10	2.5	8.5	2.5	10	2.5	8.5	2.5	10
	Delay	544	2.5	8.5	2.5	10	2.5	8.5	2.5	10	2.5	8.5	2.5	10
	Latency	543	2.5	8.5	2.5	10	2.5	8.5	2.5	10	2.5	8.5	2.5	10
	Open (Transition)	544	2.5	8.5	2.5	10	2.5	8.5	2.5	10	2.5	8.5	2.5	10
t _{PLH}	Latency	543	2.5	15.5	2.5	14	2.5	15.5	2.5	14	2.5	15.5	2.5	14
	to Data Delay	544	2.5	15.5	2.5	14	2.5	15.5	2.5	14	2.5	15.5	2.5	14
	LEAD, LEB	543	2.5	15.5	2.5	14	2.5	15.5	2.5	14	2.5	15.5	2.5	14
	to A, B Bus	544	2.5	15.5	2.5	14	2.5	15.5	2.5	14	2.5	15.5	2.5	14
t _{PHZ}	Output	543	2	15	2	14	2	15	2	14	2	15	2	14
	Enable Time	544	2	15	2	14	2	15	2	14	2	15	2	14
	OEAB, OEBA	543	2	15	2	14	2	15	2	14	2	15	2	14
	to A, B Bus	544	2	15	2	14	2	15	2	14	2	15	2	14
t _{PLZ}	Output Disable Time	5	2	9	2	13	2	9	2	13	2	9	2	13
	Setup Time	5	2	9	2	13	2	9	2	13	2	9	2	13
t _H	Hold Time	5	2	9	2	13	2	9	2	13	2	9	2	13
	to LEAB, LEB	5	2	9	2	13	2	9	2	13	2	9	2	13
t _W	Pulse Width Low	5	2.0	8.0	2.0	8.0	2.0	8.0	2.0	8.0	2.0	8.0	2.0	8.0

Notes:
 1) See Test Circuit and Waveforms. Minimums Guaranteed but not tested.
 2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS Bus Interface 8-bit Latches

QS54/74FCT573T

QS54/74FCT2573T

FEATURES/BENEFITS

- Pin and function compatible to the 74F573, 74FCT573 and 74FCT573T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T573T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A, and C speed grades with 4.7 ns tPD for C
- IOL = 48 mA Com., 32 mA Mil.

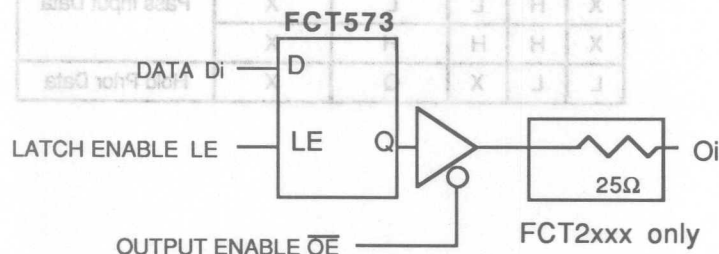
FCT-T 2573T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.2 ns tPD for A
- IOL = 12mA Com.

DESCRIPTION

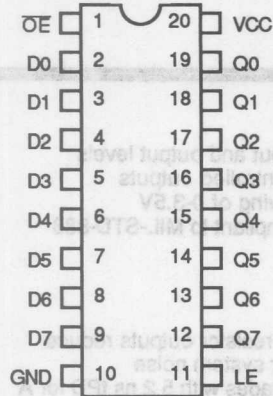
The QSFCT573T and QSFCT2573T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2573 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2573 series parts can replace the 573 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when VCC is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

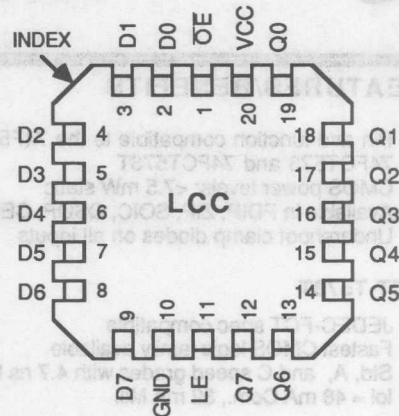
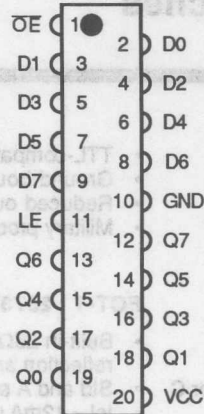


PINOUTS

PDIP, SOIC, QSOP



ZIP



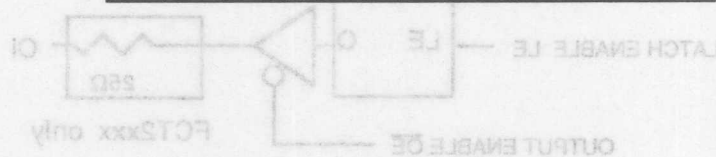
ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
O _i	O	Data Outputs
LE	I	Latch Enable
OE	I	Output Enable

FUNCTION TABLE

Inputs			Internal Q Value	Outputs	Function
OE	LE	Di		O _i	
H	X	X	X	Z	Disable Outputs
L	X	X	L	L	Enable Outputs
L	X	X	H	H	
X	H	L	L	X	Pass Input Data
X	H	H	H	X	
L	L	X	Q	X	Hold Prior Data



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP, LCC	ZIP	Unit
1-9, 11	4	4	5	7	pF
12-19	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Parameter	SOIC	QSOP	PDIP, LCC	ZIP
Input Capacitance C_{in} (pF)	4	4	5	7
Output Capacitance C_{out} (pF)	6	6	7	9
Storage Capacitance C_{stg} (pF)	8	8	9	10

QSFCT573T, 2573T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}$, $\text{freq} = 0$ $0V \leq V_{in} \leq 0.2V$ or $V_{cc} - 0.2V \leq V_{in} \leq V_{cc}$	-	1.5	mA
ΔI_{cc}	Supply Current per Input @ TTL HIGH	$V_{cc} = \text{MAX}$, $V_{in} = 3.4V$, $\text{freq} = 0$ (2)	-	2.0	
Q_{ccd}	Supply Current per input per mHz	$V_{cc} = \text{MAX}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i = 3.4V$)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_{cc} can be computed using the above parameters as explained in the Technical Overview section.

1 PW	1 PHZ	Output Enable Time OE to Y1, S2,3	COM	1.5	11	1.5	8.8	1.5	5.5
			MIL	1.5	15.5	1.5	7.5		
1 PHZ	1 PHZ	Output Disable Time OE to Y1, S2,3	COM	1.5	11	1.5	8.8	1.5	8.5
			MIL	1.5	15.5	1.5	7.5		
1 S	1 PHZ	Data Setup Time DI to LE in low	COM	5	7	1.5	5.5	1.5	5.0
			MIL	5	15	1.5	5.5		
1 H	1 H	Data Hold Time DI to LE in low	COM	5	5	5	5		
			MIL	5	15	1.5	1.5		
1 W	1 W	LE Pulse Width HIGH or LOW	COM	5	5	5	5	4	
			MIL	5	5	5	5		

Notes:
(1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
(2) This parameter is guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Load = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes (1)	573 2573		573A 2573A		573C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay Data to Oi, 573	COM	1.5	8	1.5	5.2	1.5	4.7	ns
t_{PLH}		MIL	2	8.5	1.5	5.6			
	Propagation Delay Data to Oi, 2573	COM	1.5	8	1.5	5.2	1.5	4.7	
		MIL	2	8.5	1.5	5.6			
t_{PHLE}	Propagation Delay LE high to Oi, 573	COM	2	13	2	8.5	2	6.9	
t_{PLHE}		MIL	2	14	2	9.8			
	Propagation Delay LE high to Oi, 2573	COM	2	13	2	8.5	2	6.9	
		MIL	2	14	2	9.8			
t_{PZH}	Output Enable Time $\overline{OE}$ to Yi, 573	COM	1.5	11	1.5	6.5	1.5	5.5	
t_{PZL}		MIL	1.5	12.5	1.5	7.5			
	Output Enable Time $\overline{OE}$ to Yi, 2573	COM	1.5	11	1.5	6.5	1.5	6.5	
		MIL	1.5	12.5	1.5	7.5			
t_{PHZ}	Output Disable Time $\overline{OE}$ to Yi	COM	2	1.5	7	1.5	5.5	1.5	5.0
t_{PLZ}		MIL	2	1.5	8.5	1.5	6.5		
t_S	Data Setup Time Di to LE hi to low	COM	2		2		2		
		MIL	2		2				
t_H	Data Hold Time Di to LE hi to low	COM	1.5		1.5		1.5		
		MIL	1.5		1.5				
t_W	LE Pulse Width HIGH or LOW	COM	2	6	5		4		
		MIL	2	6	6				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.



High Speed CMOS Bus Interface 8-bit Registers

QS54/74FCT574

QS54/74FCT2574

FEATURES/BENEFITS

- Pin and function compatible to the 74FCT574 and 74FCT574T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 574

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, and C speed grades with 5.2ns tPD for C
- I_{OL} = 48 mA Com., 32 mA Mil.

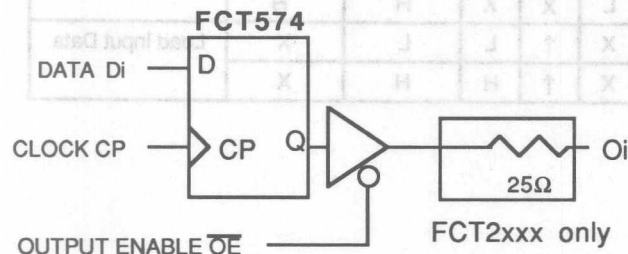
FCT-T 2574

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, & C speed grades with 6.5ns tPD for A
- I_{OL} = 12mA Com.

DESCRIPTION

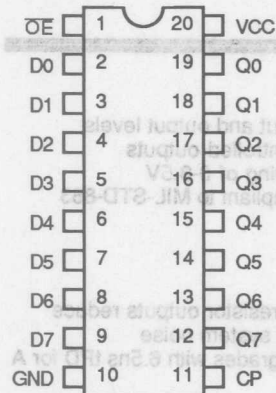
The QSFCT574/A and QSFCT2574/A are 8-bit high-speed CMOS TTL-compatible buffered registers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2574 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2574 series parts can replace the 574 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

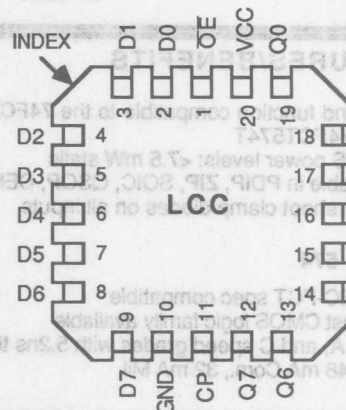
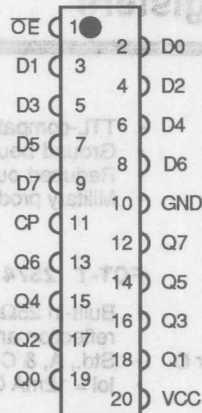


PINOUTS

PDIP, SOIC, QSOP



ZIP



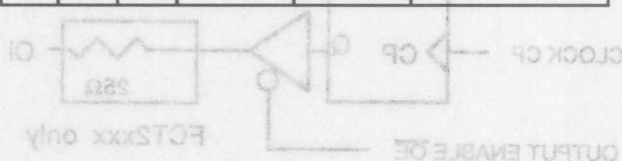
ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CP	I	Clock Input
OE	I	Output Enable

FUNCTION TABLE

Inputs			Internal Q Value	Outputs	Function
OE	CP	Di		Oi	
H	X	X	X	Z	Disable Outputs
L	X	X	L	L	Enable Outputs
L	X	X	H	H	
X	↑	L	L	X	Load Input Data
X	↑	H	H	X	



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-9, 11	4	4	5	7	pF
12-19	6	6	7	9	pF
20-24	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V _{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V _{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	V _{th} - V _{tl} for All Inputs		-	0.2	-	
I _{ih} I _{il}	Input Current Input HIGH or LOW	V _{cc} = MAX	$0 \leq V_{in} < V_{cc}$	-	-	5	μA
I _{oz}	Off State Output Current (Hi-Z)	V _{cc} = MAX, $0 \leq V_{in} \leq V_{cc}$		-	-	5	
I _{os}	Short Circuit Current FCTXXX	V _{cc} = MAX, V _o = GND (2,3)		-60	-	-	mA
I _{or}	Current Drive FCT2XXX	V _{cc} = Min, V _o = 2.0V		50	-	-	mA
V _{ic}	Input Clamp Voltage	V _{cc} = MIN, I _{in} = 18 mA (3)		-	-0.7	-1.2	Volts
V _{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	V _{cc} = MIN	I _{oh} = 12 mA (MIL)	2.4	-	-	Volts
			I _{oh} = 15 mA (COM)	2.4	-	-	
V _{ol}	Output LOW Voltage FCTXXX	V _{cc} = MIN	I _{ol} = 32 mA (MIL)	-	-	0.50	
			I _{ol} = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	V _{cc} = MIN	I _{ol} = 12 mA (MIL)	-	-	0.50	
			I _{ol} = 12 mA (COM)	-	-	0.50	
R _{out}	Output Resistance FCT2XXX (25 Ω)	V _{cc} = MIN	I _{ol} = 12 mA (MIL)	21	28	38	Ω
			I _{ol} = 12 mA (COM)	24	28	35	

- Notes:**
1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
 2. Not more than one output should be shorted and the duration is ≤ 1 second.
 3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_I=3.4V$)
3. For flipflops Qocd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

QSFCT574T, 2574T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

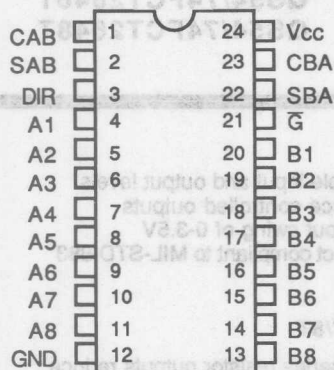
Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Load = 50 pF, $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Notes (1)	574 2574		574A 2574A		574C		Unit
			Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay CP to Oi, 574	COM	2	10	2	6.5	2	5.2	ns
t _{PLH}		MIL	2	11	2	7.2	2	6.2	
	Propagation Delay CP to Oi, 2574	COM	2	10	2	6.5			
		MIL	2	11	2	7.2			
t _{PZH}	Output Enable Time $\overline{\text{OE}}$ to Yi, 574	COM	1.5	12.5	1.5	6.5	1.5	5.5	
t _{PZL}		MIL	1.5	14	1.5	7.5	1.5	6.2	
	Output Enable Time $\overline{\text{OE}}$ to Yi, 2574	COM	1.5	12.5	1.5	6.5			
		MIL	1.5	14	1.5	7.5			
t _{PHZ}	Output Disable Time $\overline{\text{OE}}$ to Yi	COM	2	1.5	8	1.5	5.5	1.5	5
t _{PLZ}		MIL	2	1.5	8	1.5	6.5	1.5	5.7
t _S	Data Setup Time Di to CP	COM	2		2		2		
		MIL	2		2		2		
t _H	Data Hold Time Di to CP	COM	2		1.5		1.5		
		MIL	2		1.5		1.5		
t _W	Clock Pulse Width HIGH or LOW	COM	2	7	5		5		
		MIL	2	7	6		6		

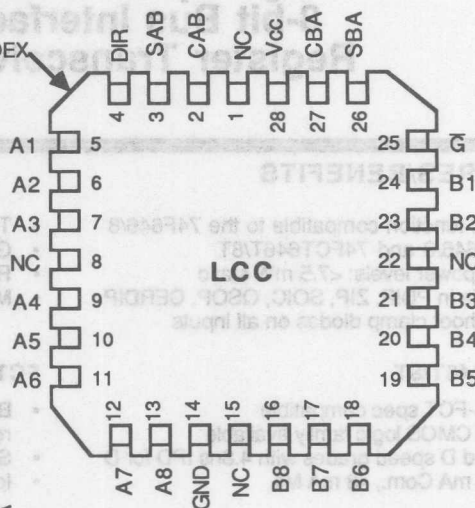
Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

PDIP, SOIC, QSOP



INDEX



QSFCT646T, 648T, 2646T, 2648T

FUNCTION TABLES - QSFCT646/8, 2646/8

Inputs						Outputs		Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1-8	B1-8	646/2646	648/2648
H	-	-	-	-	-	Z	Z	Disabled	Disabled
L	L	-	-	-	-	A	Z	Output A	Output A
L	H	-	-	-	-	Z	B	Output B	Output B
-	-	$\uparrow$	-	-	-	-	-	Load A Reg	Load A Reg
-	-	-	$\uparrow$	-	-	-	-	Load B Reg	Load B Reg
-	-	-	-	L	-	-	-	A Bus $\rightarrow$ B Bus	$\bar{A}$ Bus $\rightarrow$ B Bus
-	-	-	-	H	-	-	-	A Reg $\rightarrow$ B Bus	$\bar{A}$ Reg $\rightarrow$ B Bus
-	-	-	-	-	L	-	-	B Bus $\rightarrow$ A Bus	$\bar{B}$ Bus $\rightarrow$ A Bus
-	-	-	-	-	H	-	-	B Reg $\rightarrow$ A Bus	$\bar{B}$ Reg $\rightarrow$ A Bus

H	= HIGH
L	= LOW,
Z	= High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T _{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
-----	4	4	5	7	pF
-----	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysteresis	Vth - Vtl for All Inputs		-	0.2	-	
Iih Iil	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	μA
Ioz	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-	
Ior	Current Drive FCT2XXX (25Ω)	Vcc = Min, Vo =2.0V		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	21	28	38	Ω
			Iol = 12 mA (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input (V_i = 3.4V)
- For flipflops Q_{ccd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_c can be computed using the above parameters as explained in the Technical Overview section.

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
V _{ic}	Input Clamp Voltage	V _{cc} = MIN, V _i = 0.5V	-	0.7	V
V _{oh}	Output HIGH Voltage	V _{cc} = MIN, I _{oh} = 15 mA (MIL)	2.4	-	V
V _{oh}	Output HIGH Voltage	V _{cc} = MIN, I _{oh} = 15 mA (COM)	2.4	-	V
V _{ol}	Output LOW Voltage	V _{cc} = MIN, I _{ol} = 48 mA (MIL)	-	0.55	V
V _{ol}	Output LOW Voltage	V _{cc} = MIN, I _{ol} = 48 mA (COM)	-	0.55	V
V _{ol}	Output LOW Voltage	V _{cc} = MIN, I _{ol} = 12 mA (MIL)	-	0.50	V
V _{ol}	Output LOW Voltage	V _{cc} = MIN, I _{ol} = 12 mA (COM)	-	0.50	V
R _{out}	Output Resistance	V _{cc} = MIN, I _{ol} = 12 mA (MIL)	24	38	Ω
R _{out}	Output Resistance	V _{cc} = MIN, I _{ol} = 12 mA (COM)	24	38	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T = 25°C.
2. Not more than one output should be shorted and the duration is 25 seconds.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Load = 50 pF, $R_{load} = 500\Omega$ unless otherwise noted

FCT646, FCT2646

Symbol	Description	Notes (1)	646, 2646		646A, 2646A		646C, 2646C		646D, 2646D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHLB} t_{PLHB}	Bus to Bus Delay 646	Com	2	9	2	6.3	1.5	5.4	1.5	4.8	ns
		Mil	2	11	2	7.7	1.5	6.0			
	Bus to Bus Delay 2646	Com	2	9	2	6.3	1.5	5.4			
		Mil	2	11	2	7.7	1.5	6.0			
t_{PZH} t_{PZL}	Output Enable Time 646	Com	2	14	2	9.8	1.5	7.8	1.5	7.3	
		Mil	2	15	2	10.5	1.5	8.9			
	Output Enable Time 2646	Com	2	14	2	9.8	1.5	7.8			
		Mil	2	15	2	10.5	1.5	8.9			
t_{PHZ} t_{PLZ}	Output Disable Time	Com	2	2	2	6.3	1.5	6.3	1.5	6.3	
		Mil	2	2	2	7.7	1.5	7.7			
t_{PHLC} t_{PLHC}	Clock to Bus Delay 646	Com	2	9	2	6.3	1.5	5.7	1.5	5.2	
		Mil	2	10	2	7	1.5	6.3			
	Clock to Bus Delay 2646	Com	2	9	2	6.3	1.5	5.7			
		Mil	2	10	2	7	1.5	6.3			
t_{PHLS} t_{PLHS}	SBA/SAB to Bus Delay 646	Com	2	11	2	7.7	1.5	6.2	1.5	5.8	
		Mil	2	12	2	8.4	1.5	7.0			
	SBA/SAB to Bus Delay 2646	Com	2	11	2	7.7	1.5	6.2			
		Mil	2	12	2	8.4	1.5	7.0			
t_S	Data Setup Time	Com	4		2		2		2		
		Mil	4.5		2		2				
t_H	Data Hold Time	Com	2		1.5		1.5		1.5		
		Mil	2		1.5		1.5				
t_{PWH} t_{PWL}	Clock Pulse Width High or Low	Com	2	6	5		5		5		
		Mil	2	6	5		5				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

QSFCT646T, 648T, 2646T, 2648T

FCT648, FCT2648

Symbol	Description	Notes (1)	648, 2648		648A, 2648A		648C, 2648C		Unit
			Min	Max	Min	Max	Min	Max	
t _{PHLB} t _{PLHB}	Bus to Bus Delay 648	Com	2	8	2	5.6	1.5	5.4	ns
		MII	2	9	2	6.3	1.5	6.0	
	Bus to Bus Delay 2648	Com	2	8	2	5.6	1.5	5.4	
		MII	2	9	2	6.3	1.5	6.0	
t _{PZH} t _{PZL}	Output Enable Time 648	Com	2	15	2	10.5	1.5	7.8	
		MII	2	18	2	12.6	1.5	8.9	
	Output Enable Time 2648	Com	2	15	2	10.5	1.5	7.8	
		MII	2	18	2	12.6	1.5	8.9	
t _{PHZ} t _{PLZ}	Output Disable Time	Com	2	9	2	6.3	1.5	6.3	
		MII	2	11	2	7.7	1.5	7.7	
t _{PHLC} t _{PLHC}	Clock to Bus Delay 648	Com	2	9	2	6.3	1.5	5.7	
		MII	2	10	2	7	1.5	6.3	
	Clock to Bus Delay 2648	Com	2	9	2	6.3	1.5	5.7	
		MII	2	10	2	7	1.5	6.3	
t _{PHLS} t _{PLHS}	SBA/SAB to Bus Delay 648	Com	2	11	2	7.7	1.5	6.2	
		MII	2	12	2	8.4	1.5	7.0	
	SBA/SAB to Bus Delay 2648	Com	2	11	2	7.7	1.5	6.2	
		MII	2	12	2	8.4	1.5	7.0	
t _S	Data Setup Time	Com	4		2		2		
		MII	4.5		2		2		
t _H	Data Hold Time	Com	2		1.5		1.5		
		MII	2		1.5		1.5		
t _{PWH} t _{PWL}	Clock Pulse Width High or Low	Com	2	6	5		5		
		MII	2	6	5		5		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS 8-bit Bus Interface Register Transceivers

QS54/74FCT651T

QS54/74FCT652T

QS54/74FCT2651T

QS54/74FCT2652T

FEATURES/BENEFITS

- Pin and function compatible to the 74F651/2
- 74FCT651/2 and 74FCT651T/2T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T651T/2T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A and C speed grades with 5.4 ns tPD for C
- Iol = 64 mA Com., 48 mA Mil.

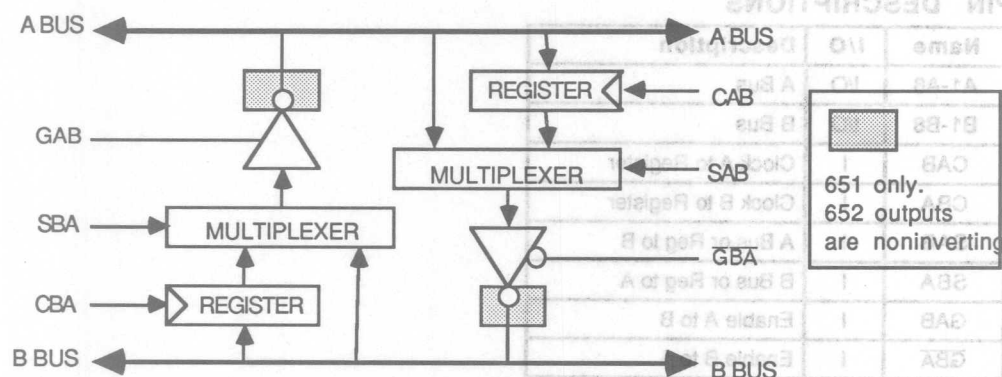
FCT-T 2651T/2T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 6.3 ns tPD for A
- Iol = 12mA Com.

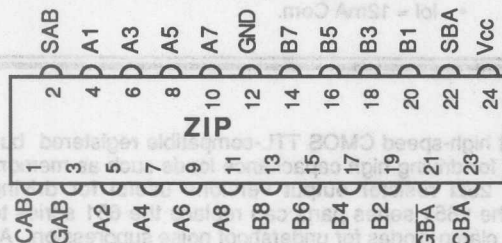
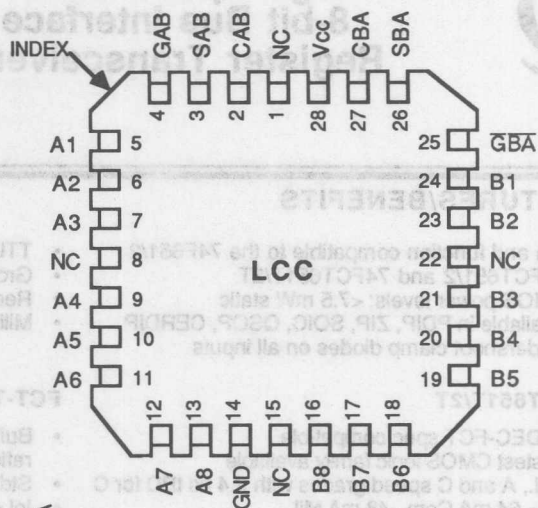
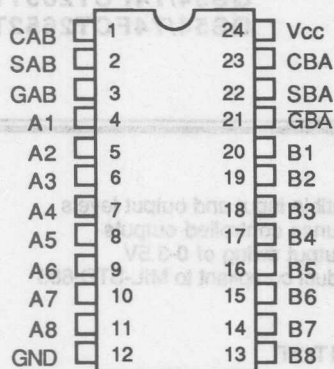
DESCRIPTION

The QSFCT651T/2T and QSFCT651T/2T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2651/2 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2651 series parts can replace the 651 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PDIP, SOIC, QSOP



ALL PINS TOP VIEW

PIN DESCRIPTIONS

Name	I/O	Description
A1-A8	I/O	A Bus
B1-B8	I/O	B Bus
CAB	I	Clock A to Register
CBA	I	Clock B to Register
SAB	I	A Bus or Reg to B
SBA	I	B Bus or Reg to A
GAB	I	Enable A to B
GBA	I	Enable B to A

QSFCT651T, 652T, 2651T, 2652T

FUNCTION TABLES - QSFCT651/2, 2651/2

Inputs						Outputs		Function	
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A1-8	B1-8	651/2651	652/2652
L	H	-	-	-	-	Z	Z	Disabled	Disabled
L	L	-	-	-	-	A	Z	Output A	Output A
H	H	-	-	-	-	Z	B	Output B	Output B
H	L	-	-	-	-	A	B	Output A & B	Output A & B
-	-	↑	-	-	-	-	-	Load A Reg	Load A Reg
-	-	-	↑	-	-	-	-	Load B Reg	Load B Reg
-	-	-	-	L	-	-	-	$\overline{\text{A}}$ Bus -> B Bus	A Bus -> B Bus
-	-	-	-	H	-	-	-	$\overline{\text{A}}$ Reg -> B Bus	A Reg -> B Bus
-	-	-	-	-	L	-	-	$\overline{\text{B}}$ Bus -> A Bus	B Bus -> A Bus
-	-	-	-	-	H	-	-	$\overline{\text{B}}$ Reg -> A Bus	B Reg -> A Bus

↑ = LOW-to-HIGH transition
 H = HIGH
 L = LOW,
 Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V				
DC Output Voltage V_O	-0.5V to 7.0V				
DC Input Voltage V_I	-0.5V to 7.0V				
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V				
DC Input Diode Current with $V_I < 0$	-20 mA				
DC Output Diode Current with $V_O < 0$	-50 mA				
DC Output Current Max. sink current/pin.....	120 mA				
N=Number of Outputs, M=Number of inputs					
Maximum Power Dissipation.....	0.5 watts				
T_{STG} Storage Temperature.....	-65° to +165°C				

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
	4	4	5	7	pF
	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T _A =0°C to 70°C, V _{CC} =5.0V±5%				Military T _A =-55°C to 125°C, V _{CC} =5.0V±10%			
Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V _{IH}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V _{IL}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV _I	Input Hysteresis	V _{IH} - V _{IL} for All Inputs		-	0.2	-	
I _{IH} I _{IL}	Input Current Input HIGH or LOW	V _{CC} = MAX	0 ≤ V _{IN} < V _{CC}	-	-	5	μA
I _{OZ}	Off State Output Current (Hi-Z)	V _{CC} = MAX, 0 ≤ V _{IN} ≤ V _{CC}		-	-	5	
I _{OS}	Short Circuit Current FCTXXX	V _{CC} = MAX, V _O = GND (2,3)		-60	-	-	mA
I _{OR}	Current Drive FCT2XXX (25Ω)	V _{CC} = Min, V _O = 2.0V		50	-	-	mA
V _{IC}	Input Clamp Voltage	V _{CC} = MIN, I _{in} = 18 mA (3)		-	-0.7	-1.2	Volts
V _{OH}	Output HIGH Voltage FCTXXX & FCT2XXX	V _{CC} = MIN	I _{OH} = 12 mA (MIL)	2.4	-	-	Volts
			I _{OH} = 15 mA (COM)	2.4	-	-	
V _{OL}	Output LOW Voltage FCTXXX	V _{CC} = MIN	I _{OL} = 48 mA (MIL)	-	-	0.55	
			I _{OL} = 64 mA (COM)	-	-	0.55	
	Output LOW Voltage FCT2XXX (25Ω)	V _{CC} = MIN	I _{OL} = 12 mA (MIL)	-	-	0.50	
			I _{OL} = 12 mA (COM)	-	-	0.50	
R _{OUT}	Output Resistance FCT2XXX (25Ω)	V _{CC} = MIN	I _{OL} = 12 mA (MIL)	21	28	38	Ω
			I _{OL} = 12 mA (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input (V_I = 3.4V)
- For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_{cc} can be computed using the above parameters as explained in the Technical Overview section.

mA	-	-	30	V _{cc} = MIN, V _o = 5.0V	Current Drive FCT300X (SS2)	I _{OL}
V _{IC}	-	-0.7	-	V _{cc} = MIN, I _{in} = 18 mA (3)	Input Clamp Voltage	V _{IC}
V _{OH}	-	-	5.4	I _{OH} = 12 mA (MIL) V _{cc} = MIN	Output HIGH Voltage FCT300X & FCT300X	V _{OH}
	-	-	5.4	I _{OH} = 12 mA (COM)		
V _{OL}	0.55	-	-	I _{OL} = 48 mA (MIL) V _{cc} = MIN	Output LOW Voltage FCT300X	V _{OL}
	0.55	-	-	I _{OL} = 64 mA (COM)		
	0.55	-	-	I _{OL} = 12 mA (MIL) V _{cc} = MIN	Output LOW Voltage FCT300X (SS2)	V _{OL}
	0.55	-	-	I _{OL} = 12 mA (COM)		
R _{OUT}	38	38	21	I _{OL} = 12 mA (MIL) V _{cc} = MIN	Output Resistance FCT300X (SS2)	R _{OUT}
Ω	38	38	24	I _{OL} = 12 mA (COM)		

- Notes:
- Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
 - Not more than one output should be shorted and the duration is 21 seconds.
 - These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Load = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes (1)	651/2 2651/2		651/2 A, 2651/2 A		651/2 C, 2651/2 C		Unit
			Min	Max	Min	Max	Min	Max	
tPHLB tPLHB	Bus to Bus Delay 651	Com	2	9	2	6.3	1.5	5.4	ns
		MII	2	10	2	6.7	1.5	6.0	
	Bus to Bus Delay 2651	Com	2	9	2	6.3			
		MII	2	10	2	7.7			
tPZH tPZL	Output Enable Time 651	Com	2	10	2	9.8	1.5	7.8	
		MII	2	12	2	10.5	1.5	8.9	
	Output Enable Time 2651	Com	2	10	2	9.8			
		MII	2	12	2	10.5			
tPHZ tPLZ	Output Disable Time	Com	2	2	9	2	6.3	1.5	6.3
		MII	2	2	12	2	7.7	1.5	7.7
tPHLC tPLHC	Clock to Bus Delay 651	Com	2	9	2	6.3	1.5	5.7	
		MII	2	10	2	7	1.5	6.3	
	Clock to Bus Delay 2651	Com	2	9	2	6.3			
		MII	2	11	2	7			
tPHLS tPLHS	SBA/SAB to Bus Delay 651	Com	2	11	2	7.7	1.5	6.2	
		MII	2	12	2	8.4	1.5	7.0	
	SBA/SAB to Bus Delay 2651	Com	2	11	2	7.7			
		MII	2	12	2	8.4			
tS	Data Setup Time	Com	4		2		2		
		MII	4.5		2		2		
tH	Data Hold Time	Com	2		1.5		1.5		
		MII	2		1.5		1.5		
tPWH tPWL	Clock Pulse Width High or Low	Com	2	6	5		5		
		MII	2	6	5		5		

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA=0°C to 70°C, VCC=5.0V±5% Military TA=-55°C to 125°C, VCC=5.0V±10%
 Load = 50 pF, Rise = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	651/2		652/2		2651/2 A		2652/2 C		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPLH	Bus to Bus Delay 651	Com	2	0	2	0	2	0.3	1.5	0.4	ns
		Mil	2	10	2	10	2	0.7	1.5	0.0	
	Bus to Bus Delay 2651	Com	2	0	2	0.3					
		Mil	2	10	2	7.7					
tPZH tPZL	Output Enable Time 651	Com	2	10	2	0.3	1.5	7.8			
		Mil	2	12	2	10.5	1.5	8.0			
	Output Enable Time 2651	Com	2	10	2	0.3					
		Mil	2	12	2	10.5					
tPHZ tPLZ	Output Disable Time	Com	2	0	2	0.3	1.5	8.3			
		Mil	2	12	2	7.7	1.5	7.7			
	Clock to Bus Delay 651	Com	2	0	2	0.3	1.5	8.7			
		Mil	2	10	2	7	1.5	8.3			
tPLS tPLS	Clock to Bus Delay 2651	Com	2	0	2	0.3					
		Mil	2	11	2	7					
	SBASB to Bus Delay 651	Com	2	11	2	7.7	1.5	8.2			
		Mil	2	12	2	8.4	1.5	7.0			
tS	SBASB to Bus Delay 2651	Com	2	11	2	7.7					
		Mil	2	12	2	8.4					
	Data Setup Time	Com	4		2		2				
		Mil	4.5		2		2				
tH	Data Hold Time	Com	2		1.5		1.5				
		Mil	2		1.5		1.5				
	Clock Pulse Width High or Low	Com	2	0	2	0	0				
		Mil	2	0	0	0	0				

Notes:
 (1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
 (2) This parameter is guaranteed by design but not tested.

Q

High Speed CMOS Bus Interface 8, 9 & 10-bit Registers

QS54/74FCT821T
QS54/74FCT823T
QS54/74FCT825T

QS54/74FCT2821T
QS54/74FCT2823T
QS54/74FCT2825T

FEATURES/BENEFITS

- Pin and function compatible to the 74F821/3/5 and 74FCT821T/3T/5T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT 821T/3T/5T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- I_{OL} = 48 mA Com., 32 mA Mil.

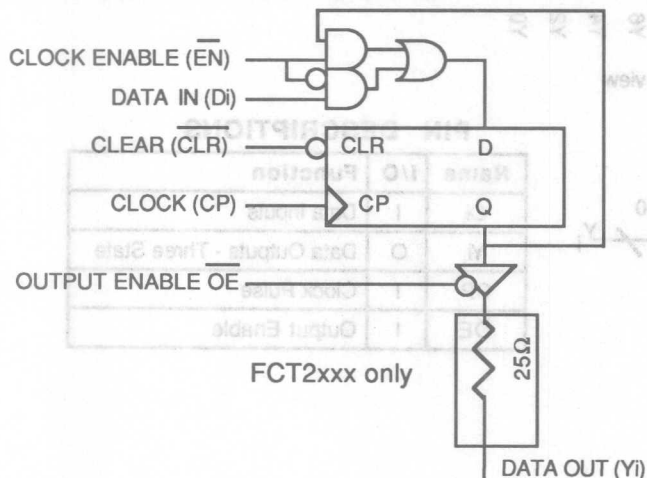
FCT 2821T/3T/5T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- I_{OL} = 12 mA Com.

DESCRIPTION

The QSFC821T/823T/825T and QSFC2821T/823T/825T are 10, 9, and 8-bit high-speed CMOS TTL-compatible buffered registers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2821/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2821 series parts can replace the 821 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

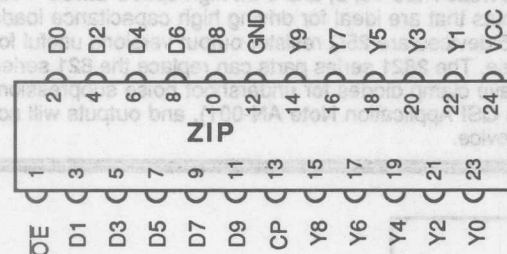
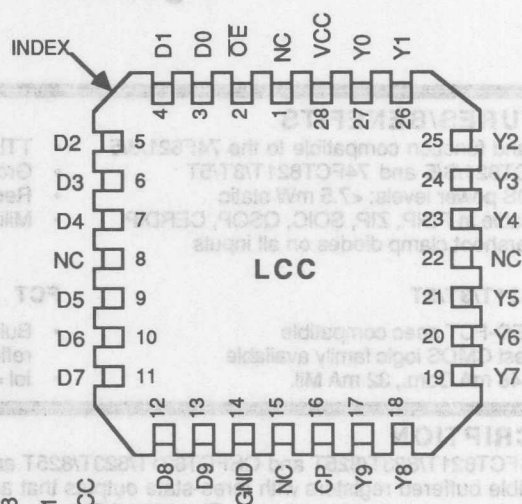
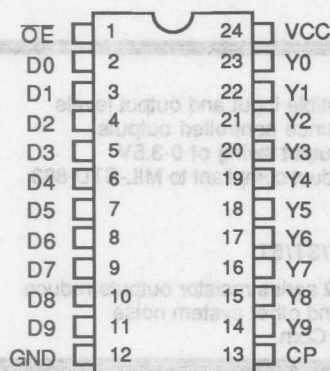


PINOUTS

FCT821 PIN CONFIGURATIONS

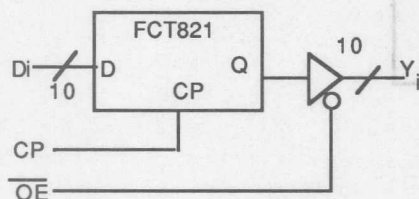
FCT821 - 10-BIT REGISTER

PDIP, SOIC, QSOP



All packages are shown with the Top view

FCT821 LOGIC SYMBOL

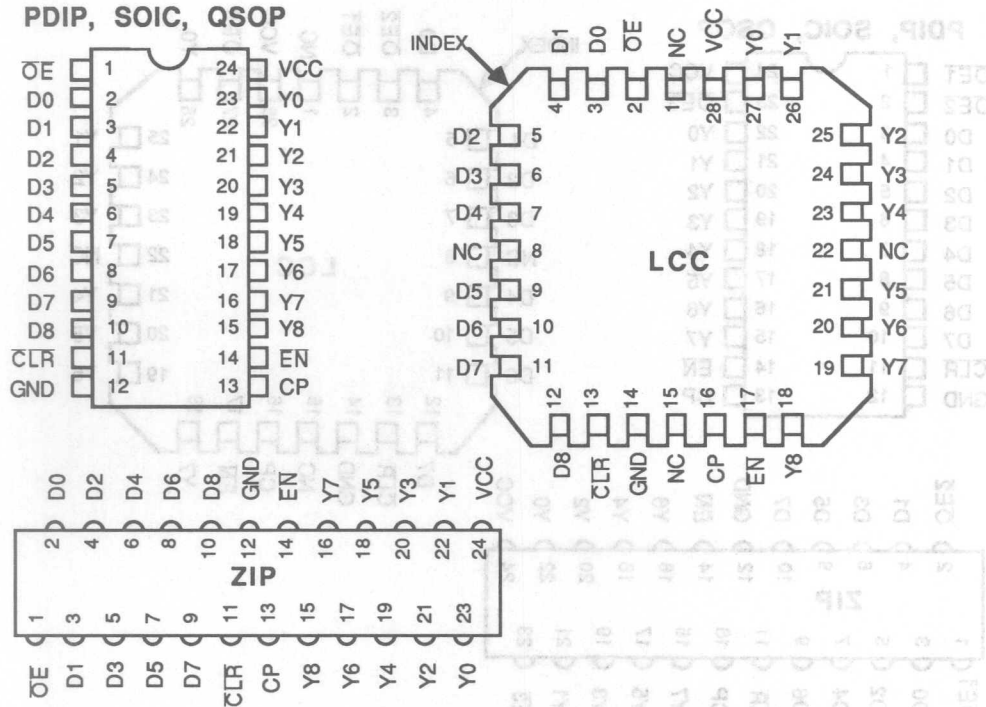


PIN DESCRIPTIONS

Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
CP	I	Clock Pulse
OE	I	Output Enable

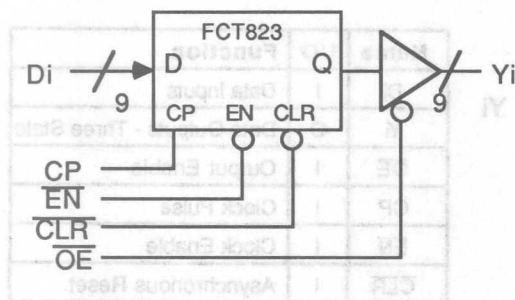
FCT823 - 9-BIT REGISTER

PDIP, SOIC, QSOP



All packages are shown with the Top view

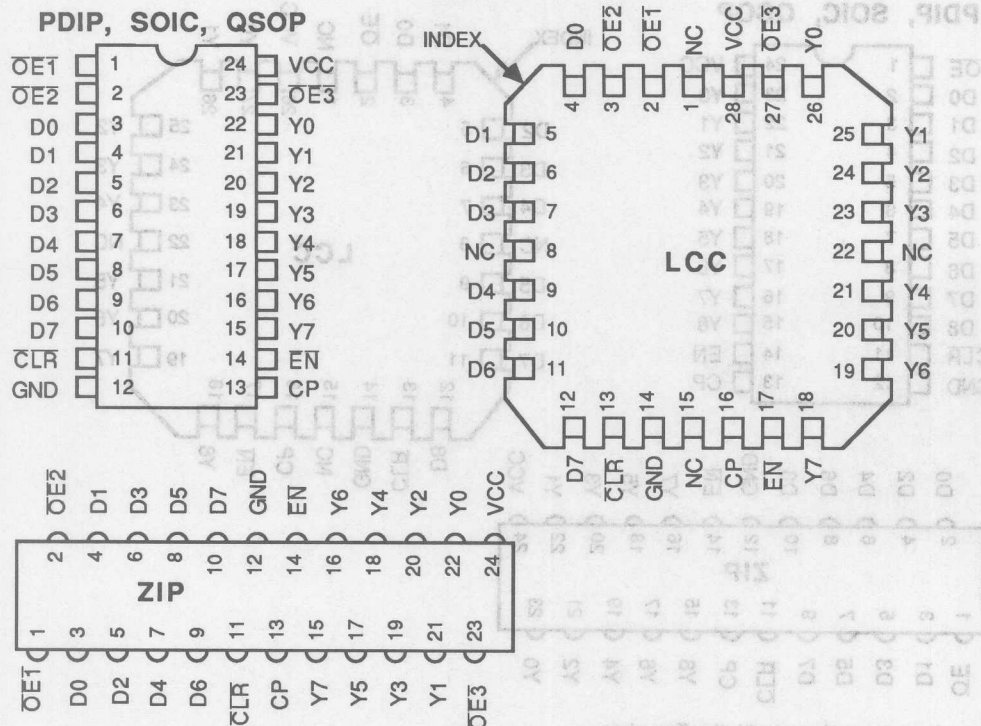
FCT823 LOGIC SYMBOL



PIN DESCRIPTIONS

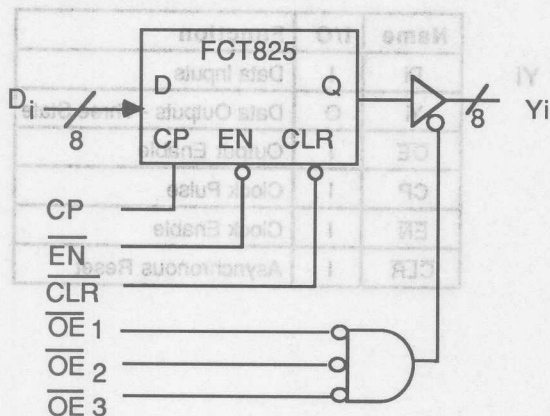
Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
OE	I	Output Enable
CP	I	Clock Pulse
EN	I	Clock Enable
CLR	I	Asynchronous Reset

FCT825 - 8-BIT REGISTER



All packages are shown with the Top View

FCT825 LOGIC SYMBOL



PIN DESCRIPTIONS

Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
$\overline{OE}$	I	Output Enable
CP	I	Clock Pulse
EN	I	Clock Enable
$\overline{CLR}$	I	Asynchronous Reset

FUNCTION TABLES - QSFCT821/823/825

Inputs					Int.	O/P	Function
OE	CLR	EN	DI	CP	QI	YI	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	
H	H	L	H	↑	H	Z	Load
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

↑ = LOW-to-HIGH transition

NC = No Change from the previous state,

H = HIGH

L = LOW,

Z = High Impedance

Int. = Internal

For the 821, the Hi-Z and Load functions only apply as the EN and CLR are not present in these devices. For the 825, there are 3 output enables, and the composite output enable is asserted only when all the three are LOW. If any one of the three output enables are HIGH, the output is disabled.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3-11,13	4	4	5	7	pF
15-22	6	6	7	9	pF
2,14,23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

For the 821, the Hi-Z and Load functions only apply as the EN and CE are not present in these devices.
For the 822, there are 3 output enables, and the composite output enable is asserted only when all three are LOW. If any one of the three output enables are HIGH, the output is disabled.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ i_{ih} $ $ i_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	mA
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 15 \text{ mA}$ (MIL)	2.4	-	Volts
			$I_{oh} = 24 \text{ mA}$ (COM)	2.4	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qocd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Load = 50 pF, $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Notes	821A 823A (1) 825A 2821A 2823A 2825A		821B 823B 825B 2821B 2823B 2825B		821C 823C 825C		821D 823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}	Clock to Y Delay	Com		10.0		7.5		6.0		5.3	ns
t_{PLH}	OE=low, FCT821/3/5	Mil		11.5		8.5		7.0			
		Com	2,3	20.0		15.0		12.5		12.5	
		Mil	2,3	20.0		16.0		13.5			
	Clock to Y Delay	Com		10.0		7.5					
	OE=low, FCT2821/3/5	Mil		11.5		8.5					
		Com	2,3	20.0		15.0					
		Mil	2,3	20.0		16.0					
t_S	Data to Cp Setup Time	Com	4.0		3.0		3.0		3.0		
		Mil	4.0		3.0		3.0				
t_H	Data to Cp Hold Time	Com	2.0		1.5		1.5		1.5		
		Mil	2.0		1.5		1.5				
t_{ENS}	$\overline{EN}$ to Cp Setup Time	Com	4.0		3.0		3.0		3.0		
		Mil	4.0		3.0		3.0				
t_{ENH}	$\overline{EN}$ to Cp Hold Time	Com	2.0		0.0		0.0		0.0		
		Mil	2.0		0.0		0.0				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Load = 300 pF
- 4) Load = 5 pF

QSFCT821/3/5T, 2821/3/5T

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 $C_{load} = 50\text{ pF}$, $R_{load} = 500\Omega$ unless otherwise noted

Symbol	Description	Notes	821A 823A 825A 2821A 2823A 2825A		821B 823B 825B 2821B 2823B 2825B		821C 823C 825C		821D 823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t CLR	CLR to Y Delay 823/5	Com		11.0		9.0		8.0		7.0	ns
		Mil		12.0		9.5		8.5			
	CLR to Y Delay 2823/5	Com		11.0		9					
		Mil		12.0		9.5					
t REC	CLR to Cp Setup Time	Com	6.0	6.0	6.0	6.0	6.0	6.0			
		Mil	7.0	6.0	6.0	6.0	6.0	6.0			
t PWH t PWL	Clock Pulse Width High or Low	Com 2	7.0	6.0	6.0	6.0	6.0	6.0			
		Mil 2	7.0	6.0	6.0	6.0	6.0	6.0			
tPZH tPZL	Output Enable Time OE to Yi, FCT821-5	Com		12.0		8.0		7.0		6.5	
		Mil		13.0		9.0		8.0			
		Com 2,3		23		15		12.5		12.5	
		Mil 2,3		25		16		13.5			
	Output Enable Time OE to Yi, FCT2821-5	Com		12		8.0					
		Mil		13		9.0					
		Com 2,3		23							
		Mil 2,3		25							
tPHZ tPLZ	Output Disable Time OE to Yi	Com 2,4		7		6.5		6.2		6.2	
		Mil 2,4		8		7		6.2			
		Com 2		9		7.5		6.5		6.5	
		Mil 2		10		8		6.5			

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) $C_{load} = 300\text{ pF}$
- 4) $C_{load} = 5\text{ pF}$

Q

High Speed CMOS Bus Interface 10-bit Buffers

QS54/74FCT827T
QS54/74FCT828T

QS54/74FCT2827T
QS54/74FCT2828T

FEATURES/BENEFITS

- Pin and function compatible to the 74F827/8 and 74FCT827T/8T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 827T/8T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A, and C speed grades with 4.4ns tPD for C
- IOL = 48mA Com., 32 mA Mil.

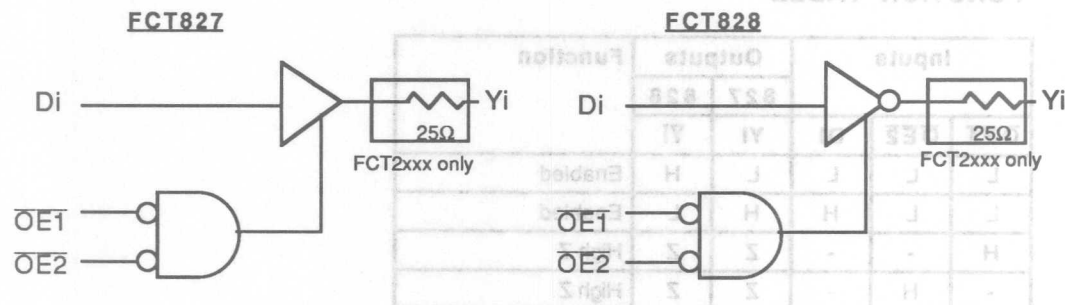
FCT-T 2827T/8T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.0ns tPD for A
- IOL = 12mA Com.

DESCRIPTION

The QSFCT827T/828T and QSFCT2827T/2828T are 10-bit buffers/line drivers with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. The 2827/8 are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2827 series parts can replace the 827 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when VCC is removed from the device.

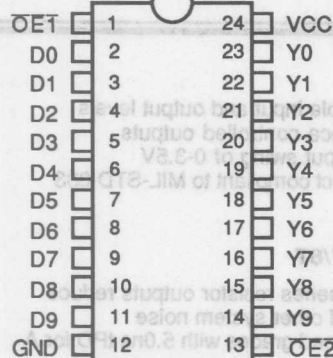
FUNCTIONAL BLOCK DIAGRAM



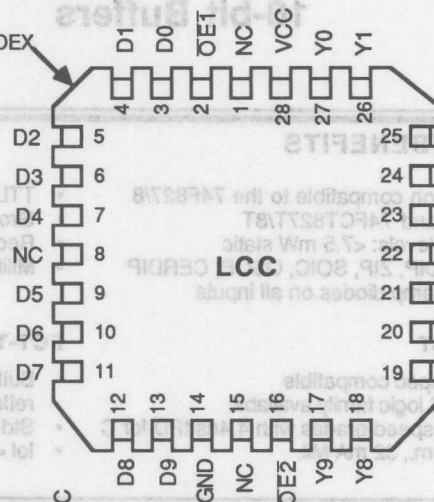
QSFCT827T, 828T, 2827T, 2828T

PINOUTS

PDIP, SOIC, QSOP



INDEX



ALL PINS TOP VIEW

FUNCTION TABLE

Inputs			Outputs		Function
OE1	OE2	DI	YI	YI	
L	L	L	L	H	Enabled
L	L	H	H	L	Enabled
H	-	-	Z	Z	High Z
-	H	-	Z	Z	High Z

H=High, L=Low, Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
-----	4	4	5	7	pF
-----	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

V _{in}	V _{out}	Output HIGH Voltage FCTXXX & FCTXXX		Output LOW Voltage FCTXXX		Output LOW Voltage FCTXXX (SSD)		Output Resistance FCTXXX (SSD)	
		Min	Max	Min	Max	Min	Max	Min	Max
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50

QSFCT827T, 828T, 2827T, 2828T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{tLH} - V_{tHL}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 15 \text{ mA (MIL)}$	2.4	-	-	Volts
			$I_{oh} = 24 \text{ mA (COM)}$	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 48 \text{ mA (COM)}$	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 12 \text{ mA (COM)}$	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	21	28	38	Ω
			$I_{ol} = 12 \text{ mA (COM)}$	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{CC} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{CC} - 0.2V ≤ V _{in} ≤ V _{CC}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{CC} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{CC} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{CC} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_i=3.4V$)
3. For flipflops Qocd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Load = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes (1)	827/8A, 2827/8A		827/8B, 2827/8B		827/8C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Ai to Yi, FCT827	Com	-	8	-	5	-	4.4	ns
		MII	-	9	-	6.5	-	5.0	
		Com	2,3	15	-	13	-	10	
		MII	2,3	17	-	14	-	11	
	Propagation Delay Ai to Yi, FCT2827	Com	-	8	-	5	-	-	
		MII	-	9	-	6.5	-	-	
		Com	2,3	17	-	-	-	-	
		MII	2,3	18	-	-	-	-	
	Propagation Delay Ai to Yi, FCT828	Com	-	7.5	-	5	-	4.4	
		MII	-	9.5	-	6.5	-	5.0	
		Com	2,3	14	-	13	-	10	
		MII	2,3	16	-	14	-	11	
	Propagation Delay Ai to Yi, FCT2828	Com	-	7.5	-	5	-	-	
		MII	-	9.5	-	6.5	-	-	
		Com	2,3	17	-	-	-	-	
		MII	2,3	18	-	-	-	-	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi, FCT827/8	Com	-	12	-	8	-	7	
		MII	-	13	-	9	-	8	
		Com	2,3	23	-	15	-	14	
		MII	2,3	25	-	16	-	15	
	Output Enable Time $\overline{OE}$ to Yi, FCT2827/8	Com	-	12	-	8	-	-	
		MII	-	13	-	9	-	-	
		Com	2,3	23	-	-	-	-	
		MII	2,3	25	-	-	-	-	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	Com	2	9	-	6	-	5.7	
		MII	2	10	-	7	-	6.7	
		Com	2	10	-	7	-	6	
		MII	2	10	-	8	-	7	

- Notes: 1. Minimum propagation delay values guaranteed but not tested.
2. This parameter is guaranteed but not tested.
3. Load = 300 pF



High Speed CMOS Transceivers With Parity

QS29FCT833T

QS29FCT853T

QS29FCT2833T

QS29FCT2853T

ADVANCE INFORMATION

FEATURES/BENEFITS

- Pin and function compatible to the Am29833/53
- Parity generation and detection
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT 833T/53T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- I_{OL} = 48 mA Com., 32 mA Mil.

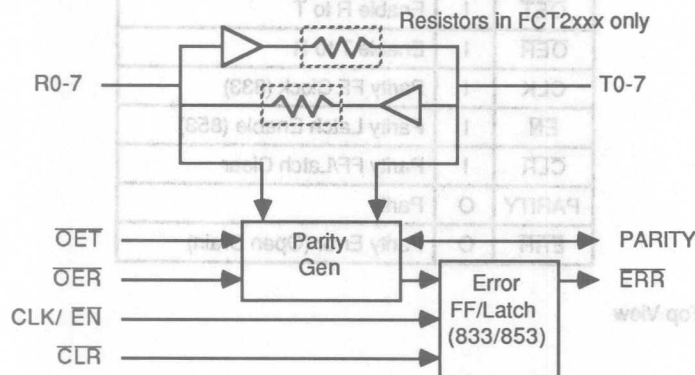
FCT 2833T/53T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- I_{OL} = 12 mA Com.

DESCRIPTION

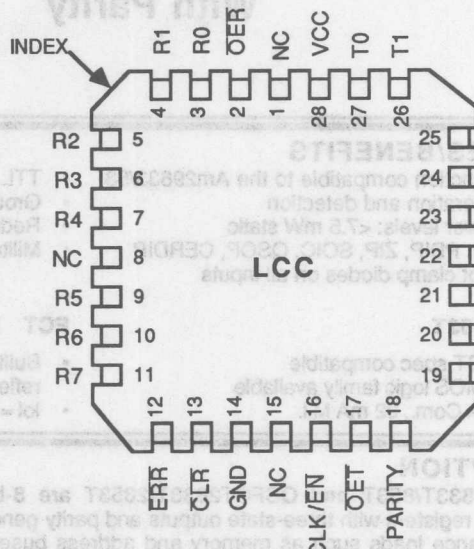
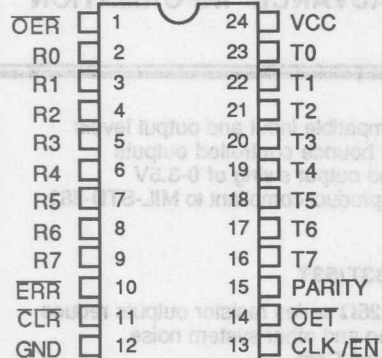
The QSFCT833T/853T and QSFCT2833T/2853T are 8-bit high-speed CMOS TTL compatible transceivers registers with three-state outputs and parity generate/detect logic that are ideal for driving high capacitance loads such as memory and address buses. These parts generate and check odd parity. All lows (zeros) in generates a one for parity. The 833 has a FF and the 853 has a latch to record a parity error defined as a difference between parity generated from the inputs and the parity bit supplied with the inputs. Once the FF/latch is set, it remains set until cleared by a pulse on CLR. ERR is the output from this FF/latch and is open drain allowing multiple devices to be ORed. The 2833/53 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2833 series parts can replace the 833 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

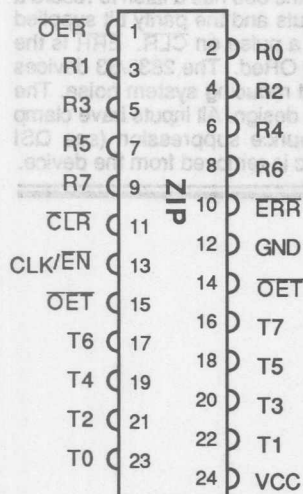


FCT833/853 PIN CONFIGURATIONS

PDIP, SOIC, QSOP



Note: Pin 13 (pin 16 of LCC) is CLK on 833 and EN on 853.



PIN DESCRIPTIONS

Name	I/O	Function
Ri	I/O	Data Bus, R side
Ti	I/O	Data Bus, T side
OET	I	Enable R to T
OER	I	Enable T to R
CLK	I	Parity FF Clock (833)
EN	I	Parity Latch Enable (853)
CLR	I	Parity FF/Latch Clear
PARITY	O	Parity
ERR	O	Parity Error (Open Drain)

All packages are shown with the Top View

Q

High Speed CMOS Bus Interface 8, 9 & 10-bit Latches

QS54/74FCT841T
QS54/74FCT843T
QS54/74FCT845T

QS54/74FCT2841T
QS54/74FCT2843T
QS54/74FCT2845T

FEATURES/BENEFITS

- Pin and function compatible to the Am29841/3/5 74FCT 841/3/5 and 74FCT841T/3T/5T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, Cerdip
- Undershoot Clamp diodes on all inputs

- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 841T, 843T, 845T

- JEDEC-FCT spec compatible
- Fastest CMOS Logic family Available
- A, B and C speed grades with 5.5ns tPD for C
- IOL = 48 mA Com, 32 mA Mil

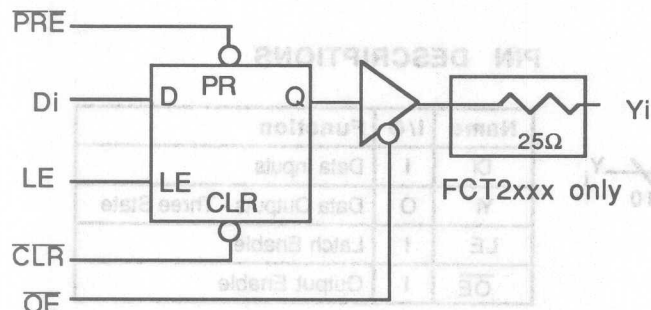
FCT-T 2841T, 2843T, 2845T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B and C speed grades with 5.5ns tPD for C
- IOL = 12mA Com

DESCRIPTION

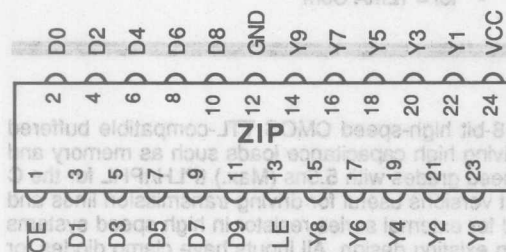
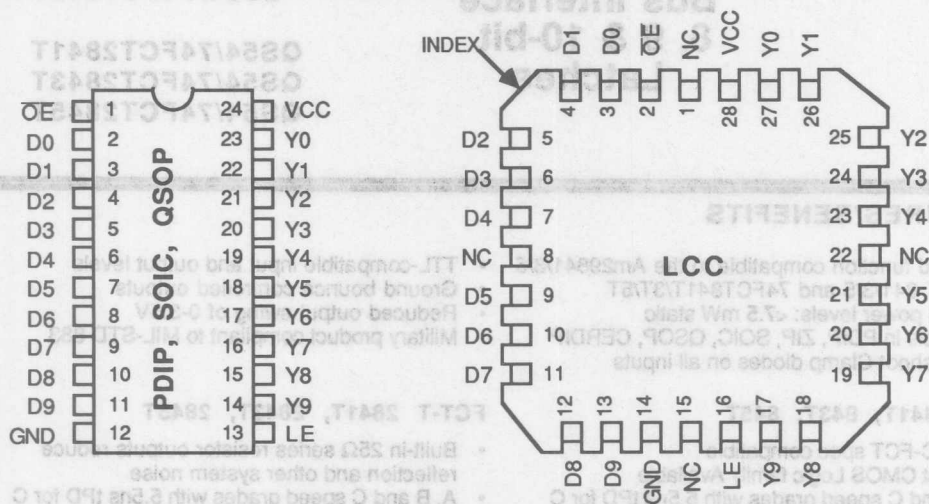
The QS54/74FCT841T, 843T, and 845T are 10, 9, and 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The devices come in A, B, and C speed grades with 5.5ns (Max.) tPLH/tPHL for the C grade. The 2841/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 284x eliminate the need for external series resistor in high speed systems and can replace the 84x series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression, and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



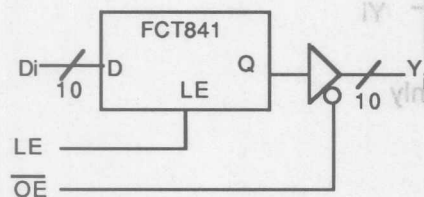
PINOUTS

FCT841 PIN CONFIGURATIONS



• ALL PINS TOP VIEW

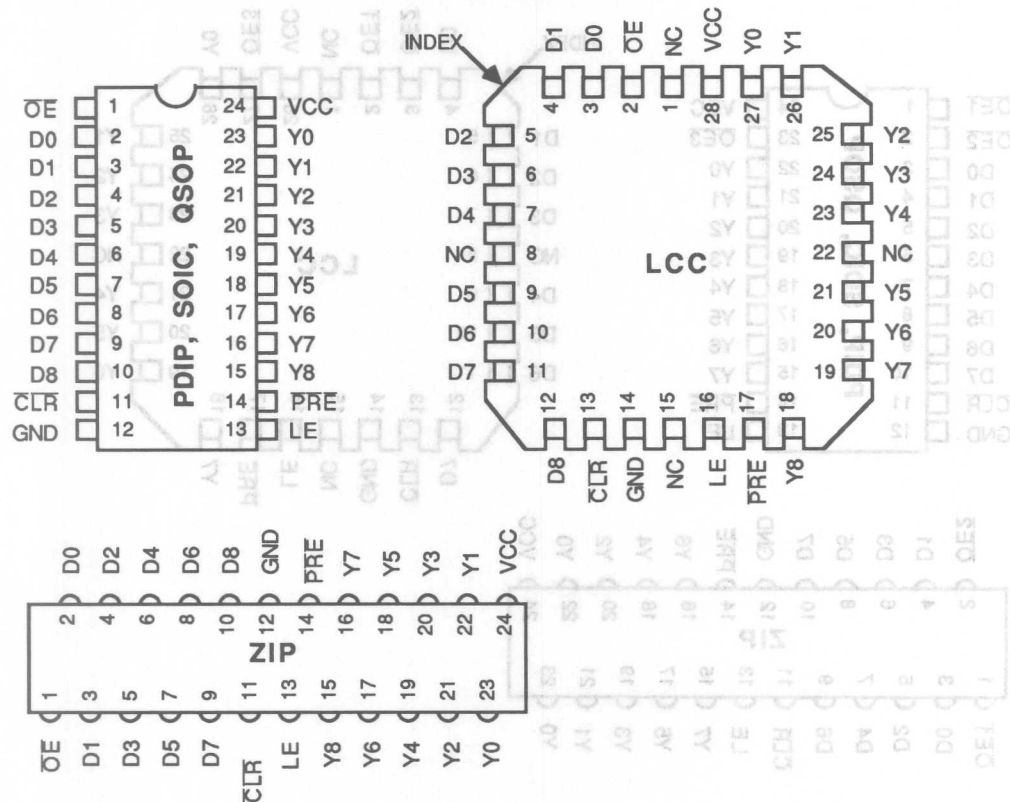
FCT841 LOGIC SYMBOL



PIN DESCRIPTIONS

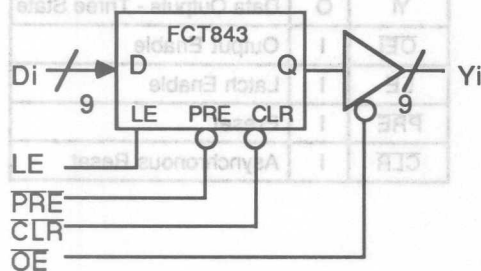
Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
LE	I	Latch Enable
OE	I	Output Enable

FCT843 PIN CONFIGURATIONS



• ALL PINS TOP VIEW

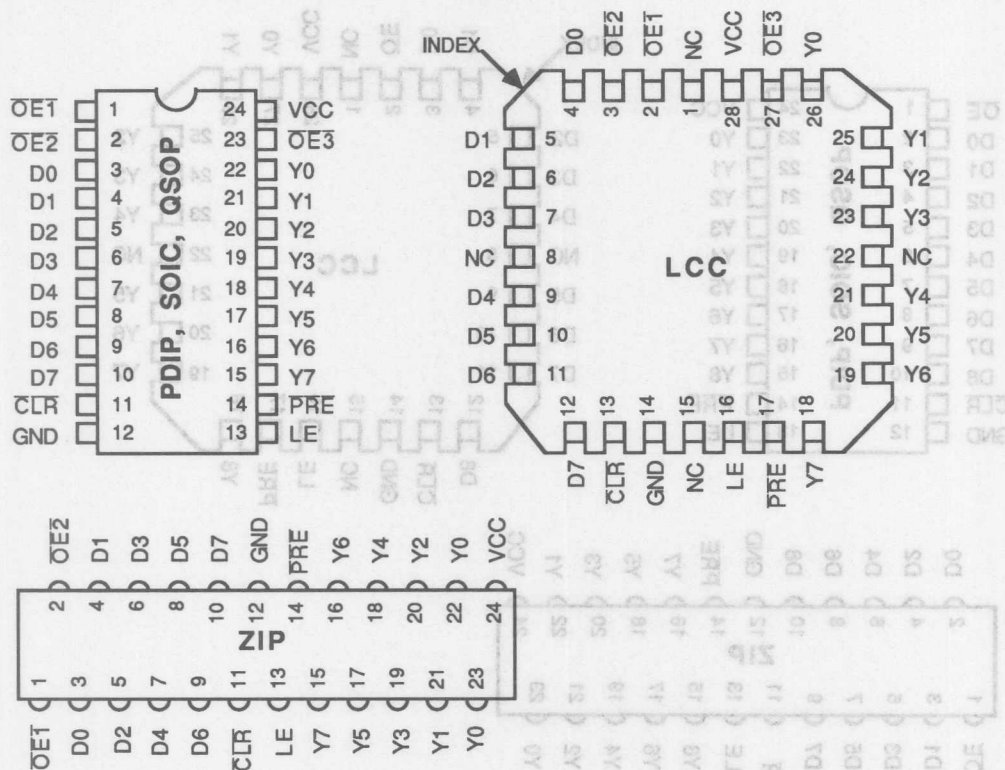
FCT843 LOGIC SYMBOL



PIN DESCRIPTIONS

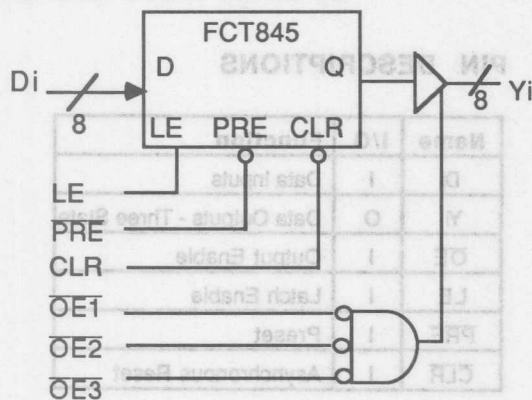
Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
OE	I	Output Enable
LE	I	Latch Enable
PRE	I	Preset
CLR	I	Asynchronous Reset

FCT845 PIN CONFIGURATIONS



• ALL PINS TOP VIEW

FCT845 LOGIC SYMBOL



PIN DESCRIPTIONS

Name	I/O	Function
D_i	I	Data Inputs
Y_i	O	Data Outputs - Three State
OE_i	I	Output Enable
LE	I	Latch Enable
PRE	I	Preset
$\overline{CLR}$	I	Asynchronous Reset

FUNCTION TABLES -

QSFCT841, 2841

Inputs			Int.	O/P	Function
OE	LE	DI	QI	YI	
H	X	X	X	Z	Hi-Z
L	X	X	H	H	Output Enabled
L	X	X	L	L	Output Enabled
X	H	H	H	X	Transparent
X	H	L	L	X	Transparent
X	L	X	NC	X	Latched

QSFCT843/5, 2843/5

Inputs					Int.	O/P	Function
CLR	PRE	OE	LE	DI	QI	YI	
H	H	H	X	X	X	Z	Hi-Z
X	X	L	X	X	H	H	Output Enabled
X	X	L	X	X	L	L	Output Enabled
H	H	L	H	H	H	H	Transparent
H	H	L	H	L	L	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset

Notes:

- NC = No Change from the previous state
- H = HIGH
- L = LOW
- Z = High Impedance
- Int. = Internal

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3-10,13	4	4	5	7	pF
15-22	6	6	7	9	pF
2,11,14,23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Output Enabled	H	X	X	X	X	H	H	H
Output Enabled	L	L	X	X	L	X	X	X
Transparent	H	H	H	H	L	H	H	H
Transparent	L	L	L	L	H	L	H	H
Latched	NC	NC	X	L	L	H	H	H
Preset	H	H	X	X	L	L	H	H
Clear	L	L	X	X	L	L	H	L
Preset	H	H	X	X	L	L	L	L

Notes:
NC = No Change from the previous state
H = HIGH
L = LOW
Z = High Impedance
Int. = Internal

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs	2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs	-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs	-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$ $0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)	-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$	50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)	-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$ $I_{oh} = 15 \text{ mA (MIL)}$ $I_{oh} = 24 \text{ mA (COM)}$	2.4 2.4	- -	- -	Volts
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$ $I_{ol} = 32 \text{ mA (MIL)}$ $I_{ol} = 48 \text{ mA (COM)}$	- -	- -	0.50 0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	- -	- -	0.50 0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$ $I_{ol} = 12 \text{ mA (MIL)}$ $I_{ol} = 12 \text{ mA (COM)}$	21 24	28 28	38 35	Ω

- Notes:
1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
 2. Not more than one output should be shorted and the duration is ≤ 1 second.
 3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_I = 3.4V)
3. For flipflops Q_{ccd} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	mA
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/MHz

1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is 25 seconds.
3. These parameters are guaranteed by design but not tested.

QSFACT841/3/5T, 2841/3/5T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Clod = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes	841A 843A 845A 2841A 2843A 2845A	841B 843B 845B 2841B 2843B 2845B	841C 843C 845C 2841C 2843C 2845C	Unit
		(1)				
t PHL t PLH	Data to Y Delay OE=low, FCT841/3/5	Com		9	6.5	5.5
		MII		10	7.5	6.3
		Com	2,3	13	13	13
		MII	2,3	15	15	15
	Data to Y Delay OE=low, FCT2841/3/5	Com		9.5	6.5	7.0
		MII		11	7.5	8.0
		Com	2,3	20	6.5	13
		MII	2,3	20	7.5	15
t S	Data to LE Setup Time	Com		2.5	2.5	2.5
		MII		2.5	2.5	2.5
t H	Data to LE Hold Time	Com		2.5	2.5	2.5
		MII		3	2.5	2.5
t LEY	LE to Y Delay OE=low, FCT841/3/5	Com		12	8	6.4
		MII		13	10.5	6.8
		Com	2,3	16	15.5	15
		MII	2,3	20	18	16
	LE to Y Delay OE=low, FCT2841/3/5	Com		12	8	8
		MII		13	10.5	10.5
		Com	2,3	16	15.5	15
		MII	2,3	20	18	16

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Clod = 300 pF
- 4) Clod = 5 pF

QSFCT841/3/5T, 2841/3/5T

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$
 Cload = 50 pF, Rload = 500 Ω unless otherwise noted

Symbol	Description	Notes	841A 843A 845A 2841A 2843A 2845A	841B 843B 845B 2841B 2843B 2845B	841C 843C 845C 2841C 2843C 2845C	Unit
t SLEC	CLR to LE Setup Time	Com	3	2.5	2.5	ns
		MII	3	2.5	2.5	
t CLR t PRE	CLR, PRE to Y Delay 843/5	Com	12	8	7	
		MII	14	10	9	
	CLR, PRE to Y Delay 2843/5	Com	12	8	7	
		MII	14	10	9	
t CLRR t PRER	CLR, PRE Recovery Time	Com	2	14	8	8
		MII	2	17	10	9
t LEH	LE Pulse Width High	Com	2	6	4	4
		MII	2	6	4	4
t PREL	PRE, CLR Pulse Width Low	Com	2	8	4	4
		MII	2	9	4	4
t PZH t PZL	Output Enable Time OE to Yi, FCT841	Com		12	8	8
		MII		14	8.5	8.5
		Com	2,3	23	14	14
		MII	2,3	25	15	15
	Output Enable Time OE to Yi, FCT2841	Com		12	8	8
		MII		14	8.5	8.5
		Com	2,3	23	8	8
		MII	2,3	25	8.5	8.5
t PHZ t PLZ	Output Disable Time OE to Yi	Com	2,4	7	6	6
		MII	2,4	9	9	6.5
		Com	2	8	8	7
		MII	2	10	10	7.5

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Cload = 300 pF
- 4) Cload = 5 pF

Q

High Speed CMOS Bus Interface 9 & 10-bit Transceivers

QS54/74FCT861T
QS54/74FCT862T
QS54/74FCT863T
QS54/74FCT864T

QS54/74FCT2861T
QS54/74FCT2862T
QS54/74FCT2863T
QS54/74FCT2864T

FEATURES/BENEFITS

- Pin and function compatible to the 74F861/2/3/4 74FCT861/2/3/4 and 74FCT861T/2T/3T/4T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T861T/2T/3T/4T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A and B speed grades with 6ns tPD for B
- IOL = 48 mA Com., 32 mA Mil.

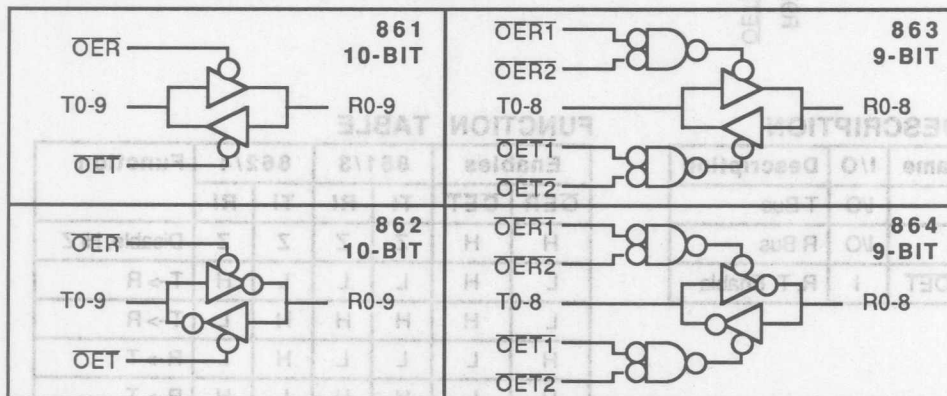
FCT-T 2861T/2T/3T/4T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 8ns tPD for A
- IOL = 12mA Com.

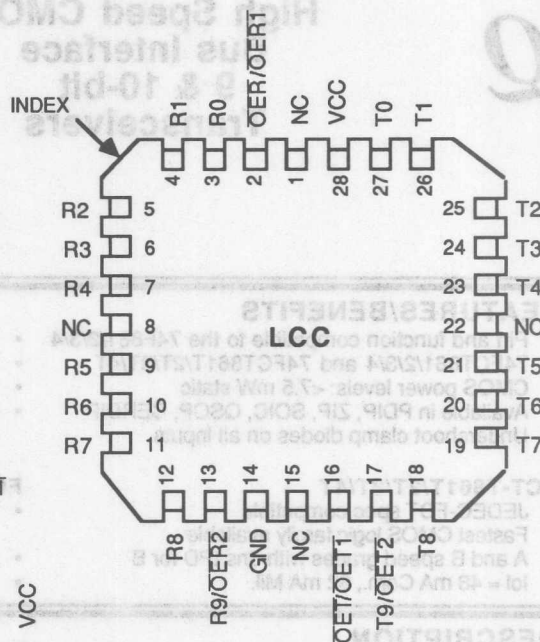
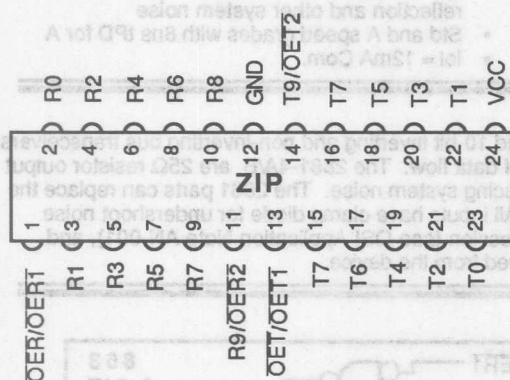
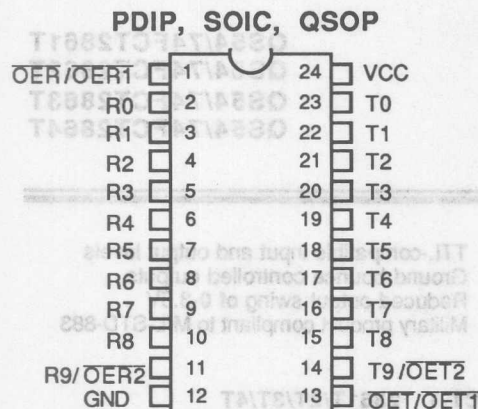
DESCRIPTION

The QSFCT861-4T and QSFCT2861-4T are 9-bit and 10-bit inverting and non-inverting bus transceivers. Separate enables for each bus control the direction of data flow. The 2861-4A/B are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2861 parts can replace the 861 series to reduce noise in an existing design. All inputs have clamp diode for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when VCC is removed from the device.

FUNCTIONAL BLOCK DIAGRAMS



PINOUTS



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin	Name	I/O	Description
Ti		I/O	T Bus
Ri		I/O	R Bus
OER, OET		I	R, T Enable

FUNCTION TABLE

Enables		861/3		862/4		Function
OER	OET	Ti	Ri	Ti	Ri	
H	H	Z	Z	Z	Z	Disable, Hi Z
L	H	L	L	L	H	T->R
L	H	H	H	H	L	T->R
H	L	L	L	H	L	R->T
H	L	H	H	L	H	R->T

H=High, L=Low, Hi-Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
N=Number of Outputs, M=Number of inputs	
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
-----	4	4	5	7	pF
-----	6	6	7	9	pF
1-11,13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

Symbol	Parameter	Test Conditions	Typical Value
V_{IH}	Input High Voltage	$V_{CC} = \text{MIN}$, $V_{OL} = 0.1V$	2.4
V_{IL}	Input Low Voltage	$V_{CC} = \text{MIN}$, $V_{OH} = 2.4V$	0.8
ΔV_I	Input Hysteresis	$V_{CC} = \text{MIN}$, $V_{OH} = 2.4V$	0.2
I_{IH}	Input Current	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1
I_{IL}	Input Current	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1
I_{OH}	Output Current	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1
I_{OL}	Output Current	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1
C_{in}	Input Capacitance	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1
C_{out}	Output Capacitance	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$	1

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is 1 second.
3. These parameters are guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$ Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
V_{ih}	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
V_{il}	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}$, $0 \leq V_{in} \leq V_{CC}$		-	-	5	
I_{os}	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}$, $V_o = \text{GND}$ (2,3)		-60	-	-	mA
I_{or}	Current Drive FCT2XXX	$V_{CC} = \text{Min}$, $V_o = 2.0\text{V}$		50	-	-	mA
V_{ic}	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{in} = 18 \text{ mA}$ (3)		-	-0.7	-1.2	Volts
V_{oh}	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 15 \text{ mA}$ (MIL)	2.4	-	-	Volts
			$I_{oh} = 24 \text{ mA}$ (COM)	2.4	-	-	
V_{ol}	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 48 \text{ mA}$ (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	-	-	0.50	
			$I_{ol} = 12 \text{ mA}$ (COM)	-	-	0.50	
R_{out}	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA}$ (MIL)	21	28	38	Ω
			$I_{ol} = 12 \text{ mA}$ (COM)	24	28	35	

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	1.5	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{cc}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ mHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_i = 3.4V)
3. For flipflops Q_{cc} is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_c can be computed using the above parameters as explained in the Technical Overview section.

9	-	8	-	13	-	15	-	Output Enable Time OE to P or FI, PCT861-4	1.5H 1.5L
18	-	18	-	25	-	20	-	Output Enable Time OE to TI or RI, PCT861-4	
9	-	8	-	13	-	15	-	Output Enable Time OE to TI or RI, PCT861-4	
	-		-	25	-	20	-	Output Enable Time OE to TI or RI, PCT861-4	
7	-	8	-	9	-	8	-	Output Disable Time OE to P or FI	1.5H 1.5L
8	-	7	-	10	-	10	-	Output Disable Time OE to TI or RI	

- Notes
1. Minimum are guaranteed but not tested on production delays.
 2. These parameters are guaranteed but not tested in final production.
 3. C_{load} = 300 pF
 4. C_{load} = 5 pF

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: Ta = 0 °C to 70 °C, Vcc = 5.0V ±5% Military: Ta = -55 °C to +125 °C, Vcc = 5.0V ±10%
 Load = 50 pF, Rload = 500Ω unless otherwise noted.

Symbol	Description	Notes (1)	861-4A, 2861-4A		861-4B, 2861-4B				Unit		
			Com		MII		Com			MII	
			Min	Max	Min	Max	Min	Max		Min	Max
† PHL † PLH	Propagation Delay Ti to/fm Ri, FCT861/3		-	8	-	9	-	6	-	6.5	ns
		2,3	-	15	-	17	-	13	-	14	
	Propagation Delay Ti to/fm Ri, FCT2861/3		-	8	-	9	-	6	-	6.5	
		2,3	-	17	-	18	-		-		
	Propagation Delay Ti to/fm Ri, FCT862/4		-	7.5	-	9	-	5.5	-	6.5	
		2,3	-	14	-	16	-	13	-	14	
† PZH † PZL	Output Enable Time OE to Ti or Ri, FCT861-4		-	12	-	13	-	8	-	9	
		2,3	-	20	-	22	-	15	-	16	
	Output Enable Time OE to Ti or Ri, FCT2861-4		-	12	-	13	-	8	-	9	
		2,3	-	20	-	22	-		-		
	Output Disable Time OE to Ti or Ri	2,4	-	9	-	9	-	6	-	7	
		2	-	10	-	10	-	7	-	8	

Notes

1. Minimum are guaranteed but not tested on propagation delays.
2. These parameters are guaranteed but not tested in final production.
3. Load = 300 pF
4. Load = 5 pF

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1	General Information
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QuickSwitch Ordering Information

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QuickSwitch Family Characteristics

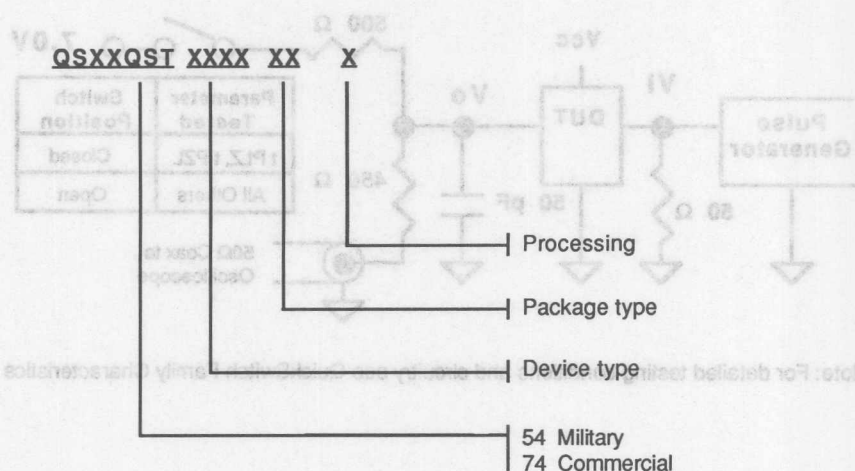
5-17

OST3383155 QuickSwitch Bus Exchange

5-23

OST3384155 QuickSwitch Bus Connect

QuickSwitch Ordering Information



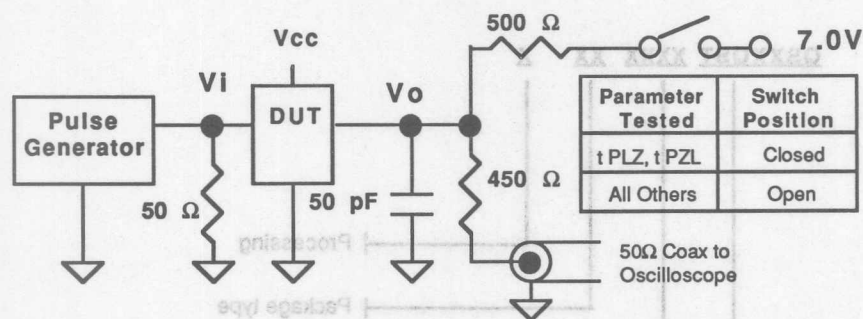
Processing:

Blank - Standard
B - MIL-STD 883

Package Type:

P - Plastic DIP, 300 mil
D - Ceramic DIP, 300 mil
L - Leadless Ceramic Chip Carrier
SO - Small Outline IC, 300 mil
S1 - Small Outline IC, 150 mil
Z - Plastic ZIP
Q - QSOP, Quarter Size Outline Package, 150 mil

QuickSwitch Test Configuration



Note: For detailed testing conditions and circuitry see QuickSwitch Family Characteristics

Package Type:

- P - Plastic DIP, 300 mil
- D - Ceramic DIP, 300 mil
- L - Leadless Ceramic Gull Wing
- SO - Small Outline IC, 300 mil
- SI - Small Outline IC, 150 mil
- Σ - Plastic SIP
- O - QSO, Quarter Size Outline Package, 150 mil

Process:

- B - Bink - Standard
- B - MIL-STD 883

QuickSwitch™ Family Circuit Characteristics

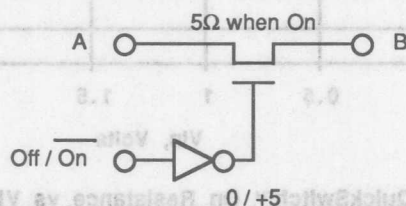
These devices have been designed to operate in excess of 84 mA each. The resistance rises somewhat as the V_Q voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region, the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. This is shown in the on resistance plot below.

QuickSwitch™ Family Characteristics

The QuickSwitch™ family of CMOS Bus Switches introduced by QSI in 1990 by Quality Semiconductor are high speed TTL bus connect devices. When they are enabled, the bus switches directly connect two buses with a connection resistance of less than 5Ω. They are like a 5 nanosecond multi-pole relay for TTL signals with an on resistance of 5Ω. Since these devices directly connect the bus signals they introduce no additional propagation delay, timing skew or noise, are inherently bidirectional and dissipate no additional power. They can replace traditional TTL buffers and transceivers to reduce propagation delay, noise, control complexity and power. Applications of the QuickSwitch™ are discussed in application note AN09.

QuickSwitch™ Circuitry

The basic element of the QuickSwitch™ is a fast, low on resistance, low capacitance, high current capacity switch. The combination of low on resistance and low capacitance is provided by the QCMOS™ short channel length, high performance CMOS process. Each switch consists of an N channel MOS transistor driven by a CMOS gate, as shown below.



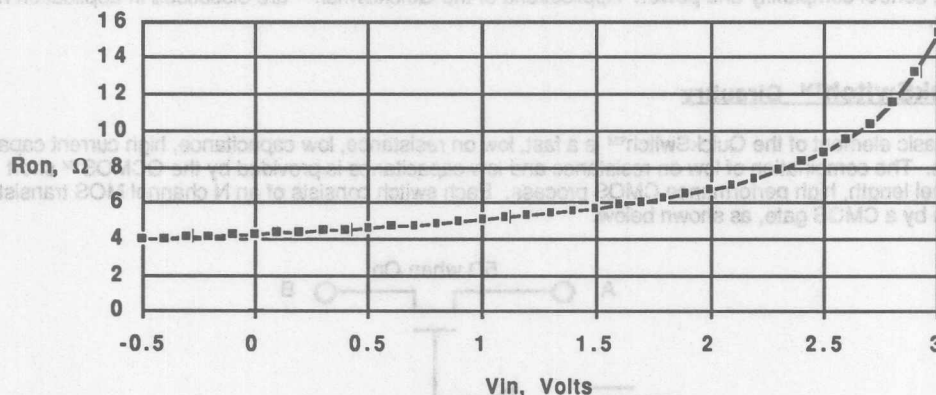
QuickSwitch™ Block Diagram

When the switch is enabled, the gate of the N channel transistor is at V_{cc} (+5 volts) and the device is on, with a typical on resistance of 5 ohms. When disabled, the switch is off. Due to the structure of the N channel transistor, there is no direct leakage and very capacitance across the transistor in the off state. Off state leakage is in the form of diode leakage to the substrate (ground) and is typically 1 nanoampere at room temperature. Off state capacitance across the switch itself is small because the input and output pins are shielded to some degree by the gate, which is grounded.

QuickSwitch™ On Resistance

These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. This is shown in the on resistance plot below. As the I/O voltage rises to approximately 4.0 volts, the transistor turns off. This corresponds to a typical TTL high of 3.5 to 4.0 volts.

The input range also extends to 0.5 volts below ground. Below this voltage, the input clamp diode starts to draw current. Also, the switch will start to turn on at voltages below approximately 0.8 volts, causing leakage between the input and output. This negative signal capability allows video signals of up to 1.0 volt peak to peak around ground to be switched.

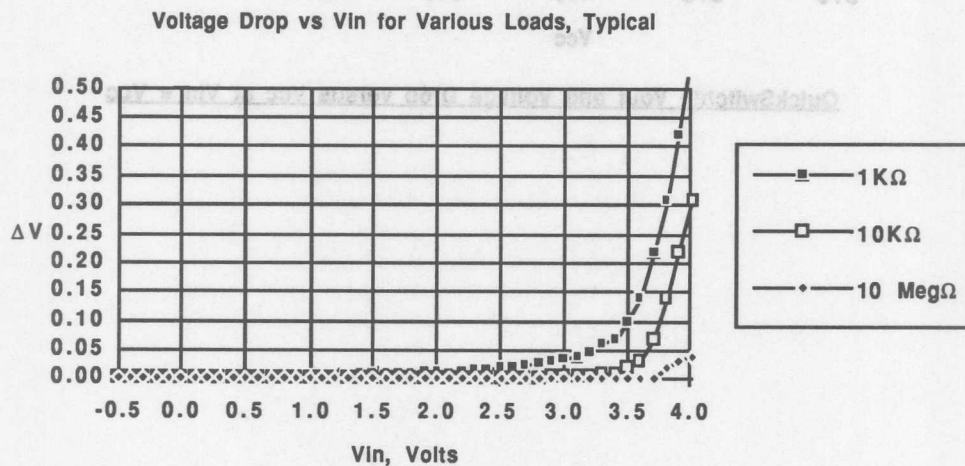
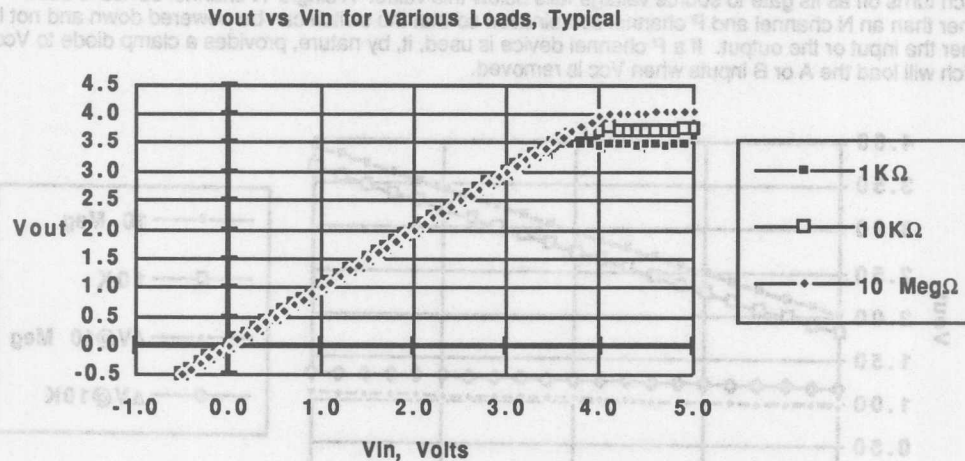
On Resistance vs V_{in} @ 4.75 V_{cc}**QuickSwitch™ On Resistance vs V_{in}**

When the switch is enabled, the gate of the N channel transistor is at V_{cc} (+5 volts) and the device is on with a typical on resistance of 5Ω . When disabled, the switch is off. Due to the structure of the N channel transistor, there is no direct leakage and very capacitance across the transistor in the off state. Off state leakage is in the form of diode leakage to the substrate (ground) and is typically 1 nanampere at room temperature. Off state capacitance across the switch lead is small because the input and output pins are shielded to some degree by the gate, which is grounded.

QuickSwitch™ Family Characteristics

QuickSwitch™ Vout versus Vin

The QuickSwitch™ provides a low resistance connection between inputs and outputs for voltages below 3.0 volts. As the I/O voltage rises above 3 volts, the resistance increases until the switch turns off, at approximately 4.0 volts. This is shown in the Vout versus Vin charts. The switch on resistance is determined by the lower of the voltages on the two I/O pins. The resistance rises as the I/O voltage rises, as shown below.



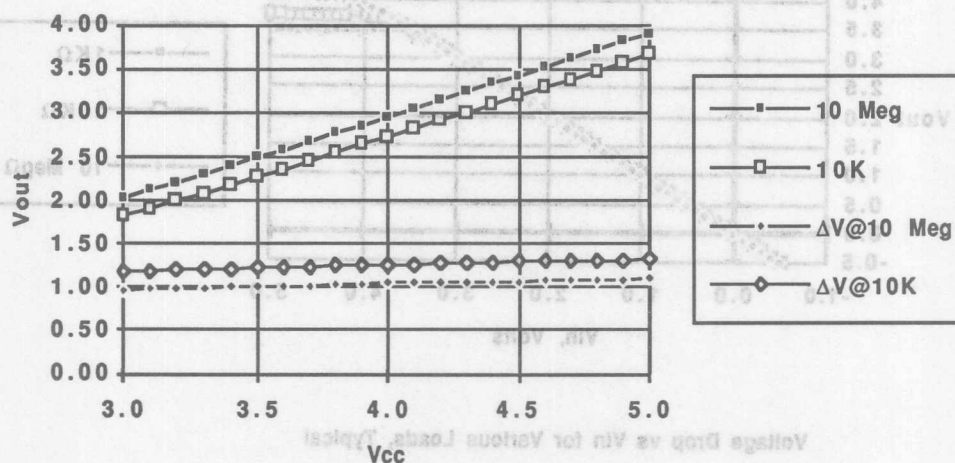
QuickSwitch™ Vout vs Vin

QuickSwitch™ Family Characteristics

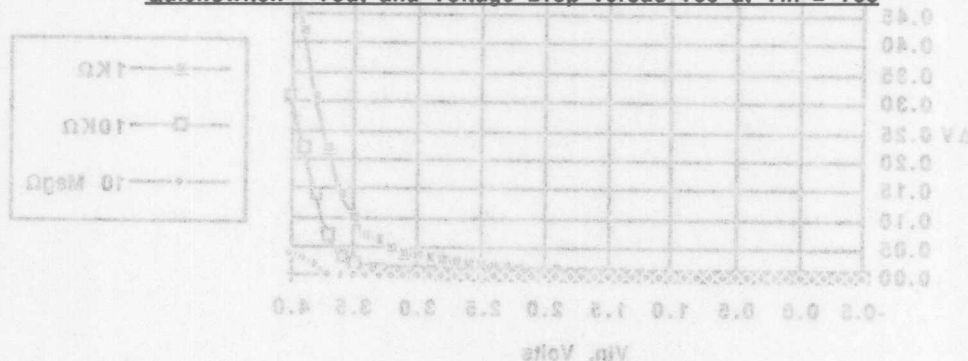
QuickSwitch™ Vout versus Vcc

The QuickSwitch™ output voltage for an input voltage equal to Vcc is approximately 1.0 to 1.5 volts below Vcc. Increasing or decreasing Vcc will increase or decrease the output voltage by the same amount, as shown in the plot below. In this plot, the "ΔV" curves shown the difference between the output and Vcc, i.e. the voltage drop across the switch.

The output limit of 1.0 to 1.5 volts below Vcc is because an N channel transistor is used as the switch which turns off as its gate to source voltage falls below this value. A single N channel device is used rather than an N channel and P channel combination so that the switch can be powered down and not load either the input or the output. If a P channel device is used, it, by nature, provides a clamp diode to Vcc which will load the A or B inputs when Vcc is removed.



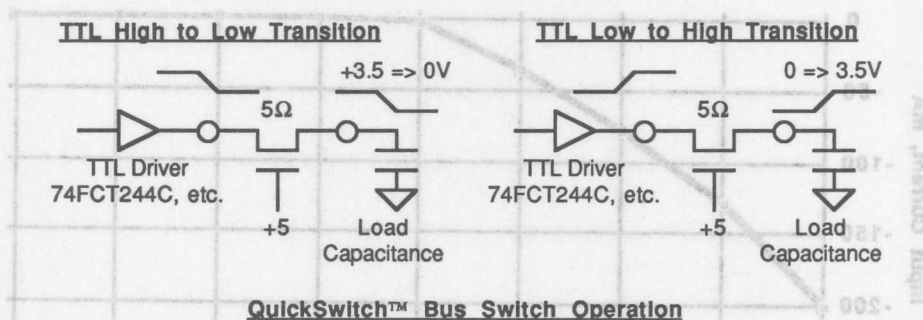
QuickSwitch™ Vout and Voltage Drop versus Vcc at Vin = Vcc



QuickSwitch™ Family Characteristics

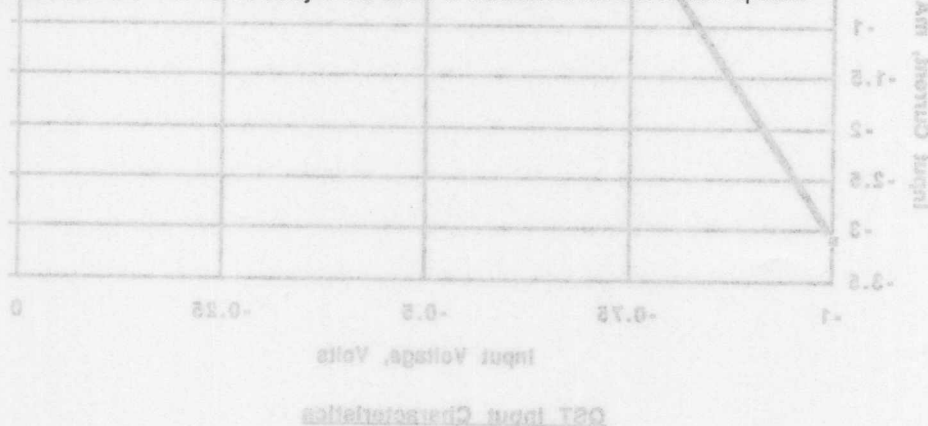
QuickSwitch™ Operation with TTL Signals

The QuickSwitch™ provides a path for a driving device to drive capacitance to ground and to drive capacitance up from ground. This is shown below. When the A (or B) input is driven to a TTL low of 0.0 volts, the N channel transistor is fully on and the B (or A) output will follow it. Likewise, when the A (or B) input is driven from a TTL low of 0.0 volts to a TTL high, the capacitor side of the N channel switch is at 0.0 volts, the switch is fully on and the B (or A) output will follow it through threshold and beyond. This means that the rise and fall time characteristics and waveforms of the B (or A) output will be determined by the TTL driver, not the bus switch. The switch introduces no propagation delay, to a first approximation.



When the QuickSwitch™ is disabled, the N channel transistor gate is at 0.0 volts, and the transistor is off. By the nature of the N Channel transistor design, the A and B pins are fully isolated when the transistor is off. Leakage and capacitance is to the chip substrate (i.e., ground) rather than between input and output. This minimizes feedthrough in the off state. Because only an N channel transistor is used, either A or B pin(s) can be taken to Vcc and above, and the device can be powered down without loading either bus.

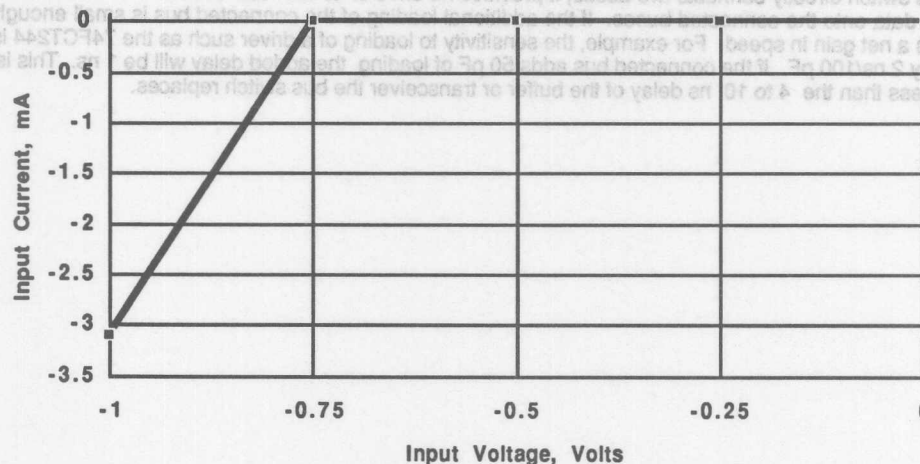
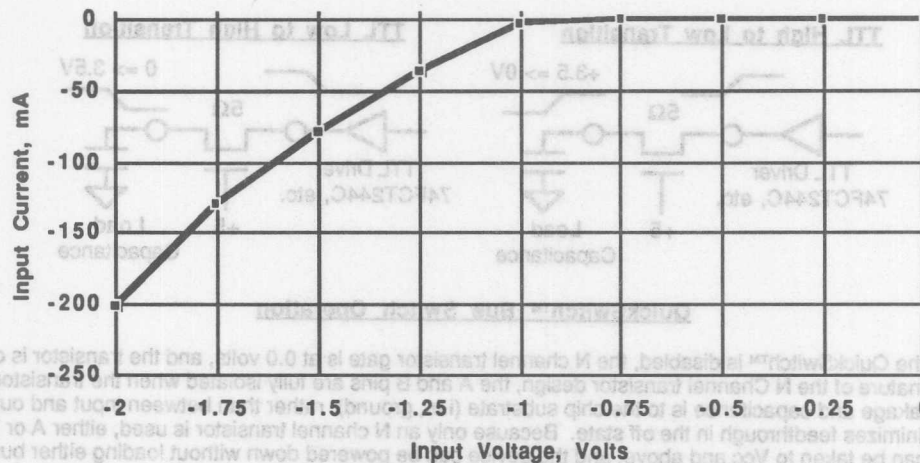
The bus switch can replace drivers and transceivers in systems if bus repowering is not required. Since the bus switch directly connects two buses, it provides no drive of its own but relies on the device that is driving data onto the connected buses. If the additional loading of the connected bus is small enough, there is a net gain in speed. For example, the sensitivity to loading of a driver such as the 74FCT244 is typically 2 ns/100 pF. If the connected bus adds 50 pF of loading the added delay will be 1 ns. This is much less than the 4 to 10 ns delay of the buffer or transceiver the bus switch replaces.



QuickSwitch Family Characteristics

Input Clamp

Since the QuickSwitch™ is intended for high speed logic applications, it has input undershoot clamp diodes. The input clamp diode turns on when the input goes negative, providing clamp action for negative undershoot transients and thereby reducing system noise. Note that there is no positive clamp. The input can go above V_{CC} without conducting current. In fact, actual input leakage is of the order of a few nanoamperes over the input range of 0.0 to 5.0 volts at room temperature. Graphs of typical input characteristics is shown below.

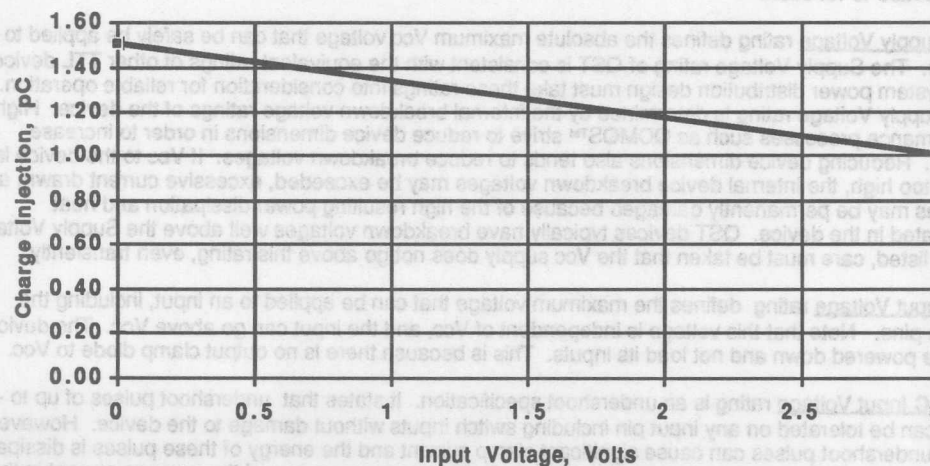


QST Input Characteristics

Charge Injection at Turnoff

When a QuickSwitch™ connected to a capacitive load turns off, the capacitance holds the prior signal level. This provides a hold function which is called a dynamic latch in digital terms or a track and hold in analog terms. When the switch turns off, a small amount of charge is coupled from the switch gate to the outputs. Since the gate transitions from high to low at turn off, this will couple a negative step into the capacitive load. For a 50 pF load, this step will be approximately 30 millivolts. The corresponds to a charge injection of 1.5 picocoulombs. A plot of charge injection versus V_{in} is shown below. To calculate the negative voltage step at turn off, divide the charge injection value in picocoulombs by the capacitance in picofarads.

The hold time for typical capacitances and leakages can be quite long compared to the clock cycle times of fast systems. Assuming a 1 volt change in level and a typical total system leakage of 50 nanoamperes, the hold time is of the order of $(50 \times 10^{-12} / 50 \times 10^{-9}) = 1$ millisecond.



QuickSwitch™ Charge Injection at Turnoff versus V_{in}

Ratings, Specifications and Waveforms

General Comments

In this section, the ratings, specifications and waveforms used in the data sheets are discussed to provide information on their meaning and how they are interpreted.

Absolute Maximum Ratings

The Absolute Maximum ratings define the limits of operation of the QST devices. Operation beyond these limits may cause permanent damage to the device, i.e. it may no longer meet its specifications or may even cease to function.

The Supply Voltage rating defines the absolute maximum Vcc voltage that can be safely be applied to the device. The Supply Voltage rating of QST is consistent with the equivalent ratings of other TTL devices, and system power distribution design must take these ratings into consideration for reliable operation. The Supply Voltage rating is determined by the internal breakdown voltage ratings of the device. High performance processes such as QCMOS™ strive to reduce device dimensions in order to increase speed. Reducing device dimensions also tends to reduce breakdown voltages. If Vcc to the device is taken too high, the internal device breakdown voltages may be exceeded, excessive current drawn, and devices may be permanently damaged because of the high resulting power dissipation and heat generated in the device. QST devices typically have breakdown voltages well above the Supply Voltage rating listed, care must be taken that the Vcc supply does not go above this rating, even transiently.

The Input Voltage rating defines the maximum voltage that can be applied to an input, including the switch pins. Note that this voltage is independent of Vcc, and the input can go above Vcc. The device can be powered down and not load its inputs. This is because there is no output clamp diode to Vcc.

The AC Input Voltage rating is an undershoot specification. It states that undershoot pulses of up to -3 volts can be tolerated on any input pin including switch inputs without damage to the device. However, large undershoot pulses can cause significant clamp current and the energy of these pulses is dissipated in the device. If these pulses have a high duty cycle, the average power and the average current in the undershoot pulses can be significant and must be taken into account to insure that the DC Input Diode Current and the Maximum Power Dissipation ratings are not exceeded.

The DC Input Diode Current defines the rating of the input undershoot clamp diode. The average current from undershoot clamp pulses must be below this rating.

The DC Switch Current Maximum Sink Per Pin defines the maximum DC switch current that can be drawn per switch to pull down an external load to ground.

The Maximum Power Dissipation defines the maximum total power dissipation capability of the device. It represents a package power dissipation limit for the device, above which the die will overheat and be damaged. Note that the power dissipation limit includes power dissipated by the input clamp diodes as well as power from Vcc for driving internal circuitry.

The Storage Temperature rating defines the maximum temperature that the packages may be subject to for long term storage. Long term storage above this temperature may cause degradation of the chip. This is a precautionary specification. Chips cannot be subjected to extremely high temperatures, significantly above the Storage Temperature rating, even if unpowered and be expected to work reliably thereafter.

Input and Switch Capacitance

QuickSwitch Family Characteristics

Each input control pin and switch pin has a capacitance associated with it. The switch pins have two capacitance values, one for the off state and one for the on state. In the off state, each switch pin is isolated and has a capacitance to ground. In the on state, two pins are connected, and the capacitance seen at one pin includes the capacitance of the other pin to which it is connected.

DC Electrical Characteristics

The DC Electrical Specifications define the input requirements for valid operation, output specifications during valid operation and responses to applied signals such as leakage currents, clamp voltages and output resistance.

V_{ih} defines the minimum DC input voltage for a TTL high. This applies to the control input pins. Typical TTL high voltages applied to inputs are 3.5 to 5.0 volts. V_{il} defines the maximum DC input voltage for a TTL low. This applies to the control input pins. Typical TTL low voltages applied to inputs are 0.0 to 0.5 volts. Note that the AC characteristics are guaranteed for input switching values of 3.0 volts for a TTL high and 0.0 volts for a TTL low.

ΔV_t defines the typical input hysteresis. This applies to the control input pins. Input hysteresis is the difference in input threshold voltages for low-to-high and high-to-low input transitions. This specification guarantees that there is some hysteresis and gives its typical value.

I_{ih} and I_{il} define the maximum input leakage current; I_{oz} defines the maximum switch off state leakage current. The maximum input or switch leakage is $\pm 1 \mu A$, and a typical value is 1-5 nanoamperes at 25 °C.

I_{os} defines switch short circuit current for one input at V_{cc} and the other input at ground. This is an indication of drive capability of the switch to pull up capacitance from ground.

V_{ic} defines the input undershoot clamp voltage for a specified input current. It guarantees that the input undershoot clamp is sufficiently low impedance to provide useful clamping action.

R_{on} defines the range of resistance values for resistor devices. It is guaranteed over voltage and temperature. This is an incremental resistance measured at the test current. The resistance is calculated as $(V_{out} \text{ at } 12 \text{ mA} - V_{out} \text{ at } 0 \text{ mA}) \text{ divided by } (12 \text{ mA} - 0 \text{ mA})$.

Recommended Operating Conditions

The DC Electrical Characteristics define the limits of operation for the device. The recommended operating conditions are stated at the top of the DC Electrical Characteristics and Switching Characteristics specifications. The recommended operating conditions are those the parts are expected to encounter in normal operation. The switching characteristics are guaranteed under these conditions. The recommended operating conditions for QST logic cover operating temperatures of 0 to 70 °C for commercial and -55 to + 125 °C for military temperature range parts and a nominal Vcc voltage of 5.0 volts with an operating range of within $\pm 10\%$ of this value (i.e. 4.5 to 5.5 volts).

Switching Characteristics

Data Propagation Delay Specifications: t_{PLH} , t_{PHL}

Data propagation delay specifications through the switch are shown for reference only. Actual propagation delay through the switch is very low, approximately the propagation delay of a 5 ohm resistor. For a 50 pF load, this is equivalent to a propagation delay of 0.25 nanosecond.

Switch Turn On and Turn Off Delay Specifications: t_{PZH} , t_{PZL} , t_{PHZ} , t_{PLZ}

Switch turn on and turn off delay specifications cover two conditions: going from the high impedance (high-Z) condition to the low impedance, on state condition, and going from the low impedance, on state condition to the high impedance (high-Z) condition. In the high-Z to low-Z case, propagation delay measurements are done in the same manner as any other: the output must settle to the correct logic high or low state before the stated maximum time, t_{PZH} or t_{PZL} .

In the low-Z to high-Z case, the output must be in the high-Z condition by the stated maximum time, t_{PHZ} or t_{PLZ} . Special measurement must be done to detect the high-Z condition. Since the high-Z condition means the output is undriven, the high-Z condition is detected by using an external resistor load network to drive the output away from the previous high or low logic state to a level determined by the load network. The output will start to move to this level when the output has turned off. This is detected by a change in the output level away from the previous high or low. The output is defined as being in the high-Z state when the output moves from its prior high or low state by 300 millivolts. Note that this specification is usually guaranteed by design, verified by device characterization and not tested in production.

Switch Selection Delay Specifications: t_{BX}

Switch selection or multiplex delay specifications define the time required to turn off one set of switches and turn on another set. It is measured from the transition of the control input to the switched output changing state high or low.

QuickSwitch Family Characteristics

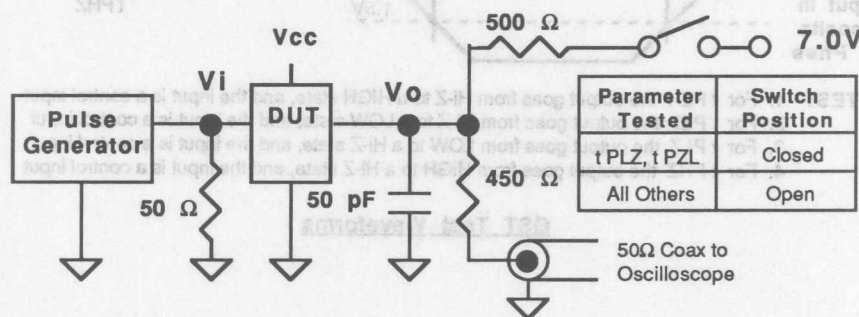
AC Test Conditions

AC test conditions are concerned with propagation delays at outputs relative to applied signals. QST is tested using industry standard test signals. Input signals transition between levels of 0.0 volts for a logic low to 3.0 volts for a logic high with a transition time of 2.5 nanoseconds measured from the 10% to 90% points of the signal transition. Rise and fall times of 1 ns are used to test minimum pulse widths such as clock width, t_W .

AC Test Circuitry

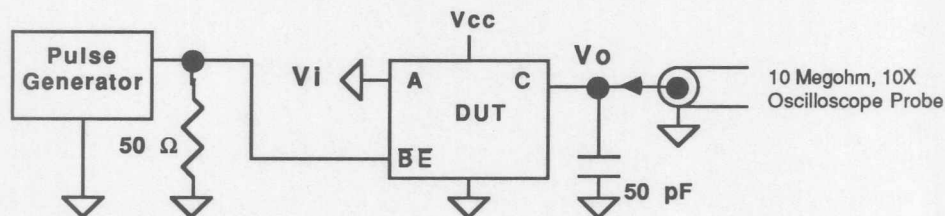
The AC test circuitry is shown below. This test circuitry is an industry standard for QST logic and many other high performance TTL logic families. Inputs under test are driven by a pulse generator with an output impedance of 50 ohms. Outputs are loaded with 50 picofarads and 500 ohms to ground except for three state tests. The 500 ohm resistor to ground is typically used as a part of a 10:1 probe for an oscilloscope used to measure the output. The 10:1 probe consists of a 450 ohm resistor feeding into a 50 ohm coax cable to the oscilloscope. This provides a 10:1 probe with no appreciable capacitive loading by the 450 ohm resistor. This is the preferred scheme for correlation to QSI test data.

Switch turn off testing of t_{PLZ} and t_{PZL} modifies the test load. An additional 500 ohm resistor is switched to +7.0 volts for these tests. This biases the output to 3.5 volts for testing the transition from high-Z to a TTL low and from a TTL low to high-Z. The 3.5 volts is an industry standard value chosen to represent the realistic situation of transitioning to or from a potential TTL high at the output under high-Z conditions.



QST Test Circuit

The charge injection test circuitry is shown below. Charge injection is measured at turn off for 0.0 volts V_{in} with a 50 pF load. This results in a negative turn off step of 30 mV for 1.5 pC charge injection.

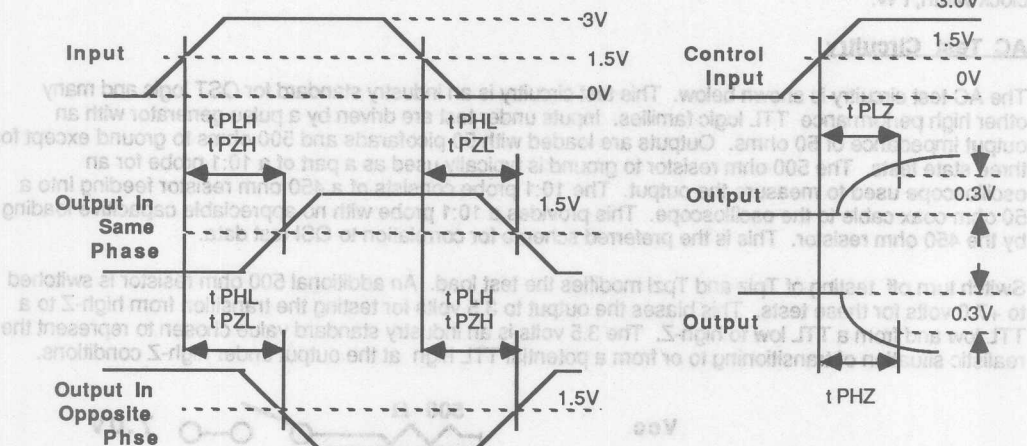


QST Charge Injection Test Circuit

QuickSwitch Family Characteristics

AC Test Waveforms

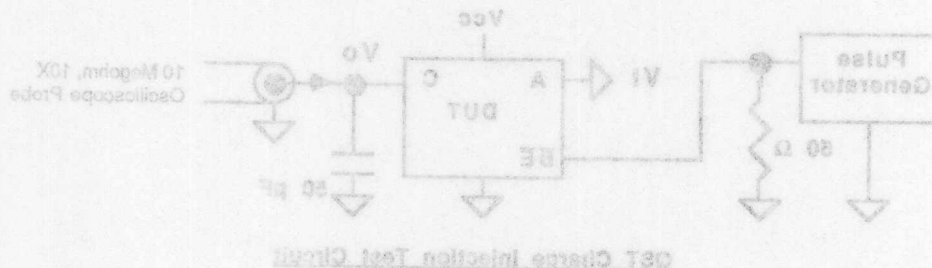
General waveforms are shown below for testing all input to output delays. Outputs are shown for normal and inverted signal phases, as determined by the logic function being tested. Switch turn off test waveforms are also shown, indicating the 300 millivolt change in level used to detect the high-Z condition.



- NOTES:**
1. For t_{PZH} the output goes from Hi-Z to a HIGH state, and the input is a control input
 2. For t_{PZL} the output goes from Hi-Z to a LOW state, and the input is a control input
 3. For t_{PLZ} the output goes from LOW to a Hi-Z state, and the input is a control input
 4. For t_{PHZ} the output goes from HIGH to a Hi-Z state, and the input is a control input

QST Test Waveforms

The charge injection test circuitry is shown below. Charge injection is measured at turn off for 0.0 volts V_{in} with a 50 pF load. This results in a negative turn off step of 30 mV for 1.5 pC charge injection.



Q

High Speed CMOS Bus Exchange Switches

QS54/74QST3383
QS54/74QST3583
(*3583 PRELIMINARY)

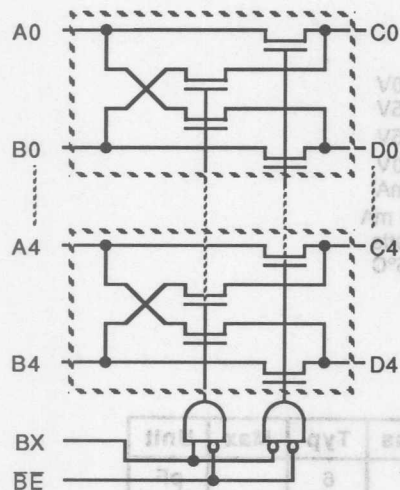
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay (3383)
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- 3583 is 25Ω version for low noise
- Bus exchange allows nibble swap
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin DIP, ZIP, SOIC and QSOP

DESCRIPTION

The QS54/74QST3383 and 3583 each provide two sets of ten high-speed CMOS TTL-compatible bus switches. The low on resistance (5Ω) of the 3383 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The 3583 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The bus enable (BE) signal turns the switches on. The bus exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM



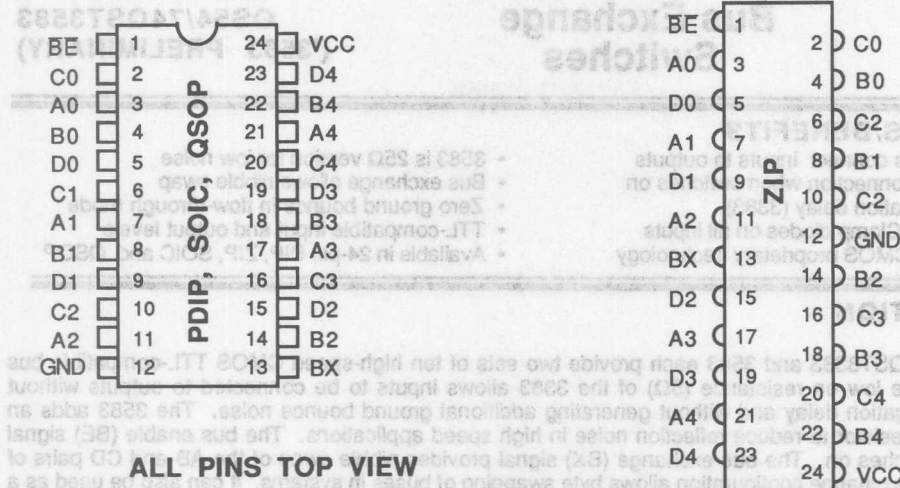
PIN DESCRIPTION

Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
BE	I	Bus Switch Enable
BX	I	Bus Exchange

FUNCTION TABLE

BE	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

PIN CONFIGURATIONS



ALL PINS TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0V$	6		pF
Coff	A/B I/O Capacitance, Switch Off	$V_{in} = 0V$	6		pF
Con	A/B I/O Capacitance, Switch On	$V_{in} = 0V$	10		pF

Capacitance is guaranteed but not tested

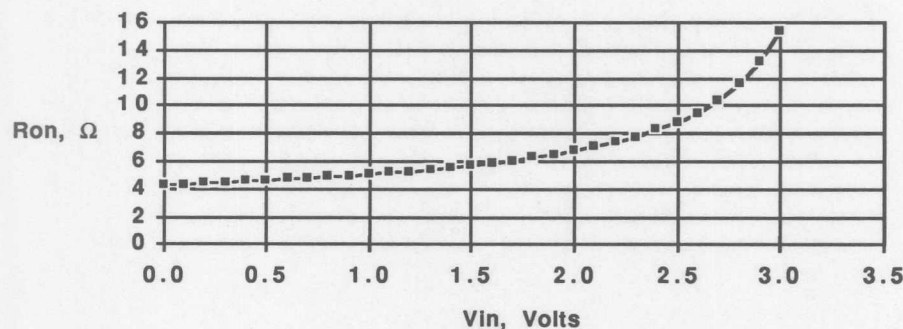
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$ Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
$ I_{in} $	Input Leakage Current	$0 \leq V_{in} \leq V_{CC}$	-	-	1	μA
$ I_{OZ} $	Off State Current (Hi-Z)	$0 \leq A, B \leq V_{CC}$	-	.001	1	μA
$ I_{OS} $	Short Circuit Current (2)	A (B) = 0V, B (A) = V_{CC}	100	-	-	mA
V_{IC}	Clamp Diode Voltage	$V_{CC} = \text{Min}$, $I_{in} = -18\text{ mA}$	-	-0.7	-1.2	Volts
R_{ON}	Switch On Resistance (Notes: 3,4)	$V_{CC} = \text{Min}$, $V_{in} = 0.0\text{ Volts}$ $I_{ON} = 48\text{ mA}$	33XX	-	5	Ω
			35XX	24	28	Ω
		$V_{CC} = \text{Min}$, $V_{in} = 2.4\text{ Volts}$ $I_{ON} = 15\text{ mA}$	33XX	-	10	Ω
			35XX	24	35	Ω

Notes:

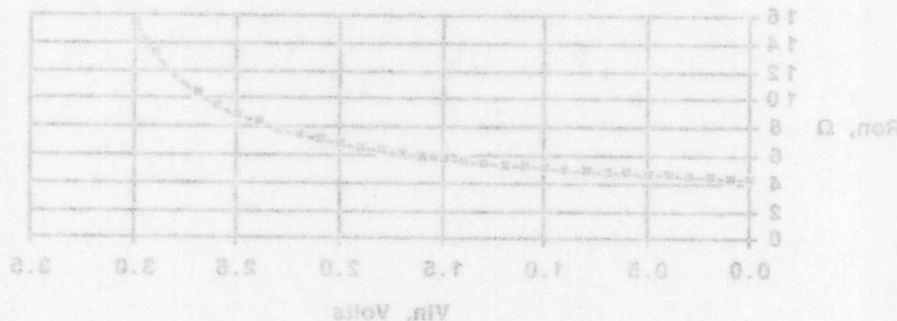
- Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^\circ\text{C}$.
- Not more than one output should be used to test this high power condition, and the duration is ≤ 1 second.
- Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.
- 35xx R_{ON} is a preliminary specification.

On Resistance vs V_{in} @ 4.75 V_{CC} (338X Only)

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{MAX}, V_i = \text{GND or } V_{CC}, f = 0$	-	-	1.5	mA
ΔI_{CC}	Pwr Supply Current, per Input High (2)	$V_{CC} = \text{MAX}, \text{Input} = 3.4 \text{ V}, f = 0$ Per control input	-	-	2.5	mA
Q_{CCd}	Dynamic Pwr Supply Current per mHz (3)	$V_{CC} = \text{MAX}, \text{A \& B pins open},$ Control input toggling @ 50% duty cycle	-	-	0.25	mA/mHz
I_C	Total Power Supply Current (4,5)	$V_{CC} = \text{MAX}, \text{A \& B pins at } 0.0\text{V},$ Control inputs toggling @ 50% duty cycle $V_{ih} = 3.4\text{V}, f_{\text{clock}} = 10 \text{ mHz}$	-	-	9.0	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i=3.4\text{V}$, control inputs only). A and B pins do not contribute to I_{CC} .
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_C = I_{CC} + \Delta I_{CC} D_h N_t + Q_{CCd} (f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for each TTL High input ($V_i=3.4\text{V}$, control inputs only)
 D_h = Duty Cycle for each TTL input that is High (control inputs only)
 N_t = Number of TTL inputs that are at DH (control inputs only)
 f_i = frequency that the inputs are toggled (control inputs only).
- Note that activity on A and/or B inputs do not contribute to I_C if A and B inputs are between gnd and V_{CC} . The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_C will be equal to I_{CC} only regardless of activity on the A and B pins.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		MII		Unit
			Min	Max	Min	Max	
† PLH † PHL	Data Propagation Delay Ai to Bi, Bi to Ai	338X 2,3		0.25		0.25	ns
		358X 2,3,7		1.25		1.25	ns
† PZH † PZL	Switch Turn On Delay BE to Ai, Bi	338X 1	1.5	6.5	1.5	7.5	ns
		358X 1,7	1.5	7.5	1.5	8.5	ns
† PLZ † PZL	Switch Turn Off Delay BE to Ai, Bi	338X 1,2	1.5	5.5	1.5	6.5	ns
		358X 1,2,7					
† BX	Switch Multiplex Delay BX to Ai, Bi	338X 1	1.5	6.5	1.5	7.5	ns
		358X 1,7	1.5	7.5	1.5	8.5	ns
Qci	Charge Injection, Typical	338X 4,6		1.5		1.5	pC
		358X 4,6,7					
Qdci	Differential Charge Injection, Typical	338X 5,6		<.5		<.5	pC
		358X 5,6,7					

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and load alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
- 5) Measured at switch turn off through bus multiplex, A to C => A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: TA = 0°C to 70°C, V_{CC} = 5.0V±5% Military: TA = -55°C to 125°C, V_{CC} = 5.0V±10%
 Load = 50 pF, P_{load} = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t _{PLH}	Data Propagation Delay	338X	0.3		0.25		ns
t _{PHL}	A to B, B to A	358X	2.3, 7	1.25		1.25	ns
t _{PSH}	Switch Turn On Delay	338X	1	1.5	0.5	1.5	ns
t _{PZL}	BE to A, B	338X	1.7	1.5	1.5	0.5	ns
t _{PLZ}	Switch Turn Off Delay	338X	1.5	1.5	1.5	0.5	ns
t _{PZL}	BE to A, B	358X	1.2, 7				
t _{BX}	Switch Multiplex Delay	338X	1	1.5	0.5	1.5	ns
	BX to A, B	358X	1.7	1.5	1.5	0.5	ns
t _{CH}	Charge Injection, Typical	338X	4.5		1.5		pC
		358X	4.8, 7				
t _{CH}	Differential Charge Injection, Typical	338X	5.5				pC
		358X	5.8, 7				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and load alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the typical times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{in} at A = 0.0 volts.
- 5) Measured at switch turn off through bus multiplexer, A to C, A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, V_{in} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.



High Speed CMOS 10-bit Bus Switches

QS54/74QST3384
QS54/74QST3584
(*3584 PRELIMINARY)

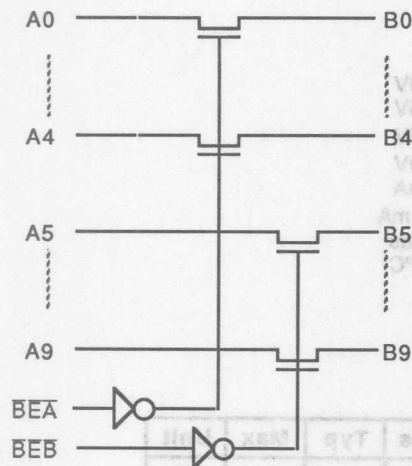
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay (3384)
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- 3584 is 25Ω version for low noise
- Two enables control 5 bits each
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin PDIP, ZIP, SOIC and QSOP

DESCRIPTION

The QS54/74QST3384 and 3584 each provide a set of ten high-speed CMOS TTL-compatible bus switches. The low on resistance (5Ω) of the 3384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The 3584 adds an internal 25Ω resistor to reduce reflection noise in high speed applications. The bus enable (BE) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

FUNCTIONAL BLOCK DIAGRAM



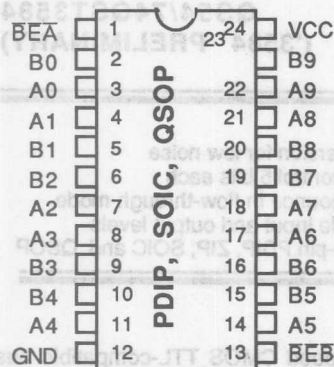
PIN DESCRIPTION

Name	I/O	Function
A0-9	I/O	Bus A
B0-9	I/O	Bus B
BEA, BEB	I	Bus Switch Enable

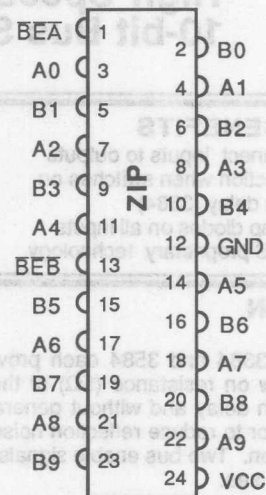
FUNCTION TABLE

BEA	BEB	B0-4	B5-9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-4	Hi-Z	Connect
H	L	Hi-Z	A5-9	Connect
L	L	A0-4	A5-9	Connect

PIN CONFIGURATIONS



ALL PINS TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage V_I	-0.5V to $V_{CC} + 0.5V$
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

CAPACITANCE

$T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0V$, $V_{out} = 0V$

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance, Controls	$V_{in} = 0V$	6		pF
Coff	A/B I/O Capacitance, Switch Off	$V_{in} = 0V$	6		pF
Con	A/B I/O Capacitance, Switch On	$V_{in} = 0V$	10		pF

Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

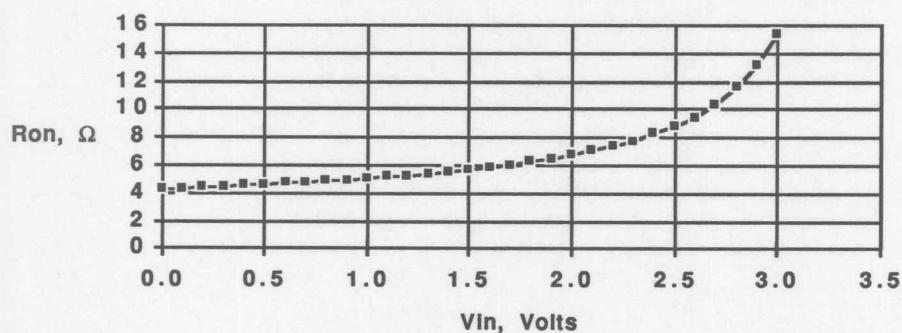
Commercial TA = 0°C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125°C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
lin	Input Leakage Current	0 ≤ Vin ≤ Vcc	-	-	1	μA
loz	Off State Current (Hi-Z)	0 ≤ A, B ≤ Vcc	-	.001	1	μA
los	Short Circuit Current (2)	A (B) = 0V, B (A) = Vcc	100	-	-	mA
Vic	Clamp Diode Voltage	Vcc = Min, lin = -18 mA	-	-0.7	-1.2	Volts
Ron	Switch On Resistance (Notes: 3,4)	Vcc = Min, Vin = 0.0 Volts Ion = 48 mA	33XX	-	5	7 Ω
			35XX	24	28	35 Ω
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	33XX	-	10	15 Ω
			35XX	24	35	48 Ω

Notes:

- Typical values indicate VCC=5.0V and TA=25°C.
- Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
- Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.
- 35xx Ron is a preliminary specification.

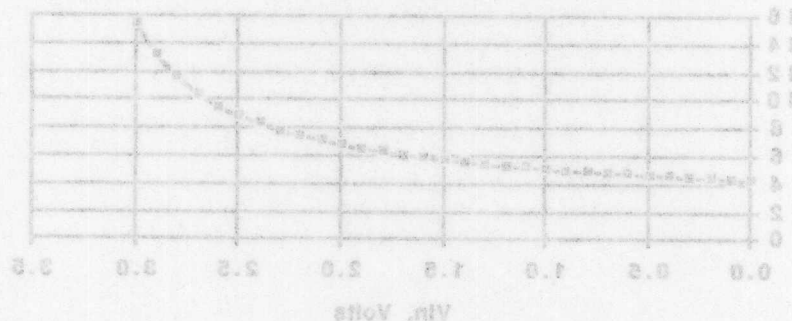
On Resistance vs Vin @ 4.75 Vcc (338X Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
I_{cc}	Quiescent Power Supply Current	$V_{cc} = \text{MAX}, V_i = \text{GND or } V_{cc}, f = 0$	-	-	1.5	mA
ΔI_{cc}	Pwr Supply Current, per Input High (2)	$V_{cc} = \text{MAX}, \text{Input} = 3.4 \text{ V}, f = 0$ Per control input	-	-	2.5	mA
Q_{ccd}	Dynamic Pwr Supply Current per mHz (3)	$V_{cc} = \text{MAX}, \text{A \& B pins open},$ Control input toggling @ 50% duty cycle	-	-	0.25	mA/ mHz
I_c	Total Power Supply Current (4,5)	$V_{cc} = \text{MAX}, \text{A \& B pins at } 0.0 \text{ V},$ Control inputs toggling @ 50% duty cycle $V_{ih} = 3.4 \text{ V}, f_{\text{clock}} = 10 \text{ mHz}$	-	-	9.0	mA

- For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_i = 3.4 \text{ V}$, control inputs only). A and B pins do not contribute to I_{cc} .
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
- $I_c = I_{\text{Quiescent}} + I_{\text{Inputs}} + I_{\text{Dynamic}}$
 $I_{cc} = \text{Quiescent Current}$
 $\Delta I_{cc} = \text{Power Supply Current for each TTL High input } (V_i = 3.4 \text{ V}, \text{ control inputs only})$
 $D_h = \text{Duty Cycle for each TTL input that is High (control inputs only)}$
 $N_t = \text{Number of TTL inputs that are at } D_h \text{ (control inputs only)}$
 $f_i = \text{frequency that the inputs are toggled (control inputs only)}$
- Note that activity on A and/or B inputs do not contribute to I_c if A and B inputs are between gnd and V_{cc} . The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_c will be equal to I_{cc} only regardless of activity on the A and B pins.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE (338x only)

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Note	Com		Mil		Unit
				Min	Max	Min	Max	
† PLH † PHL	Data Propagation Delay Ai to Bi, Bi to Ai	338X	2,3		0.25		0.25	ns
		358X	2,3,7		1.25		1.25	ns
† PZH † PZL	Switch Turn On Delay BEA, BEB to Ai, Bi	338X	1	1.5	6.5	1.5	7.5	ns
		358X	1,7	1.5	7.5	1.5	8.5	ns
† PLZ † PZL	Switch Turn Off Delay BEa, BEB to Ai, Bi	338X	1,2	1.5	5.5	1.5	6.5	ns
		358X	1,2,7					
Qci	Charge Injection, Typical	338X	4,6		1.5		1.5	pC
		358X	4,6,7					

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and aloa alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
- 5) Characterized parameter but not 100% tested.
- 6) Characterized parameter. Not 100% tested.
- 7) Preliminary data, subject to change.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (338X only)

Commercial TA = 0°C to 70°C, VCC = 5.0V±5%, Military TA = -55°C to 125°C, VCC = 5.0V±10%
 Load = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Max	Min	Max	Min	
1 PLH	Data Propagation Delay A to B, B to A	338X	5.3		0.25		ns
1 PHL		338X	5.3.7		1.25		ns
1 PZH	Switch Turn-On Delay BEA, BEB to A, B	338X	1	1.5	8.5	1.5	ns
1 PZL		338X	1.7	1.5	7.5	1.5	ns
1 PLZ	Switch Turn-Off Delay BEA, BEB to A, B	338X	1.5	1.5	8.5		ns
1 PZL		338X	1.2.7				
Qd	Charge Injection, Typical	338X	4.8		1.5		pc
		338X	4.8.7				

Notes:

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and also alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- 4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
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Ground Bounce Noise in TTL Logic

Application
Note
AN-01

By David C. Wyland

High speed TTL octal drivers such as the FCT244 can generate ground bounce noise when driving capacitive loads at high speed. On the FCT244, ground bounce occurs when seven of the eight outputs are switching high-to-low with a high capacitance load, and the eighth output is held a constant low. In this case, the high-to-low transition of the outputs causes capacitive current ($I=CdV/dt$) to flow in the single ground lead of the FCT244. This current pulse causes a voltage pulse to appear ($V=Ldi/dt$) across the package inductance of the ground lead. This voltage pulse on the unchanging low output is called ground bounce noise. This voltage pulse will appear on the output that is held low, since it shares the common ground pin.

Ground bounce noise is a concern of the system designer because it can affect other circuits in a design. Ground bounce is a chip design problem with system implications. The chip designer tries to achieve the highest speed with an acceptable level of ground bounce. The system designer needs to understand the limits of the combination of chip and package technology represented by ground bounce to know what to expect from future designs. A ground bounce model is a useful tool for achieving these goals. In this paper, we will study ground bounce using an RLC resonant circuit model.

Ground Bounce Example

Figure 1 shows a test setup which allows ground bounce to be measured, and Figure 2 shows typical results.

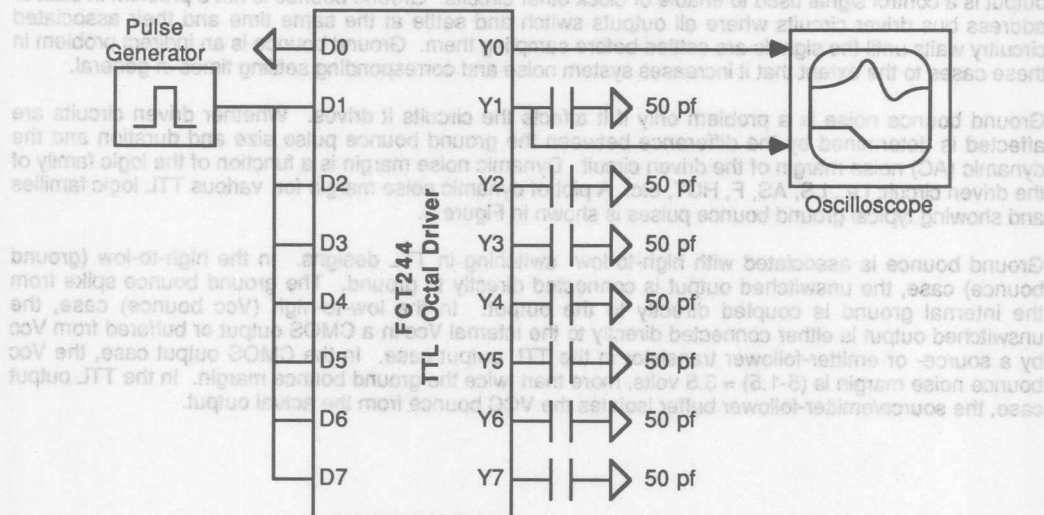


Figure 1: Ground Bounce Test Setup

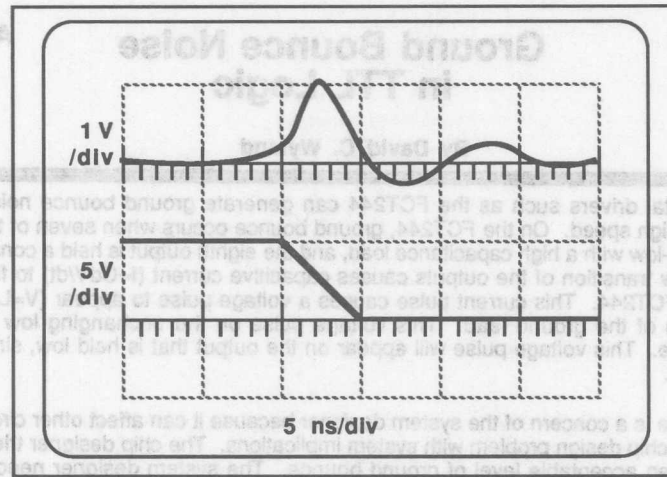


Figure 2: Ground Bounce Noise Oscilloscope Trace

Problems Caused by Ground Bounce In TTL System Designs

Ground bounce noise is a problem when it couples into other circuits or when it upsets the operation of the IC that generates it. Ground bounce noise is a problem in bus driver chips when the unswitched output is a control signal used to enable or clock other circuits. Ground bounce is not a problem in data or address bus driver circuits where all outputs switch and settle at the same time and their associated circuitry waits until the signals are settled before sampling them. Ground bounce is an indirect problem in these cases to the extent that it increases system noise and corresponding settling times in general.

Ground bounce noise is a problem only if it affects the circuits it drives. Whether driven circuits are affected is determined by the difference between the ground bounce pulse size and duration and the dynamic (AC) noise margin of the driven circuit. Dynamic noise margin is a function of the logic family of the driven circuit: i.e., LS, AS, F, HCT, etc. A plot of dynamic noise margin for various TTL logic families and showing typical ground bounce pulses is shown in Figure 3.

Ground bounce is associated with high-to-low switching in TTL designs. In the high-to-low (ground bounce) case, the unswitched output is connected directly to ground. The ground bounce spike from the internal ground is coupled directly to the output. In the low-to-high (V_{CC} bounce) case, the unswitched output is either connected directly to the internal V_{CC} in a CMOS output or buffered from V_{CC} by a source- or emitter-follower transistor in the TTL output case. In the CMOS output case, the V_{CC} bounce noise margin is $(5-1.5) = 3.5$ volts, more than twice the ground bounce margin. In the TTL output case, the source/emitter-follower buffer isolates the V_{CC} bounce from the actual output.

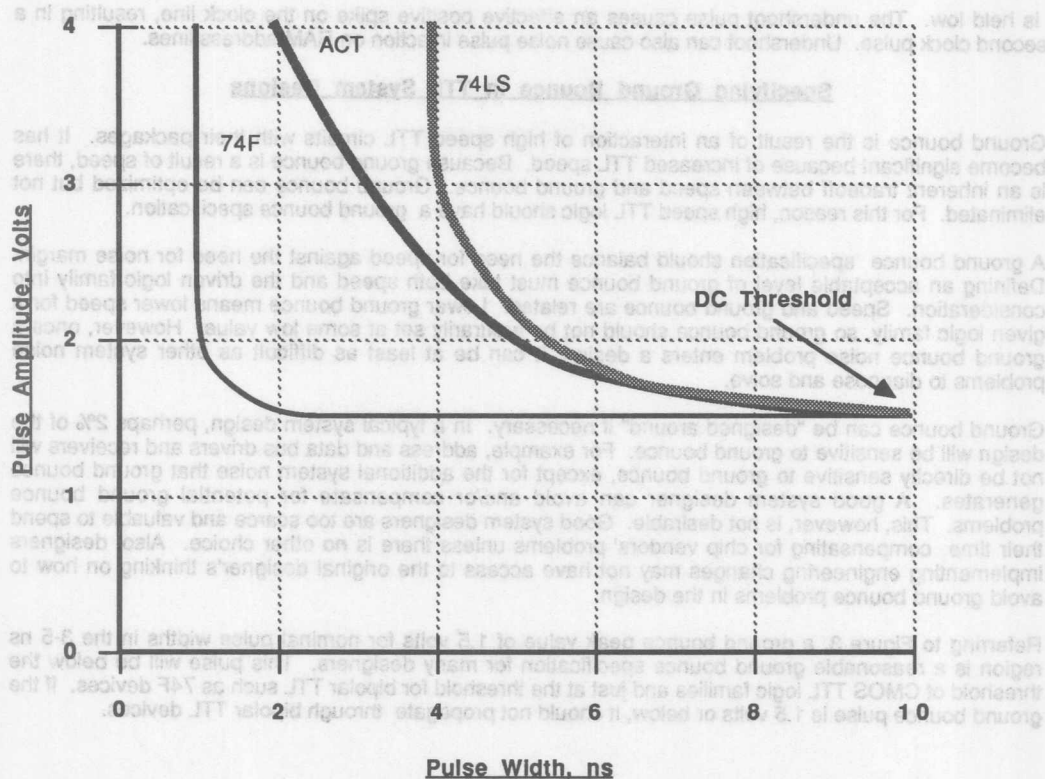


Figure 3: Dynamic Noise Margin of Various TTL Logic Families

Problems Caused by Ground Bounce In TTL Chip Designs

Ground bounce has significance for the chip as well as the system. When a ground bounce pulse is generated, the chip ground voltage is changed relative to the outside, system ground. Since the inputs to the chip are referenced to system ground, they appear to change relative to the chip ground as a result.

During the positive portion of the ground bounce pulse, the internal ground is raised. This makes the inputs appear as though they have a negative pulse added to them equal to the ground bounce pulse. If the ground bounce pulse is large enough and the driving circuit has a low V_{oh} , the high inputs would be pulsed below their thresholds. This can cause false clocking on register parts such as FCT374, etc. and false clocks and reset pulses on FIFOs such as 512x9 devices. It can also cause noise pulse injection on RAM address lines. This can result in longer access times because of disturbance of the address decoders and reactivation of the address transition detect circuitry.

After the positive portion of the ground bounce pulse, there is a negative, undershoot portion approximately equal in size to the ground bounce pulse. This makes the internal ground fall and causes logic low inputs to appear as though they have a positive pulse on them. This can cause false clocking on latch devices such as FCT373 which require their latch inputs to remain low to retain data. This undershoot pulse can also cause double clocking on registers and FIFOs during the time the clock pulse

is held low. The undershoot pulse causes an effective positive spike on the clock line, resulting in a second clock pulse. Undershoot can also cause noise pulse injection on RAM address lines.

Specifying Ground Bounce In TTL System Designs

Ground bounce is the result of an interaction of high speed TTL circuits with their packages. It has become significant because of increased TTL speed. Because ground bounce is a result of speed, there is an inherent tradeoff between speed and ground bounce. Ground bounce can be optimized but not eliminated. For this reason, high speed TTL logic should have a ground bounce specification.

A ground bounce specification should balance the need for speed against the need for noise margin. Defining an acceptable level of ground bounce must take both speed and the driven logic family into consideration. Speed and ground bounce are related. Lower ground bounce means lower speed for a given logic family, so ground bounce should not be arbitrarily set at some low value. However, once a ground bounce noise problem enters a design, it can be at least as difficult as other system noise problems to diagnose and solve.

Ground bounce can be "designed around" if necessary. In a typical system design, perhaps 2% of the design will be sensitive to ground bounce. For example, address and data bus drivers and receivers will not be directly sensitive to ground bounce, except for the additional system noise that ground bounce generates. A good system designer can avoid and/or compensate for potential ground bounce problems. This, however, is not desirable. Good system designers are too scarce and valuable to spend their time compensating for chip vendors' problems unless there is no other choice. Also, designers implementing engineering changes may not have access to the original designer's thinking on how to avoid ground bounce problems in the design.

Referring to Figure 3, a ground bounce peak value of 1.5 volts for nominal pulse widths in the 3-5 ns region is a reasonable ground bounce specification for many designers. This pulse will be below the threshold of CMOS TTL logic families and just at the threshold for bipolar TTL such as 74F devices. If the ground bounce pulse is 1.5 volts or below, it should not propagate through bipolar TTL devices.

Figure 3. Dynamic Noise Margin of Various TTL Logic Families

Problems Caused by Ground Bounce in TTL Chip Designs

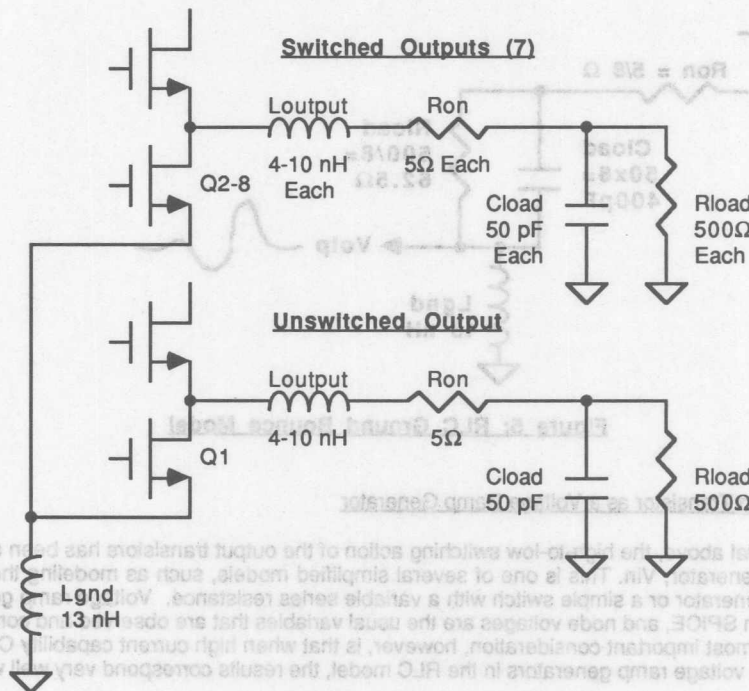
Ground bounce has significance for the chip as well as the system. When a ground bounce pulse is generated, the chip ground voltage is changed relative to the outside system ground. Since the inputs to the chip are referenced to system ground, they appear to change relative to the chip ground as a result.

During the positive portion of the ground bounce pulse, the internal ground is raised. This makes the inputs appear as though they have a negative pulse added to them equal to the ground bounce pulse. If the ground bounce pulse is large enough and the driving circuit has a low V_{OH}, the high input would be pulled below their thresholds. This can cause false clocking on register parts such as FCT37A, etc. and false clocks and reset pulses on FRCs such as 512X9 devices. It can also cause noise injection on RAM address lines. This can result in longer access times because of disturbance of the address decoders and reactivation of the address transition detect circuitry.

After the positive portion of the ground bounce pulse, there is a negative, undershoot portion approximately equal in size to the ground bounce pulse. This makes the internal ground fall and causes logic low inputs to appear as though they have a positive pulse on them. This can cause false clocking on latch devices such as FCT37B which require their latch inputs to remain low to retain data. The undershoot pulse can also cause double clocking on registers and FRCs during the clock pulse.

Ground Bounce RLC Simulation Model

Ground bounce can be modeled for SPICE analysis as shown in Figure 4. This diagram represents an octal device such as an FCT244, with 7 of 8 outputs switching high-to-low and the 8th output unswitched. Seven of the eight load capacitors have been charged to V_{oh} and are discharged through the ground lead inductance when their respective transistors switch. The eighth transistor remains on as the unswitched output.

**Figure 4: Ground Bounce Circuit**

High speed CMOS based TTL devices act like voltage ramp generators. Their output fall time does not vary appreciably over the range of 5-50 pF. If they were current sources or current limited voltage sources, one would expect the fall time to be proportional to the capacitance, at least above some value. Examining the current required to drive ground bounce in these high drive (typically above 100 mA) CMOS devices is instructive.

To verify whether the outputs are current limited during the ground bounce, consider the current built up in the ground inductance at the peak of the ground bounce pulse. This current is the integral of the ground bounce pulse divided by the inductance. If we consider the ground bounce pulse to be a half-sine wave, the inductor current at its peak is:

$$I_{peak} = (GB \text{ peak voltage}) / (1/2 \text{ GB Pulse Width (Average Value of a half-sine wave)}) \times (L_{gnd})$$

$$= 0.318 (GB \text{ peak voltage}) / (GB \text{ Pulse Width}) \times (L_{gnd})$$

$$= 0.318 (1.5) / (2.0) \times 10^{-9} = 0.159 \text{ A} = 159 \text{ mA per output for a 1.5V, 2.0 nsec pulse}$$

We are not particularly interested in the current after the voltage peak because it can cause no further increase in ground bounce. Knowing the peak current, we can calculate the maximum ground bounce

A simplified RLC model of the circuitry of Figure 4 is shown in Figure 5. In this figure, all eight outputs are assumed to be switching for maximum ground bounce. Since the load capacitors, load resistors, and lead inductances are effectively in parallel, their nominal values per pin are divided by eight. The ground inductance is in common with all, its value remains unchanged. Ground bounce appears across the ground lead inductance, L_{gnd} . The series inductances per pin have been eliminated. This is done to simplify the model. It can be done because their paralleled value is small with respect to L_{gnd} , and ignoring them will result in ground bounce values at least as bad (generally 2-5% worse) as if they were included.

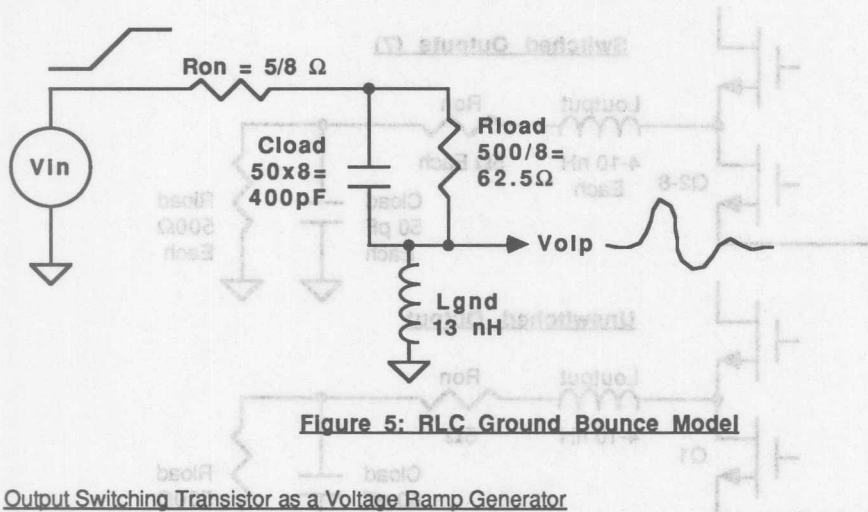


Figure 5: RLC Ground Bounce Model

Output Switching Transistor as a Voltage Ramp Generator

In the RLC model above, the high-to-low switching action of the output transistors has been replaced by a voltage ramp generator, V_{in} . This is one of several simplified models, such as modeling the switch as a current ramp generator or a simple switch with a variable series resistance. Voltage ramp generators are easy to model in SPICE, and node voltages are the usual variables that are observed and controlled by the designer. The most important consideration, however, is that when high current capability CMOS outputs are modeled as voltage ramp generators in the RLC model, the results correspond very well with observed data.

High speed CMOS based TTL devices act like voltage ramp generators. Their output fall time does not vary appreciably over the range of 5-50 pF. If they were current sources or current limited voltage sources, one would expect the fall time to be proportional to the capacitance, at least above some value. Examining the current required to drive ground bounce in these high drive (typically above 100 mA) CMOS devices is instructive.

To verify whether the outputs are current limited during the ground bounce, consider the current built up in the ground inductance at the peak of the ground bounce pulse. This current is the integral of the ground bounce pulse divided by the inductance. If we consider the ground bounce pulse to be a half-sine wave, the inductor current at its peak is:

$$\begin{aligned} I_{Vpeak} &= (GB \text{ peak voltage})(1/2 \text{ GB Pulse Width})(\text{Average Value of a half-sine wave}) / (L_{gnd}) \\ &= 0.319(GB \text{ peak voltage})(GB \text{ Pulse Width}) / (L_{gnd}) \\ &= 0.319(1.5)(5.0)/(13) = 0.184 / 8 = \underline{23 \text{ mA per output for a 1.5V, 5 ns pulse}} \end{aligned}$$

We are not particularly interested in the current after the voltage peak because it can cause no further increase in ground bounce. Knowing the peak current, we can calculate the maximum ground bounce

pulse width where the outputs can still be considered to be voltage ramp controlled. If the saturation current is given by I_O , this will be given by:

$$I_O = I_{Vpeak} = 0.319(\text{GB peak voltage})(\text{GB Pulse Width}) / (L_{\text{gnd}})$$

$$\text{GB Pulse Width} = I_O / 0.319(\text{GB peak voltage}) = 3.14 (I_O) (L_{\text{gnd}}) / \text{GB peak voltage}$$

For high speed CMOS parts such as the FCT series, the outputs are rated at 64 mA, and are typically capable of more than twice this rating in order to guarantee DC specifications over the temperature range. Using a value of 128 mA per output as the current limit and 13 nanohenries as the ground lead inductance gives the following values for the maximum ground bounce pulse width before current limit.

$$\begin{aligned} \text{GB Pulse Width} &= 3.14 (8 \times 0.128) (13) / (\text{GB peak voltage}) \\ &= 41.82 / (\text{GB peak voltage}) \\ &= 41.8 \text{ ns @ 1.0 volt peak ground bounce} \\ &= 27.8 \text{ ns @ 1.5 volts peak ground bounce} \\ &= 13.9 \text{ ns @ 3.0 volts peak ground bounce} \end{aligned}$$

These values are significantly above typical ground bounce pulse widths, which are in the 3-5 ns range. This tends to support the voltage ramp model for the high speed, high current devices used in TTL devices with significant ground bounce.

RLC Model vs Actual Waveforms

The validity of the RLC model can be determined by comparing a plot of the model output for appropriate values of R, L, C, and fall time versus results measured in the laboratory. Figure 6 shows a plot of the RLC model output using nominal values for nominal CMOS circuit resistance and fall time for an FCT244 in a 300 mil plastic DIP package. The ground bounce results shown are for all eight outputs switching; for 7 of 8 switching, the ground bounce values are multiplied by 7/8.

Figure 7 shows a plot of laboratory data recorded for a commercially available FCT244 device using the configuration of Figure 1. A high performance ground bounce test jig was used and the results recorded and plotted using a 1 GHz bandwidth sampling oscilloscope. The RLC model data in Figure 6 compares reasonably well with the recorded data in Figure 7.

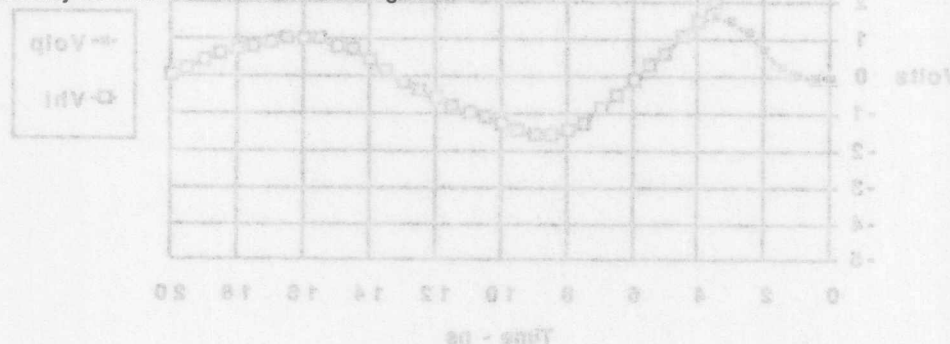


Figure 7: Measured Ground Bounce Data for FCT244

AN-01: Ground Bounce Noise in TTL Logic

pulse width where the output can still be considered to be voltage ramp controlled. If the saturation current is given by I_{sat} , this will be given by:

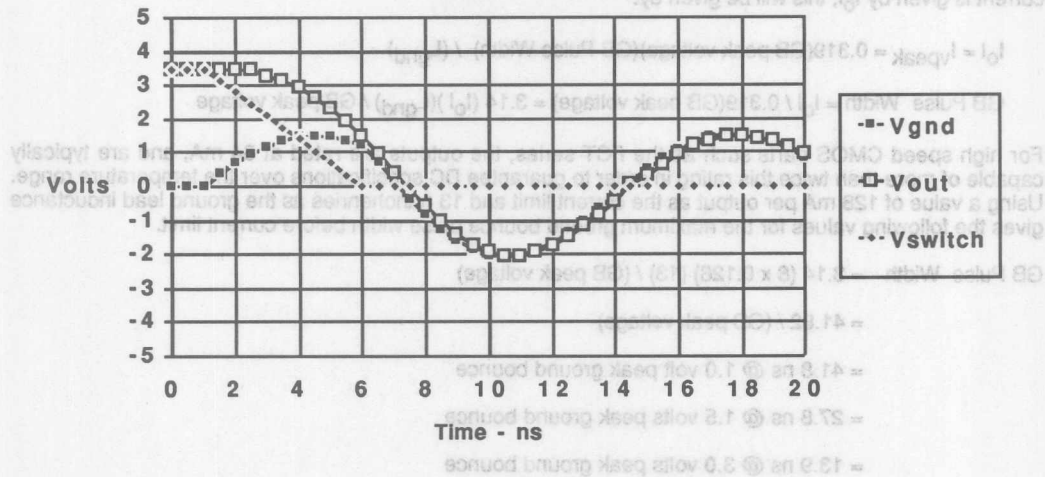


Figure 6: RLC Model Ground Bounce Waveforms

The validity of the RLC model output for appropriate values of R, L, C, and fall time results measured in the laboratory. Figure 6 shows a plot of the RLC model output for nominal CMOS circuit resistance and fall time for an FCT244 in a 300 mil classic DIP package. The ground bounce results shown are for all eight outputs switching; for 7 of 8 switching the ground bounce values are multiplied by 7/8.

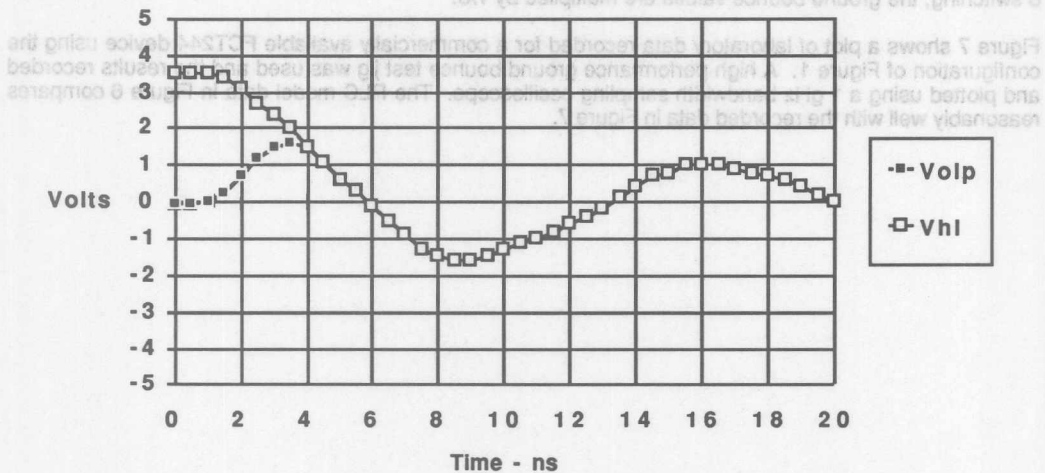


Figure 7: Measured Ground Bounce Data for QSFCT244

RLC Model Simulation Study

Using the RLC model, a simulation study was performed using various values of R, L, C, and output fall time (Tf) to reveal their effect on ground bounce and propagation delay. Given the RLC model, several useful observations can be made before simulations are begun. These are as follows.

Ground Bounce is Proportional to Voh.

Ground bounce is the result of discharging the load capacitance through the package inductance. Since the load capacitance is charged to Voh, the ground bounce will be directly proportional to Voh.

Tphl Reduces with Voh

Reducing Voh reduces the voltage swing required to reach threshold as a percentage of the total logic swing. For a given total fall time, the time to go from Voh to threshold is reduced as Voh is reduced. An extreme example would be if Voh were 1 millivolt above threshold, yielding a Tphl of nearly zero.

Ground Bounce Proportional to the Number of Outputs Switching

Ground bounce is the result of discharging the load capacitance through the package inductance. If all outputs switch, ground bounce reaches its full value. If some of the outputs switch and some are held low, there will be charge sharing between the capacitors at the beginning of the switching interval with the capacitors charged to Voh sharing charge with those that are not. After charge sharing, the effective Voh is equal to the actual Voh times the ratio of the number of outputs switching to the total number of outputs. I.e., if only half the outputs switch, the effective Voh will be half the nominal Voh.

Ground Bounce is a Non-linear Function of Tf, R, L, C

The RLC circuit forms a two pole high pass RLC filter for ground bounce. The typical fall time of the CMOS circuits of interest (3-5 ns) is similar to the RLC resonant time constant (70 mHz => 2.28 ns). Ground bounce will therefore be a function of the fall time relative to the resonant frequency as determined by R, L, and C. Changes in the resonant frequency are generally proportional to the square root (i.e., nonlinear) of changes in L and C, with R providing an additional term under the square root sign. Simple linear approximations can therefore be misleading.

Tphl has a lower limit determined by the resonant frequency of the RLC circuit

The output of the TTL device appears across the load capacitor, not across the switch. Since the load capacitor is part of a resonant circuit, its rise and fall time will be limited by the resonant frequency of the RLC circuit. The minimum fall time as seen by the load will be the time required for the capacitor to reach (Voh-Vthreshold). If the threshold is half the logic swing (Voh = 3.0 V), this will correspond to $\cos^{-1}(0.5) = 60^\circ$. The minimum propagation delay will therefore be $(60/360) * (1/70 \text{ mHz}) = 2.38 \text{ ns}$.

RLC Model Simulation Results

Ground Bounce vs Fall Time and Resonant Frequency

Figure 8 shows a plot of ground bounce voltage, V_{gb} , as a percentage of V_{oh} versus fall time as a fraction of the resonant time constant, i.e. T_f vs $1/2\pi\sqrt{LC}$. This is a plot for various values of package inductance (L), load capacitance (C) and fall time (T_f) with $R=5\Omega$ for the on resistance of the CMOS switch. Using the resonant frequency of the load capacitance and the package inductance allows the graph to be normalized for these various values.

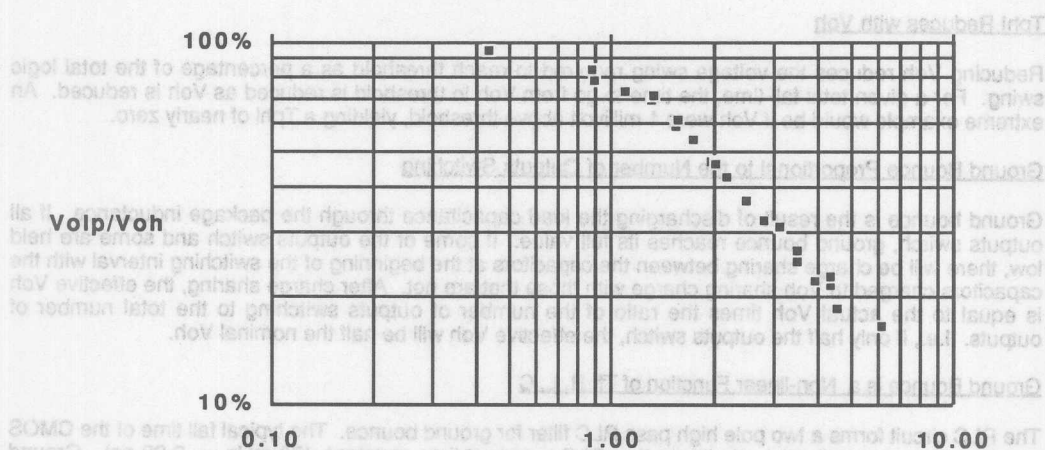


Figure 8: Ground Bounce vs Fall Time Relative to Resonant Time Constant

The plot of the data shows a high pass filter function with the ground bounce decreasing as the fall time increases. When the fall time is small relative to the resonant time constant, the ground bounce approaches V_{oh} as an asymptote.

Ground Bounce vs Package Inductance

Figure 8 is instructive as an overview, but it is more instructive to examine how we can affect ground bounce by varying specific parameters such as package inductance, etc. Figure 9 shows a plot of ground bounce versus package inductance for a fixed fall time of 5 ns and a fixed load capacitance of 50 pF per output.

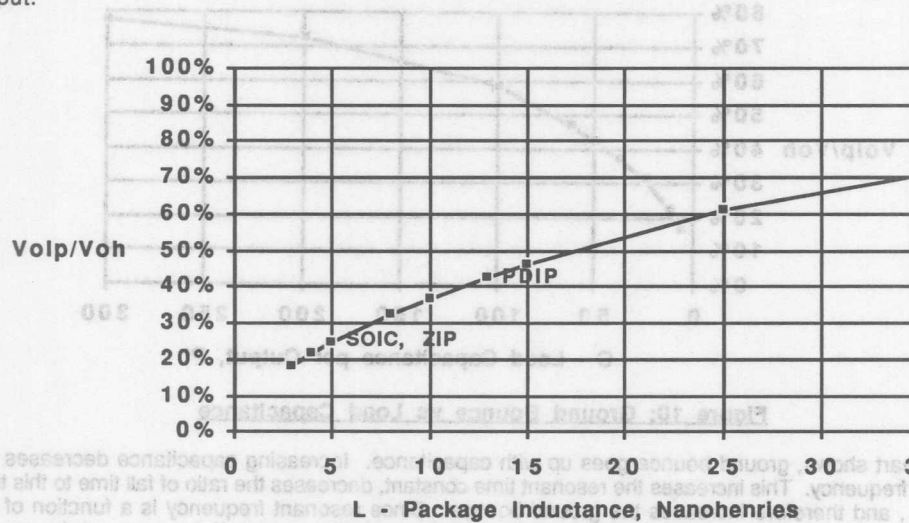


Figure 9: Ground Bounce vs Package Inductance

As the chart shows, ground bounce goes up with inductance. Increasing inductance decreases the resonant frequency. This increases the resonant time constant, decreases the ratio of fall time to this time constant, and therefore increases the ground bounce. Since resonant frequency is a function of the square root of the inductance and capacitance, cutting the inductance in half does not cut the ground bounce in half, as some simpler models show.

Ground Bounce vs Load Capacitance

Figure 10 shows a plot of ground bounce versus load capacitance for a fixed package inductance of 13 nanohenries, a fixed fall time of 5 ns, and a series resistance of 5Ω.

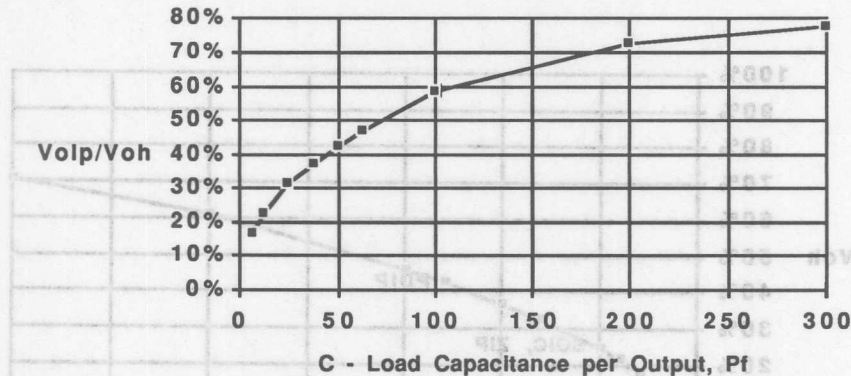


Figure 10: Ground Bounce vs Load Capacitance

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Ground Bounce vs Series Resistance

Adding series resistance will reduce ground bounce. The added series resistance increases the total impedance in the RLC current loop, reducing the current in both L and C. This causes the decrease in ground bounce. It also causes an increase in propagation delay because increasing the resistance increases the damping factor of the resonant circuit, lowering its resonant frequency. If the added resistance is less than the critical damping resistance a significant decrease in ground bounce can be traded for a small increase in propagation delay.

The following figures show the results of adding series resistance. Figure 11 shows a plot of ground bounce versus load capacitance for $L = 13$ nanohenries, $T_f = 5$ ns, and series resistances (R) of 5Ω and 25Ω . Figure 12 shows a plot of relative ground bounce reduction versus series resistance.

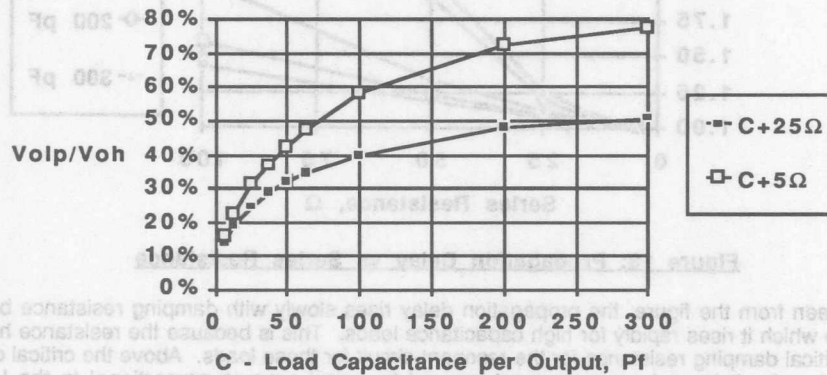


Figure 11: Ground Bounce vs Load Capacitance with Series Resistance

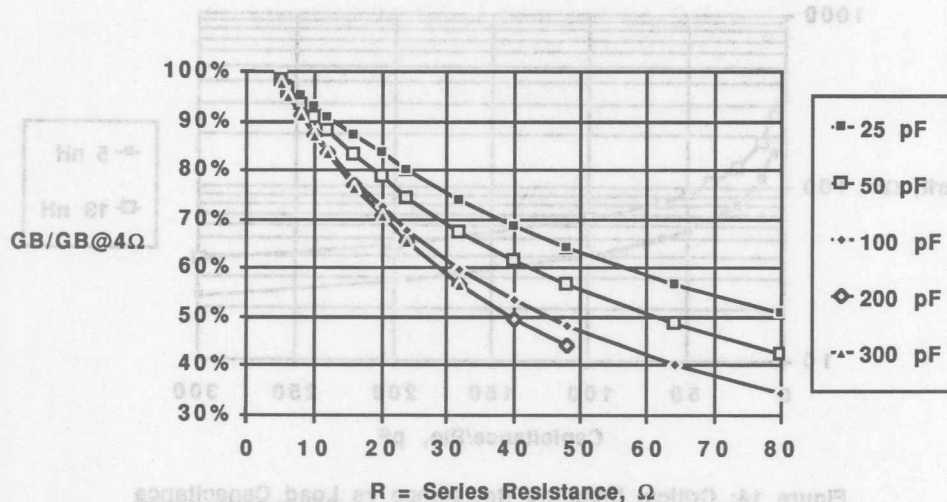


Figure 12: Ground Bounce vs Series Resistance

Figure 13 shows a plot of propagation delay versus series resistance for various values of capacitance and for $L = 13$ nanohenries and $T_f = 5$ ns. This is a minimum propagation delay and is the delay associated with the resonant RLC circuit, as derived from the simulations.

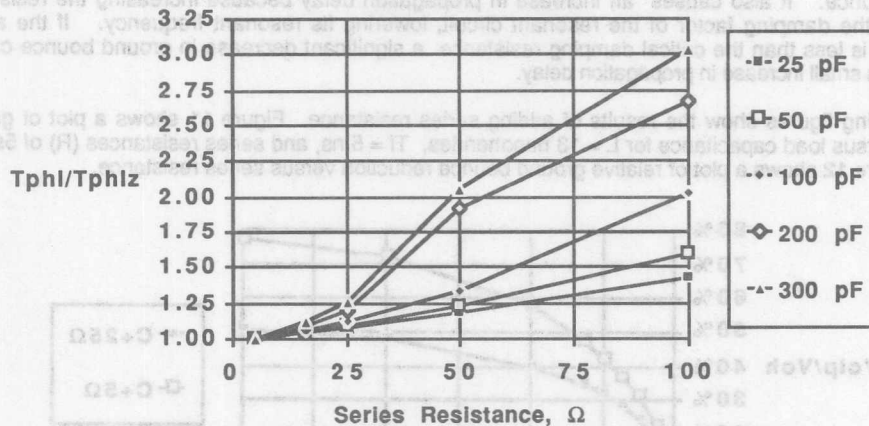


Figure 13: Propagation Delay vs Series Resistance

As can be seen from the figure, the propagation delay rises slowly with damping resistance below 50 ohms, above which it rises rapidly for high capacitance loads. This is because the resistance has risen above the critical damping resistance for the resonant circuit for these loads. Above the critical damping resistance, the circuit is no longer resonant, ground bounce becomes proportional to the L/R time constant and propagation delay becomes proportional to the RC time constant. To determine this point, Figure 14 shows a plot of critical damping resistance versus load capacitance.

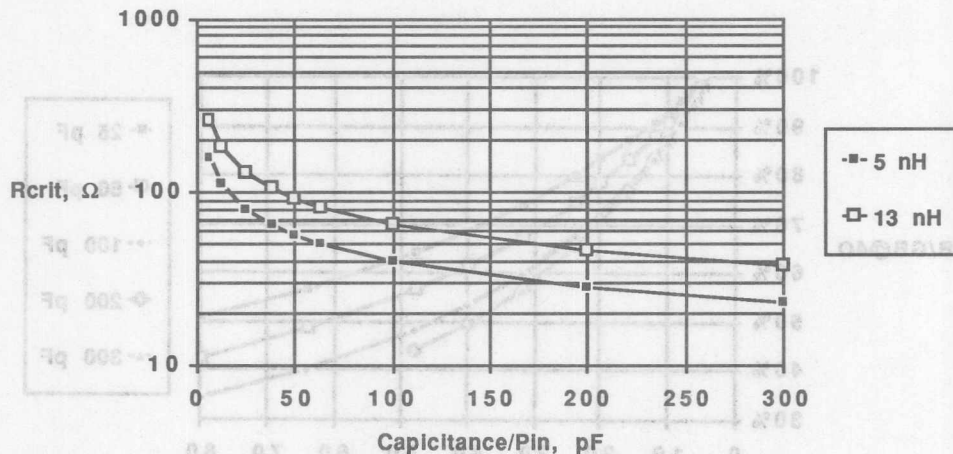


Figure 14: Critical Damping Resistance vs Load Capacitance

Propagation Delay vs Ground Bounce

Given the above data, we can plot propagation delay versus ground bounce. Figure 15 shows such a plot for the case of $V_{oh} = 3.5$ volts, $L = 13$ nanohenries and $C = 50$ pF/pin. In this figure, the main curve plots a relationship between ground bounce and propagation delay for various combinations of fall time (T_f) and series resistance (R).

Note that below the critical damping resistance of 91Ω for 50 pF & 13 nH, either series resistance or fall time can be used to trade ground bounce for propagation delay.

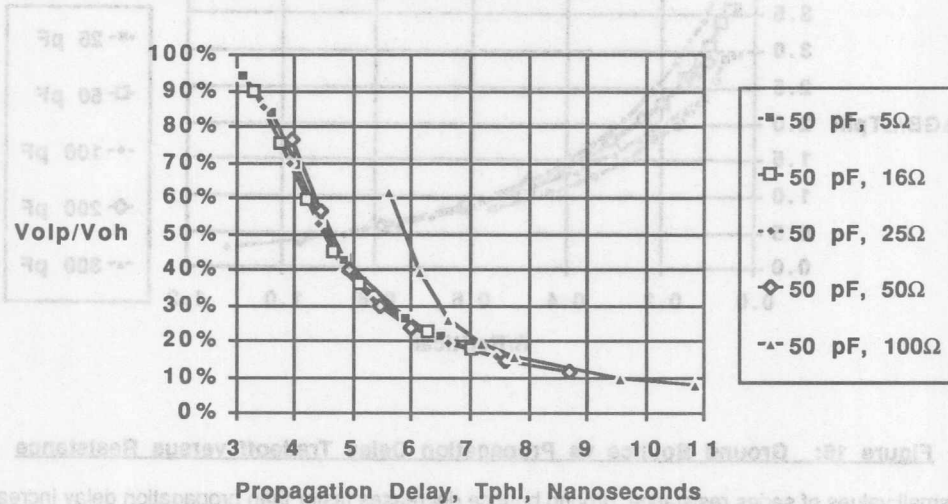


Figure 15: Propagation Delay vs Ground Bounce

We can use the above data to show the tradeoff of ground bounce versus propagation delay as a function of the series resistance. The curves of Figure 16 plot the slope of the ground bounce versus propagation delay curve; i.e. the percent decrease in ground bounce divided by the percent increase in propagation delay as a function of series resistance relative to the critical damping resistance.

Ground Bounce vs Tphl Tradeoff vs R

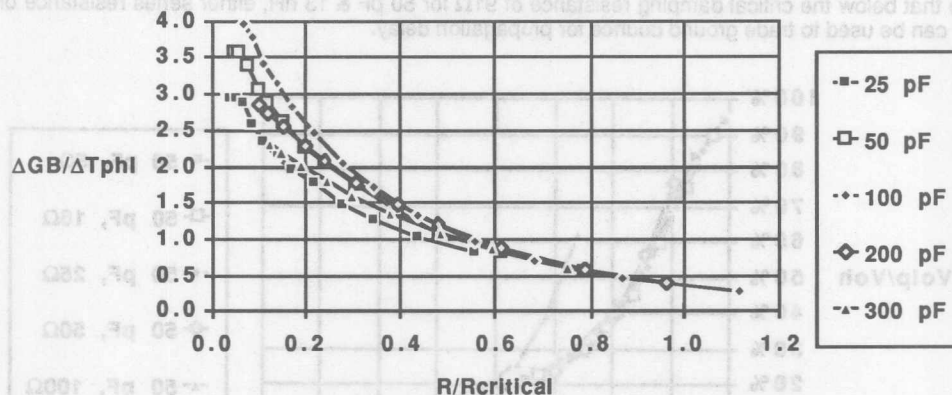


Figure 16: Ground Bounce vs Propagation Delay Tradeoff versus Resistance

For small values of series resistance, ground bounce decreases faster than propagation delay increases. For values in the 5-10Ω range at 50 pF loading, a 1% increase in propagation delay can be traded for a 3.5% decrease in ground bounce. One-half the critical damping resistance is the break-even point. For resistance values above this value, propagation delay increases relatively faster than ground bounce decreases. This implies that the series resistance should be less than half the critical damping resistance for the largest expected capacitive load.

Propagation Delay and Ground Bounce vs Voh

Propagation delay increases with Voh because the output must travel a larger voltage difference between Voh and the TTL threshold. Ground bounce is directly proportional to Voh. This is shown in the plot of ground bounce versus high-to-low propagation delay for three values of Voh shown in Figure 17. The plot in Figure 16 is for L = 13 nanohenries, C = 50 pF/pin, and various values of Tf.

Note that the high-to-low propagation represents the minimum delay associated with the RLC resonant circuit. Propagation delay for other circuitry must be added to this for actual delays.

Propagation delay for other values of L and C for a given ground bounce can be calculated using this chart and multiplying the Tphl value by the square root of the ratio of L or C to 13 nH and 50 pF, respectively.

Volp vs Tphl for 13 nH (PDIP) and 50 pF/pin Load

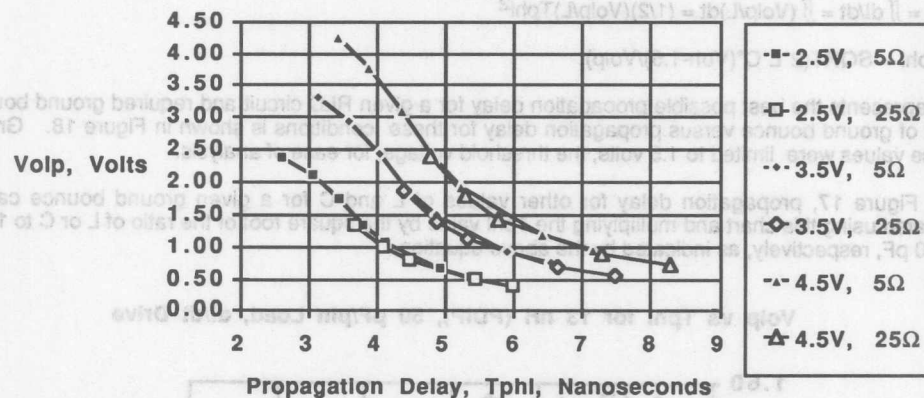


Figure 17: Ground Bounce vs Propagation Delay and Voh

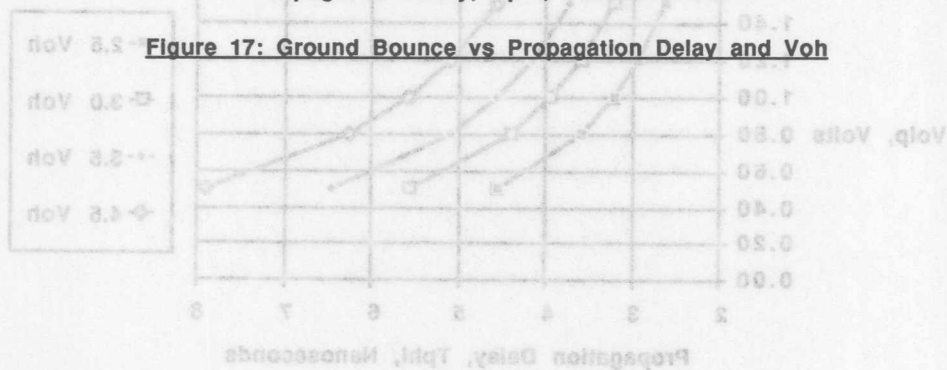


Figure 18: Ground Bounce vs Tphl and Voh for Ground Bounce Determined dthl

Propagation Delay and Ground Bounce for Shaped Drive Pulses

Propagation delay for a given ground bounce can be improved if a shaped drive pulse other than a linear ramp is used. Propagation delay is determined by the rate of voltage build up on the load capacitor, which is determined by the rate of current build up in the ground inductor. To improve the propagation delay, you increase the ramp rate of current in the inductor.

The maximum possible current ramp rate in the inductor is determined by the inductance and the ground bounce by the rule $V = L di/dt$. This could be achieved by using a current ramp instead of a voltage ramp and adjusting the ramp rate for the allowed ground bounce. The current ramp is adjusted so that the ground bounce pulse rises immediately to the desired ground bounce value and stays there until the output has achieved the high-to-low transition.

The propagation delay time for a current ramp equal to V_{olp}/L is determined by the capacitance and the difference between V_{oh} and the 1.5 volt TTL threshold by the relationship:

$$V = (V_{oh} - 1.5) = Q/C$$

$$Q = \int di/dt = \int (V_{olp}/L) dt = (1/2)(V_{olp}/L) T_{phl}^2$$

$$T_{phl} = \sqrt{2 \cdot L \cdot C \cdot (V_{oh} - 1.5) / V_{olp}}$$

This represents the best possible propagation delay for a given RLC circuit and required ground bounce. A plot of ground bounce versus propagation delay for these conditions is shown in Figure 18. Ground bounce values were limited to 1.5 volts, the threshold voltage, for ease of analysis.

As in Figure 17, propagation delay for other values of L and C for a given ground bounce can be calculated using this chart and multiplying the T_{phl} value by the square root of the ratio of L or C to 13 nH and 50 pF, respectively, as indicated by the above equation.

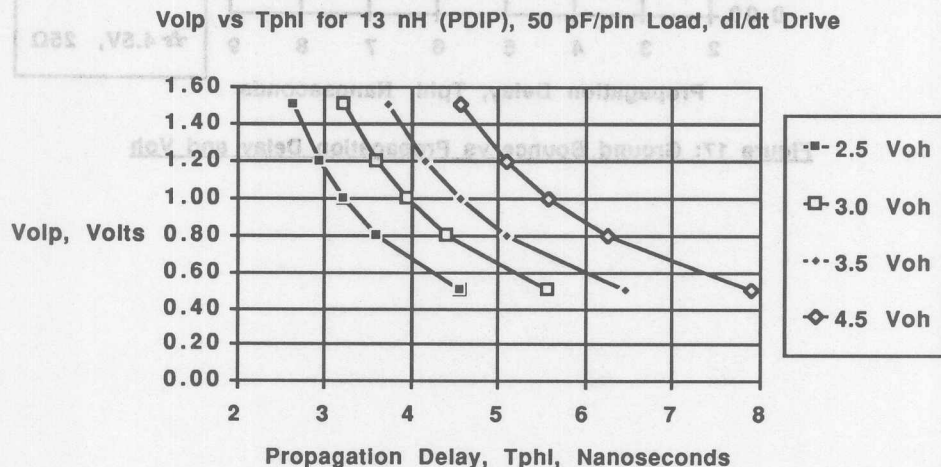


Figure 18: Ground Bounce vs T_{phl} and V_{oh} for Ground Bounce Determined di/dt



FIFOs as High-Speed Data Queues for Systems

Application
Note
AN-02

by
Suneel Rajpal

Introduction

A FIFO is a queue for data. FIFO means First-In-First-Out, the definition of a queue. FIFOs are used to queue data between parts of a system that generate and receive data at different rates and times. For example, to read data from a disk, you must be able to accept the data as it passes under the read head. This means accepting data on demand, usually at a high rate, for transfer to main memory at a more moderate rate when the main memory is ready to accept it. Unique design features and a variety of applications of FIFO integrated circuits will be discussed in this application note.

What is a FIFO ?

A short definition of a FIFO is as a queue for data. Queues are observed in everyday life in toll stations and airline check-in counters. In computer applications a data queue is required when data must be transferred between parts of a system which operate at different data rates. Often data is generated (or required) in bursts faster than it can be absorbed (or generated). The FIFO provides a temporary holding area for data to service these data bursts.

FIFOs are specially designed integrated circuits. They are designed as the hardware equivalent of the circular buffer concept used in software. They consist of a special, dual-port memory that can be read and written at the same time, and address counters for reading and writing. The counters treat the memory as though it were circular: location zero immediately follows after the last location in memory. When a counter has reached the last word in the memory, the next increment takes it to the first word.

In the circular buffer concept, data is written at the address selected by the write counter, and the counter is incremented after the write. After data is written, data is read separately from the address selected by the read counter, which is incremented after the read. The read counter thus follows the write counter continuously around the memory. If the read counter catches up to the write counter, the FIFO is said to be empty. If the write counter catches up to the read counter, the FIFO is said to be full. These full and empty conditions are detected by the flag logic, which compares the contents of the two counters.

A block diagram of the QSI FIFO family is shown in Figure 1. The FIFO devices have separate read and write pointers that are clocked by the respective read and write signals. Flag indicators such as full, empty, and half full are also provided.

FIFOs have widths and depths similar to RAM memories. Width is the number of bits per word. Depth is the size of the circular memory in words, usually a binary multiple such as 512 words, etc. QS FIFOs are available in 512x9, 1Kx9, 2Kx9, 4Kx9. The part numbers are QS8201, QS8202, QS8203, QS8204 respectively. Two or more FIFOs can be combined to increase the effective width of the FIFO. This is simple; the FIFOs are operated in parallel, and no interaction is needed between the FIFOs.

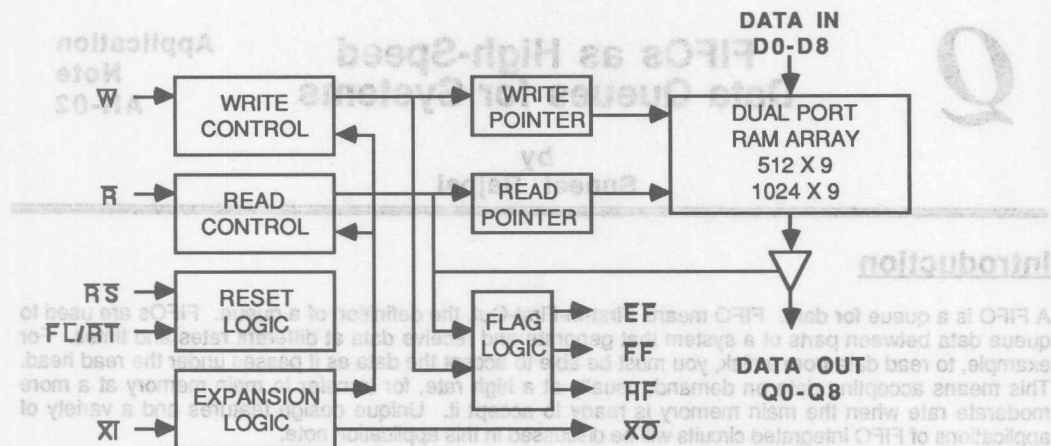


Figure 1. FIFO Block Diagram

Two or more FIFOs can be combined to increase the effective depth of a FIFO. This is called depth expansion. This requires using additional logic to pass data between the FIFOs. QSI FIFOs contain logic to provide depth expansion without additional logic or speed penalties. Depth expansion of QSI FIFOs is done by using the expansion in and expansion out signals.

FIFOs must be initialized before use because the read and write counters can come up with random values at power-up. This is done by a reset operation. A pulse on the reset (RS) pin clears both counters to feature zero, making the FIFO empty. QSI FIFOs also provide a partial reset called retransmit. A pulse on the retransmit input resets the read pointer to zero. Retransmit allows data written into the FIFO to be re-read. One application is in communications, where data may need to be retransmitted because of an error in the first transmission.

FIFOs designed using a dual port RAM with read and write address counters are said to be pointer based, to differentiate them from earlier FIFOs based on different principles. Pointer-based FIFOs have the advantage of zero fall through time, the time required to receive an output from an initially empty FIFO after the first write operation.

Figure 2 shows a diagram of the FIFO as a circular queue with two pointers. After power up both read and write pointers are reset to zero. After that, upon write operations, the write pointer is incremented. The numbers outside the circle indicate the values the pointers can have. For example the write pointer increments from 0 to 1023 and then wraps to 1024 on the next write. The shaded area indicates the number of words in the FIFO. When a read operation is performed, the read pointer is incremented. When the read pointer equals the write pointer after the completion of a read operation, the FIFO is empty. If the write pointer equals the read pointer after the completion of a write operation, then the FIFO is full. When the FIFO contains more words than half its depth, the half full flag is asserted.



6

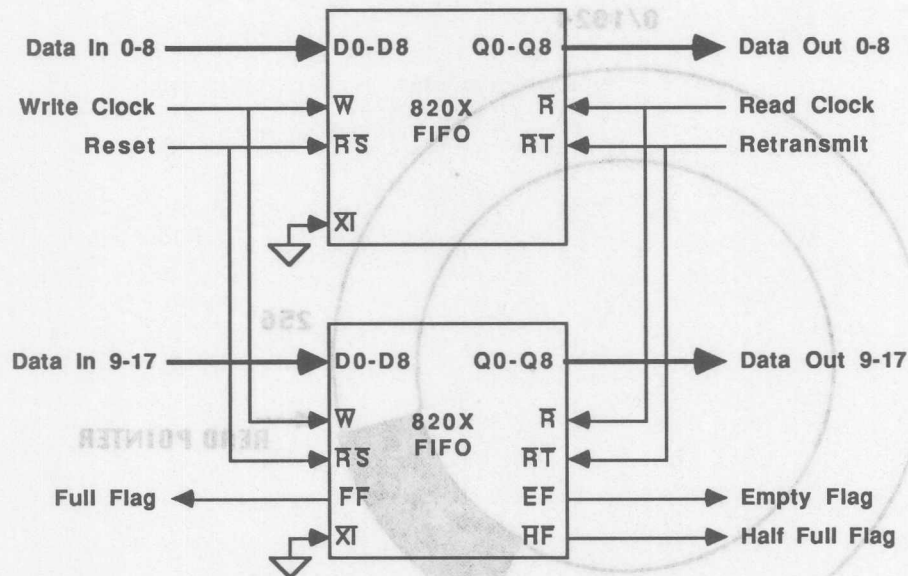


Figure 3: Width Expansion - An 18-bit FIFO From Two 9-bit FIFOs

Depth Expansion

FIFOs can be expanded in depth fairly easily. As FIFOs do not have chip selects, another mechanism must be used to identify the first FIFO that will be written to or read from. The **FL** or first load signal indicates which FIFO will receive the first N words or transmit the first N words after a reset operation where N is the depth of a single FIFO. Figure 4 shows FIFOs in a depth expansion mode. One FIFO in the array has its **FL** line grounded and the other FIFOs have their **FL** line at **Vcc**. The expansion output of one FIFO is connected to the expansion in of the other FIFO and so on until the expansion out of the last FIFO is connected to the expansion in of the first FIFO. It is good system practice to layout the FIFOs so that the trace length of the expansion out of the last FIFO is connected to the expansion in of the first FIFO. It should be kept small to minimize crosstalk effects.

DEPTH EXPANSION

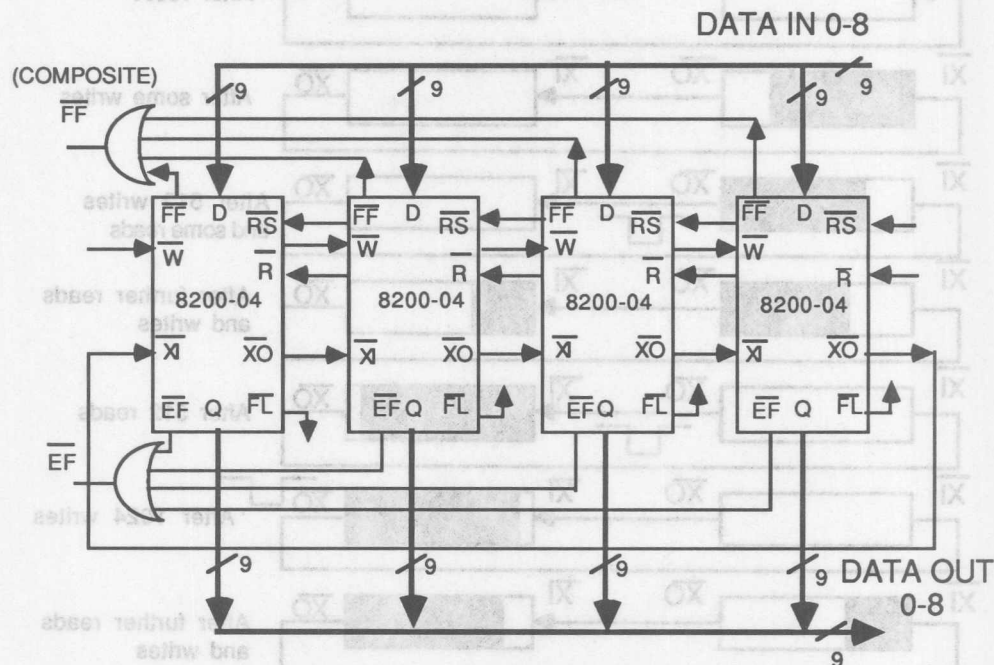


Figure 4. Building a 4-N deep FIFO out of an N-deep FIFO

6

The FIFO operates elegantly in depth expansion. After a reset operation the FIFO with the FL grounded receives the first N words. On the writing on the N th word a pulse is sent on the $\overline{XO}$ output to the input of the next FIFO. The $N+1$ th word is written into the next FIFO. Similarly the first N reads take place in the first FIFO. On the N th read a pulse is sent from the $\overline{XO}$ output to the input of the next FIFO. This allows the $N+1$ th word to be read from the next FIFO. Similarly when the $2N$ words are written the $2N+1$ th write takes place in the third FIFO. Finally when the control is transferred to the last FIFO in the queue and it too reaches its boundary, the write control is passed back to the first FIFO. This is shown for a configuration with two FIFOs in Figure 5. Some external logic, (namely OR gates) is required to combine the individual empty flags to give a composite empty flag, and the individual full flags to give a composite full flag.

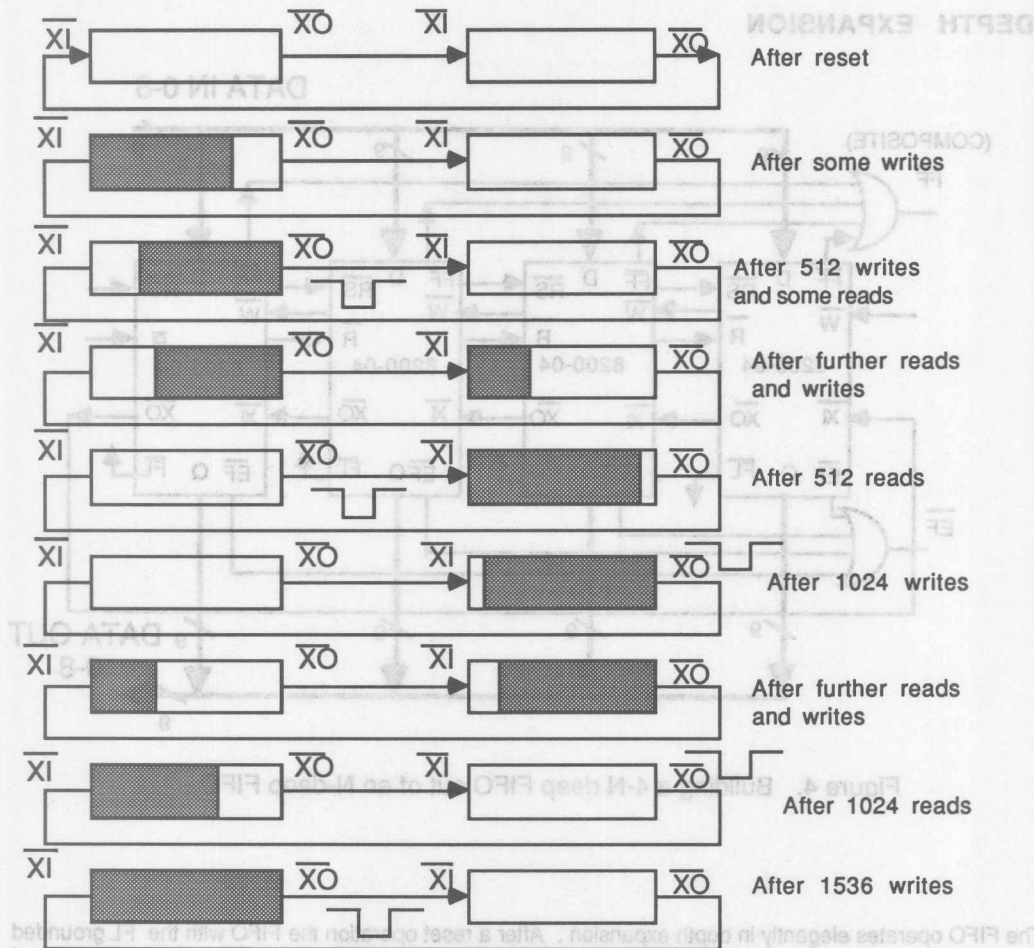
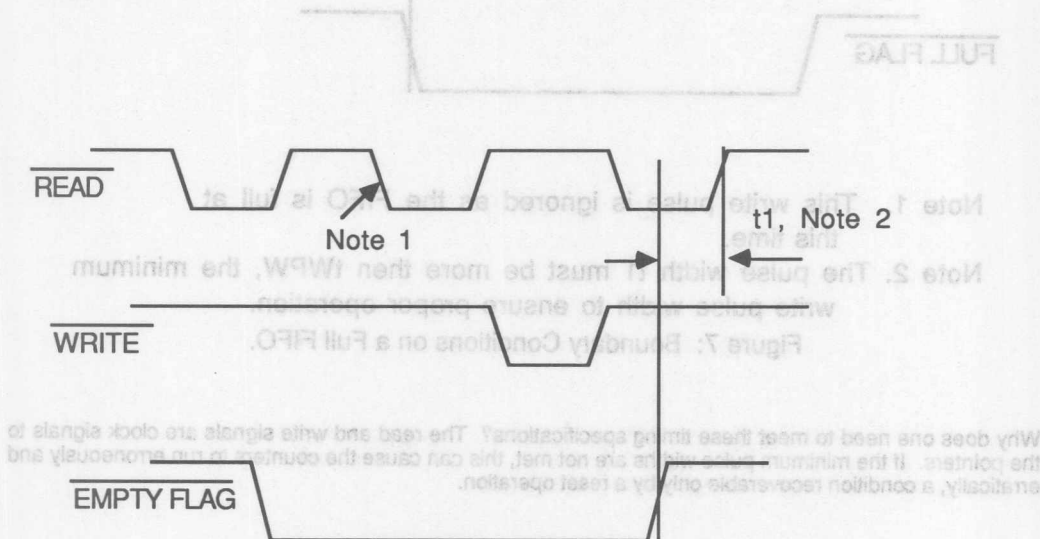


Figure 5. The Expansion Signals for a 1Kx9 FIFO using two 512x9 FIFOs.

Operating on Boundary Conditions

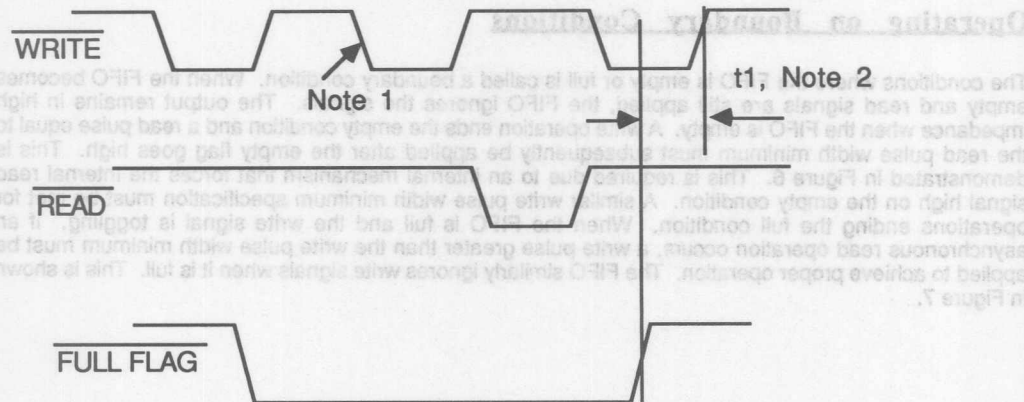
The conditions where the FIFO is empty or full is called a boundary condition. When the FIFO becomes empty and read signals are still applied, the FIFO ignores the signals. The output remains in high impedance when the FIFO is empty. A write operation ends the empty condition and a read pulse equal to the read pulse width minimum must subsequently be applied after the empty flag goes high. This is demonstrated in Figure 6. This is required due to an internal mechanism that forces the internal read signal high on the empty condition. A similar write pulse width minimum specification must be met for operations ending the full condition. When the FIFO is full and the write signal is toggling, if an asynchronous read operation occurs, a write pulse greater than the write pulse width minimum must be applied to achieve proper operation. The FIFO similarly ignores write signals when it is full. This is shown in Figure 7.



Note 1. This read pulse is ignored as the FIFO is empty at this time.

Note 2. The pulse width t_1 must be more than t_{RPW} , the minimum read pulse width to ensure proper operation.

Figure 6. Boundary Condition on an Empty FIFO.



Note 1. This write pulse is ignored as the FIFO is full at this time.

Note 2. The pulse width t_1 must be more than t_{WPW} , the minimum write pulse width to ensure proper operation.

Figure 7: Boundary Conditions on a Full FIFO.

Why does one need to meet these timing specifications? The read and write signals are clock signals to the pointers. If the minimum pulse widths are not met, this can cause the counters to run erroneously and erratically, a condition recoverable only by a reset operation.

FIFO Applications

DMA Operations

FIFOs can be used as part of DMA controllers. In DMA operations, data is accessed from a slower peripheral bus and transferred to a memory location. In certain applications, a DMA controller may have to acquire two buses, one on which the memory resides and the second on which the peripheral resides and then perform the transfer. If a slower peripheral is on one of the buses it can reduce the performance of the second bus where the faster memory resides due to a higher bus utilization rate during DMA transfers.

One way to improve the performance is to have the FIFO interface to the peripheral device and transfer data from the peripheral at the peripheral's frequency in a burst manner. The output of the FIFO can interface to the system bus at higher speeds via transceivers. Since the FIFO can be clocked at a higher frequency than its input frequency, the external bus utilization rate can be reduced. For example, if a block of 1K words has to be transferred, the peripheral can transfer the data to the FIFO. The FIFO can signal to the DMA controller that it has 512 or 1K words of data via the half-full or full flag. Then the FIFO is read in a burst manner. In this mode of operation, the faster memory bus is not acquired until the peripheral has finished or almost finished transferring its data. A FIFO can be used for the peripheral write operations as well, which creates a need for bidirectional FIFOs as shown in Figure 8.

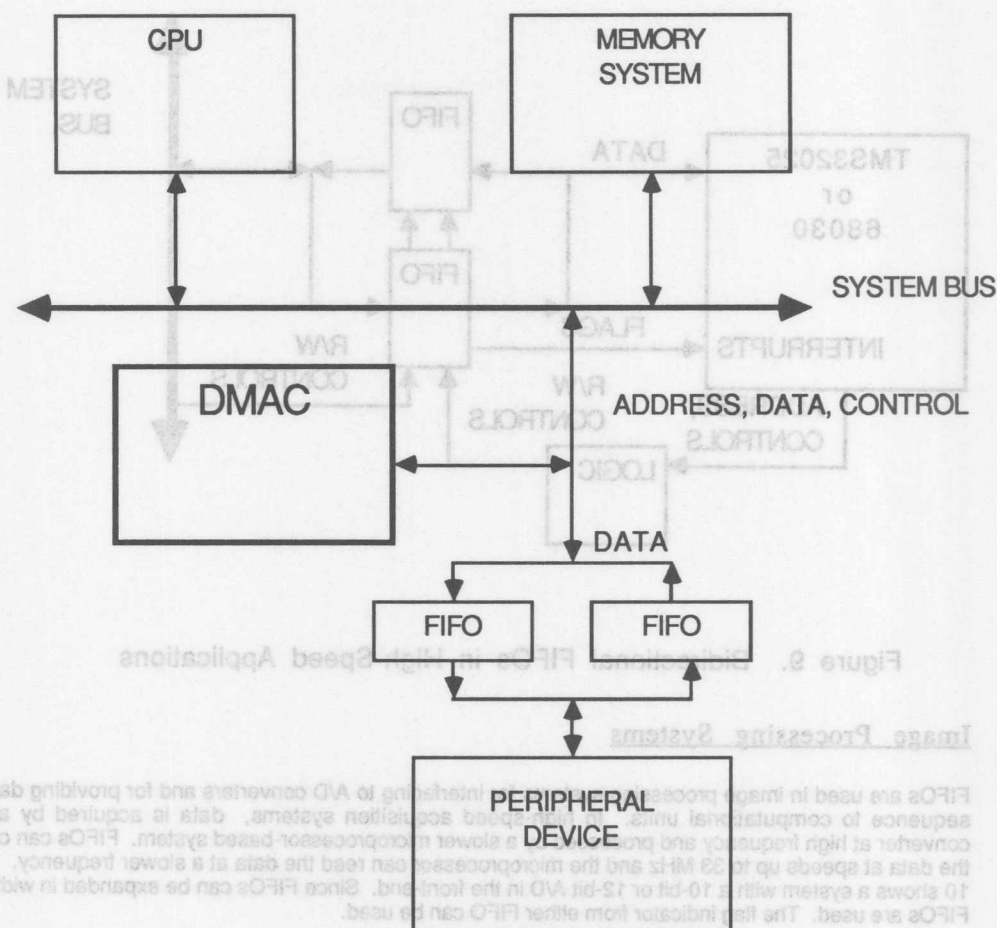


Figure 8. Using the FIFO with a High-speed CPU, DMA Controller and a Slow Peripheral

Bidirectional FIFOs also have applications for interfacing between the CPU local bus and an external system bus. The high speed access times of 20 ns and a data set up time of 10 ns in 20 ns speed -grade FIFOs make them ideally suited for high-performance DSP devices such as the TI 32025, as shown in Figure 9. Different speed grades (25 ns, 35 ns, 50 ns, 80 ns and 120 ns) are also available.

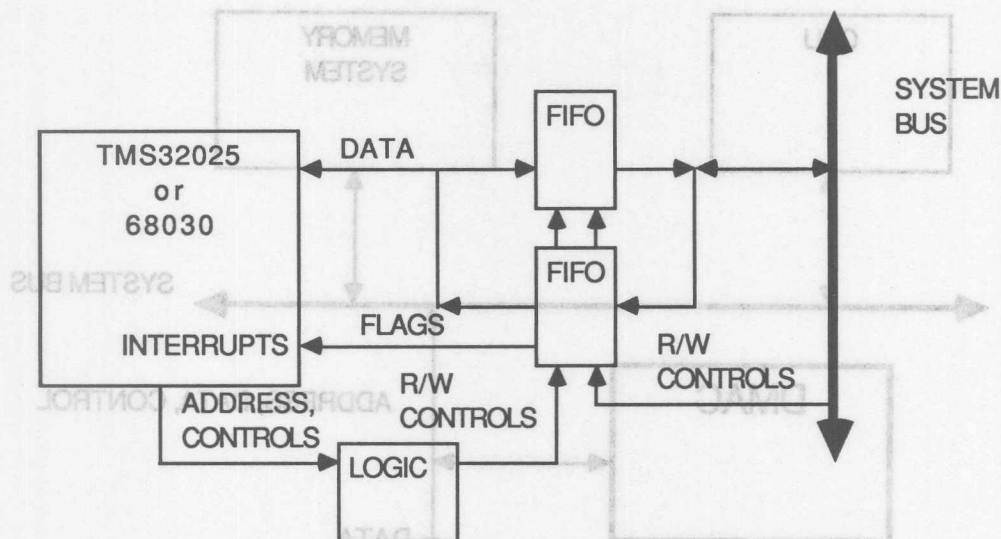


Figure 9. Bidirectional FIFOs in High-Speed Applications

Image Processing Systems

FIFOs are used in image processing systems for interfacing to A/D converters and for providing data in a sequence to computational units. In high-speed acquisition systems, data is acquired by an A/D converter at high frequency and processed by a slower microprocessor-based system. FIFOs can capture the data at speeds up to 33 MHz and the microprocessor can read the data at a slower frequency. Figure 10 shows a system with a 10-bit or 12-bit A/D in the front-end. Since FIFOs can be expanded in width, two FIFOs are used. The flag indicator from either FIFO can be used.

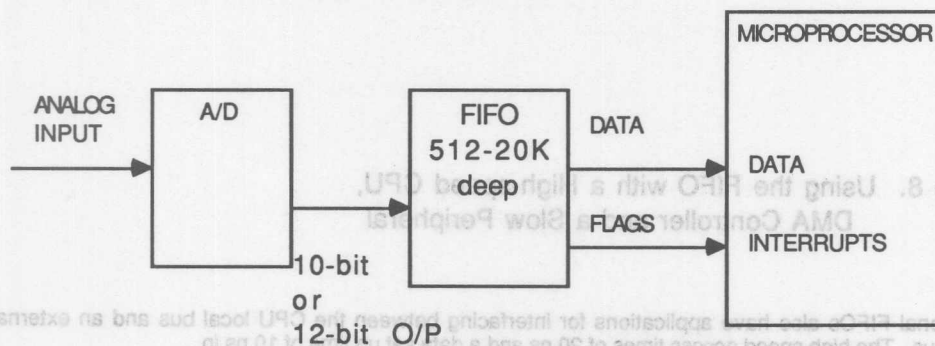
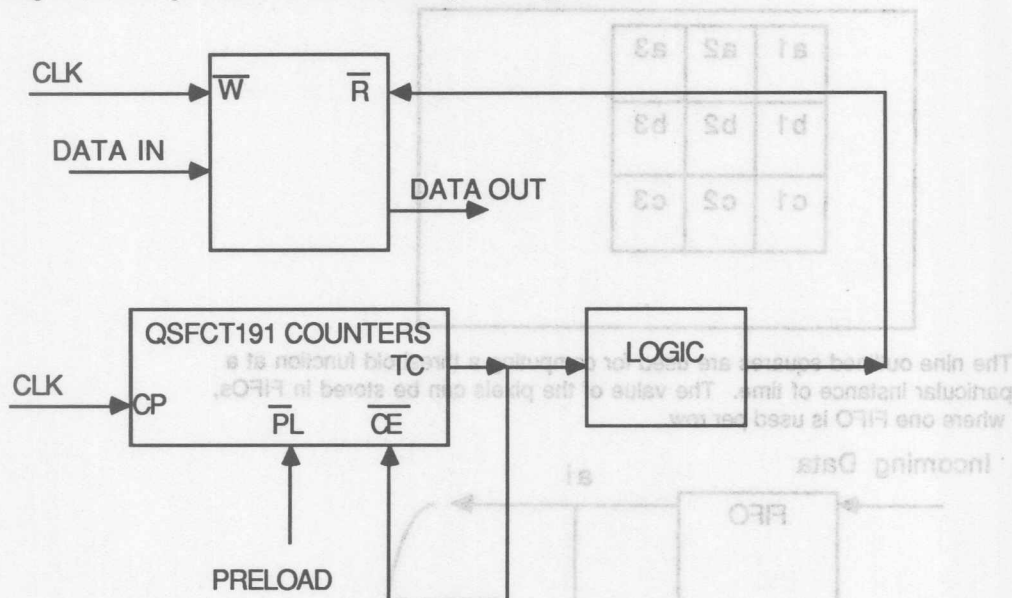


Figure 10. FIFOs in Data Acquisition Systems

FIFOs with minimal logic can create fixed-length delay times. For example, if you need a delay line of 1178 time slots, you can program a counter with 1178 and decrement it with each write clock edge. After the

count is zeroed, the read clock is enabled by the write clock signal. This allows a programmable delay and the system has reads and writes off the same clock. The schematic shown in Figure 11 is a conceptual diagram; more logic must be added depending on the application.



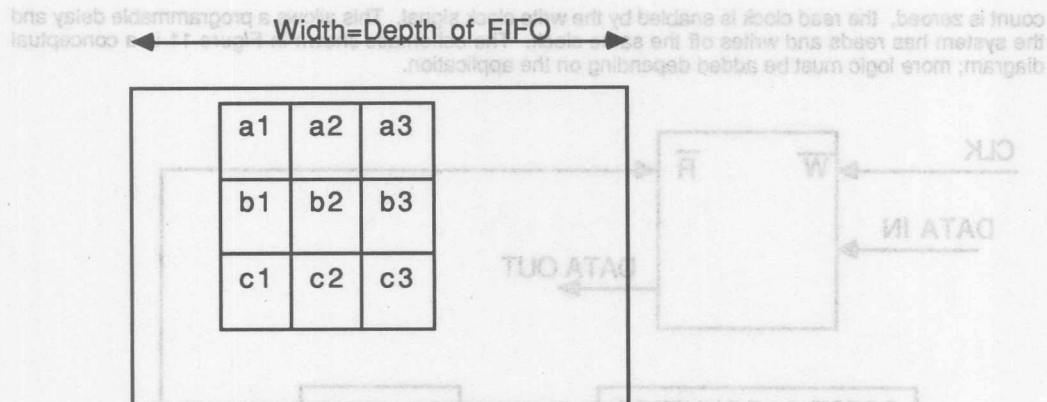
The TC can be ANDed with the CLK signal to create the Read signal to the FIFO or the read logic can be user defined.

Figure 11. A Programmable Delay Using FIFOs

FIFOs configured in the above manner can be combined with similarly configured FIFOs in image processing applications. A screen of data is shown in Figure 12. A typical operation may be the computation of a threshold function in which a matrix multiply of a 3x3 pixel arrangement with another matrix may be required. Assume that each row of the screen can be stored in a FIFO. If the row is not representable as a power of 2, counters can be added to create fixed-length delay lines to create the appropriate screen width. In a typical application, a screen width of 1024 pixels c_1, c_2, c_3 are received at a certain time. Pixels b_1, b_2, b_3 are received 1024 time delays later, and pixels a_1, a_2, a_3 are received yet another 1024 time delays later. The rows of the screen can be stored in three FIFO as shown in Figure 12. The outputs of these FIFO can be connected to numbercrunching elements to compute the required matrix multiply operation.

FIFO Retransmit Applications in Data Communications

The FIFO retransmit pin enables resetting the read pointer to zero without affecting the write pointer. The retransmit feature can be used in data communication applications where data is transmitted but an error was detected externally and the packet of data must be retransmitted. This can be done by asserting the retransmit signal and by sending the packet of data all over again. The retransmit feature is executed as follows: the FIFO is reset; the number of words written in the FIFO are less than the depth of the FIFO; the words are read and can be re-read as shown in the first level of Figure 13. If subsequent writes occur and the write pointer wraps around the zero mark, if the retransmit signal is then asserted, the user will only get the words from pointer location zero to the location of the write pointer. This is shown in the lower level of Figure 13.



The nine outlined squares are used for computing a threshold function at a particular instance of time. The value of the pixels can be stored in FIFOs, where one FIFO is used per row.

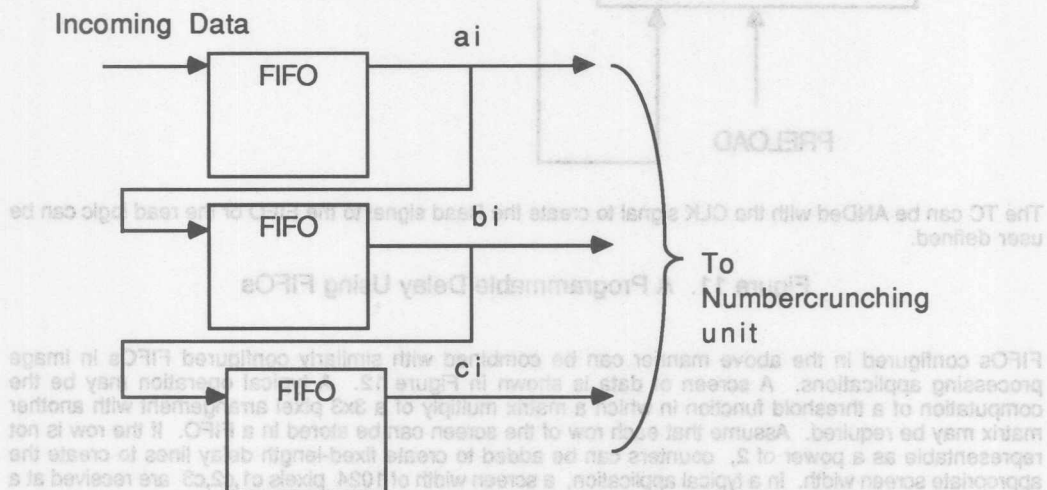
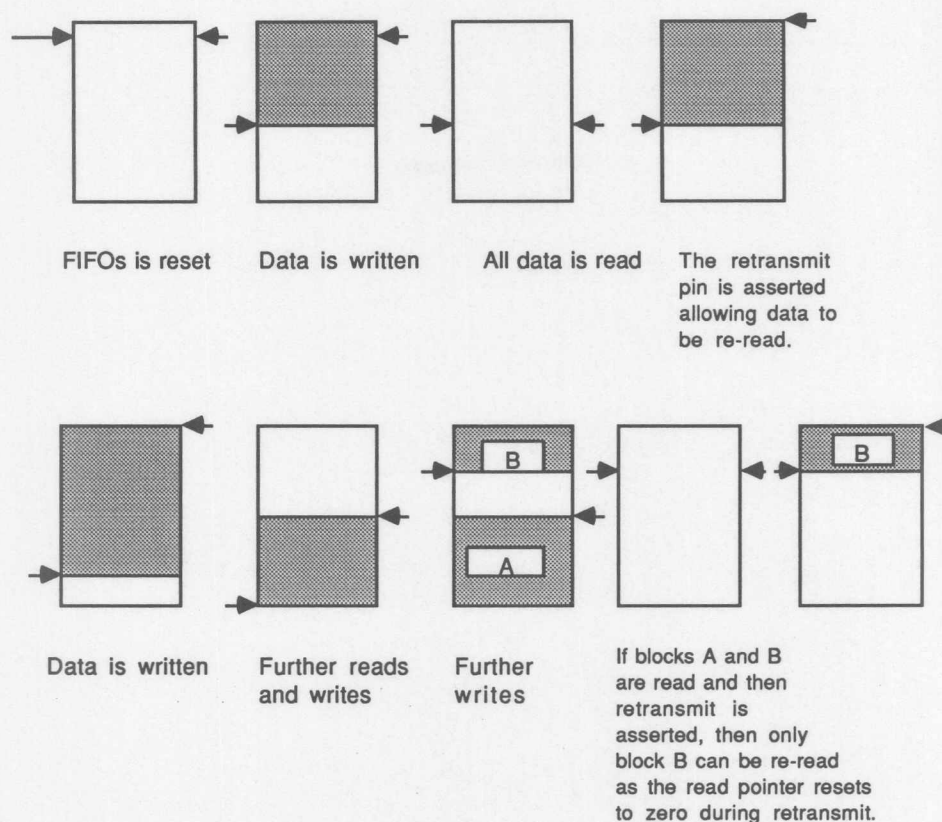


Figure 12. FIFOs in Image Processing Systems

FIFO Retransmit Applications in Data Communications

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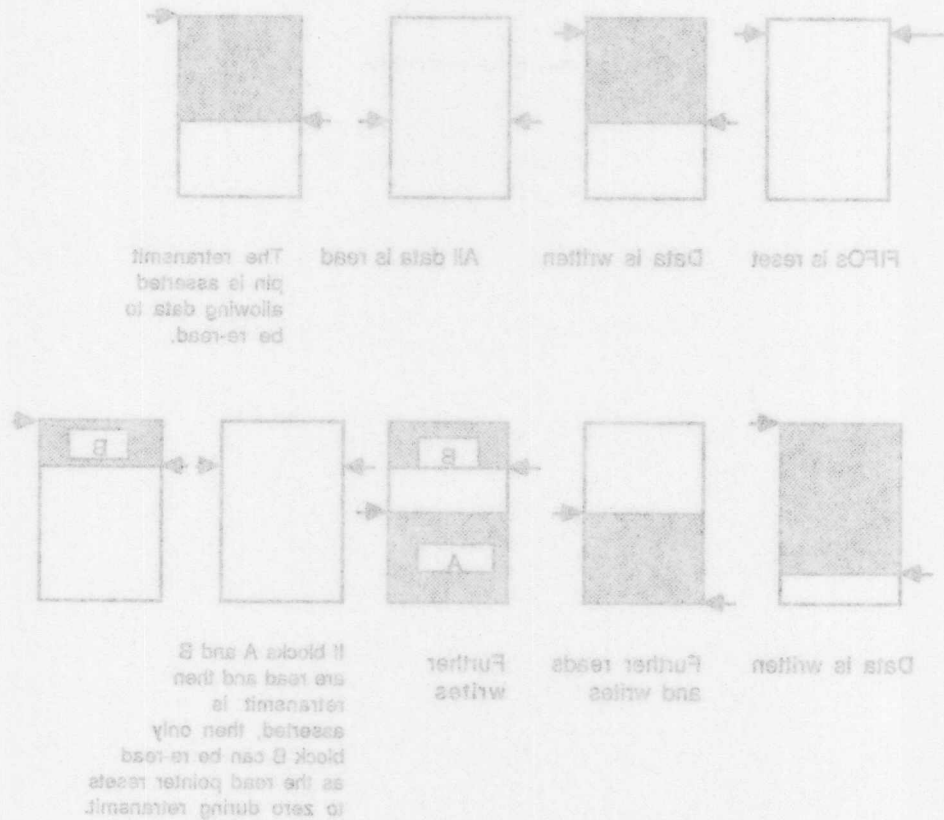


Note: The arrows on the left side indicate the write pointer and the ones on the right indicate the read pointer. The upper level diagrams are a normal retransmit and the lower level indicate a limitation of the retransmit operation.

Figure 13. Retransmit Operations

Conclusion

FIFOs are useful as data queues to match data rates in computer systems. With cycle times of 25 nsec, newer applications are available in graphics and DSP systems and in data communication systems. With fast flag access times, external timings are relaxed by using Quality Semiconductor FIFOs. These FIFOs provide better results in high reliability systems, due to the 6-transistor cell design.



Note: The arrows on the left side indicate the write pointer and the ones on the right indicate the read pointer. The upper level diagrams are a normal retransmit and the lower level indicate a limitation of the retransmit operation.

Figure 13. Retransmit Operations

Conclusion

FIFOs are useful as data queues to match data rates in computer systems. With cycle times of 25 nsec, newer applications are available in graphics and DSP systems and in data communication systems. With fast flip access times, external timings are relaxed by using Quality Semiconductor FIFOs. These FIFOs provide better results in high reliability systems due to the 6-transistor cell design.

Q

The 6-Transistor SRAM Cell and Its Advantages

Application
Note
AN-03

by
David Wyland

Data in RAM memories is stored in bit cells, one for each bit in the memory. For example, a 16Kx4 SRAM stores its 65536 bits in 65536 separate bit cells. High speed CMOS SRAM bit cells come in two types, four-transistor (4T) and six-transistor (6T). The 4T cell is the smaller of the two, while the 6T cell has higher performance. New developments in cell design allow the 6T cell to be made nearly the same size as the 4T cell. In this application note, we will examine the differences between the 4T and 6T cell and the advantages and disadvantages of each.

The four-transistor and six-transistor cells are so named because they use four and six transistors respectively in the cell design. Figure 1 shows circuit diagrams of the 4T and 6T cells in an SRAM design. The cells and their support circuitry are similar except that the 4T cell uses a pair of resistors for cell pull-up, while the 6T cell uses P-channel transistors for this purpose.

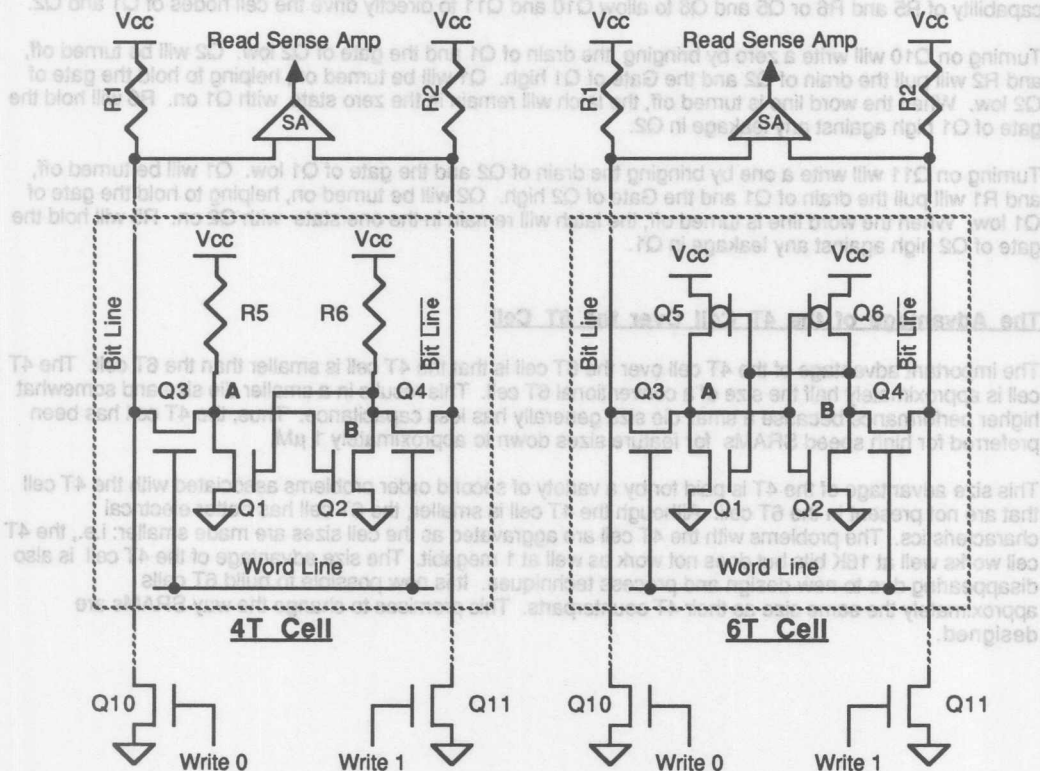


Figure 1: 4T and 6T SRAM Cells

SRAM Operation with 4T and 6T Cells

Data in the SRAM cells shown in Figure 1 is stored in the cross coupled latch formed by Q1 and Q2. A zero is stored when Q1 is on and Q2 off; a one is stored when Q2 is on and Q1 is off.

To read or write data to the cell, the bits in a word are selected by taking the word line high. This turns on the select transistors, Q3 and Q4, and connects Q1 and Q2 to the bit lines, Bit Line and Bit Line. When the select transistors are on, Bit Line or Bit Line is taken low by Q3 or Q4 if a zero or one is stored, respectively. The sense amplifier detects which line has been taken low and generates a one or zero according to the difference in voltage between the bit lines.

A sense amplifier is used to increase speed. Q3 and Q4 are intentionally made weak so that when they are turned on, only a small voltage drop appears across R1 or R2, and very little voltage develops across Q1 or Q2, respectively. This allows R1 and R2 to be made small, reducing the time constant and corresponding settling time for the voltage developed across them. The sense amplifier amplifies the voltage developed to a full logic level. The sense amplifier also provides an earlier indication of the logic level because the full, final voltage does not need to be developed across R1 or R2 before the sense amplifier can tell a one from a zero.

Data is written into the cell by turning on Q10 or Q11 when the word has been selected. This brings Bit Line or Bit Line low, respectively. Q3, Q4, Q10 and Q11 are made strong enough relative to the current capability of R5 and R6 or Q5 and Q6 to allow Q10 and Q11 to directly drive the cell nodes of Q1 and Q2.

Turning on Q10 will write a zero by bringing the drain of Q1 and the gate of Q2 low. Q2 will be turned off, and R2 will pull the drain of Q2 and the Gate of Q1 high. Q1 will be turned on, helping to hold the gate of Q2 low. When the word line is turned off, the latch will remain in the zero state with Q1 on. R6 will hold the gate of Q1 high against any leakage in Q2.

Turning on Q11 will write a one by bringing the drain of Q2 and the gate of Q1 low. Q1 will be turned off, and R1 will pull the drain of Q1 and the Gate of Q2 high. Q2 will be turned on, helping to hold the gate of Q1 low. When the word line is turned off, the latch will remain in the one state with Q2 on. R5 will hold the gate of Q2 high against any leakage in Q1.

The Advantage of the 4T Cell Over the 6T Cell

The important advantage of the 4T cell over the 6T cell is that the 4T cell is smaller than the 6T cell. The 4T cell is approximately half the size of a conventional 6T cell. This results in a smaller die size and somewhat higher performance because a small die size generally has less capacitance. Thus, the 4T cell has been preferred for high speed SRAMs for feature sizes down to approximately 1 μM .

This size advantage of the 4T is paid for by a variety of second order problems associated with the 4T cell that are not present in the 6T cell. Although the 4T cell is smaller, the 6T cell has better electrical characteristics. The problems with the 4T cell are aggravated as the cell sizes are made smaller: i.e., the 4T cell works well at 16K bits but does not work as well at 1 megabit. The size advantage of the 4T cell is also disappearing due to new design and process techniques. It is now possible to build 6T cells approximately the same size as their 4T counterparts. This promises to change the way SRAMs are designed.

The Advantages of the 6T Cell Over the 4T Cell

The 6T cell has several known advantages over the 4T. The 6T cell has a lower standby power than the 4T because the 4T has pull-up resistors in each cell drawing current, while the 6T cell has no standby current other than leakage. At room temperature, the 4T standby current may be microamperes, while the 6T current can be nanoamps. This is useful in battery powered equipment.

There are several other areas where the 6T cell has definite advantages: lack of static hold problems, good radiation hardening characteristics, ability to scale to higher densities, and better alpha particle immunity. These problems will be discussed in turn.

Static Hold In 4T and 6T Cells

Static hold refers to the ability of a device to retain information. It is defined negatively: an SRAM with a static hold problem "forgets" data if left sitting for a long enough time without use.

Static hold problems occur in 4T cell SRAMs because of leakage. The pull-up resistors in the 4T cell, R5 and R6, are very large, 100 μohm being typical at room temperature. As a result, they can sustain a leakage current in the off device of Q1 or Q2 of less than 50 picoamperes at room temperature.

Static hold problems occur in 4T SRAM cells because of subthreshold leakage in the Q1-Q4 transistors. Subthreshold leakage is actually transistor action. When the gates of Q1-Q4 are at zero volts, significantly below threshold, there is still some transistor action, albeit very small. If a plot of current versus gate voltage is made, the current through these devices does not cut off immediately at threshold but declines exponentially with gate voltage. Even though the gate voltage may be zero, there can still be some current flowing. It can be eliminated only by taking the gate voltage significantly below the threshold voltage.

The typical static hold problem with a 4T cell occurs at cold temperature rather than hot. The subthreshold leakage current is a function of transistor geometry and doping profiles, and is not a strong function of temperature. The R5/R6 pull up resistors are made from high resistivity polysilicon, which has a strong temperature coefficient, with the resistance going up as the temperature goes down. The current capability of these resistors therefore decreases rapidly with decreasing temperature. At cold temperatures, the subthreshold leakage may exceed the current that can be supplied by R5/R6 and cause the cell to become unstable or flip over. At this point, the SRAM has "forgotten" its data.

Static hold problems are expensive to find in terms of test time. Because the leakage is very small compared to the node capacitances, you typically have to wait one or more seconds for the subthreshold leakage to drag down one or more nodes. Also, tests must be performed at cold temperatures; you cannot correlate a static hold problem to room temperature data.

Static hold problems in 4T cell SRAMs usually occur because of variations in the manufacturing process. If the resistivity of the polysilicon gets too high on a lot or varies significantly across a wafer, you can have static hold problems. These can be overlooked because the part appears to work at room temperature and for normal test times of a few milliseconds per read/write pass through the RAM.

The 6T cell has no static hold problems. The Q5/Q6 pull-up transistors are capable of supplying orders of magnitude more current, microamperes instead of picoamperes, compared to the 4T cell. As a result, subthreshold leakage cannot cause a static hold problem.

Radiation Hardening Capability of 4T and 6T Cells

Gamma radiation affects 4T cells more than 6T cells. Typical failure dose numbers for untreated SRAMs are on the order of 10K rads for 4T devices and **50-100K rads** for 6T devices. Gamma radiation is commonly encountered in spacecraft and satellites, being solar radiation without benefit of shielding by the atmosphere.

Gamma radiation changes the threshold of devices. It also causes additional leakage currents because of surface effects at the silicon/SiO₂ interface. Change in threshold voltage is generally in the direction to increase subthreshold leakage in N-Channel devices. Because the 4T cell is sensitive to leakage in the cell due to the low leakage tolerance of the R5/R6 pull up resistors, 4T cell RAMs have relatively low radiation tolerance. Absorbing a large enough dose of radiation results in static hold problems. The 6T cell fares much better because it lacks the resistors which cause static hold problems.

High Density Scaling Capability of 4T and 6T Cells

The 6T cell looks increasingly better than the 4T as the cell sizes are made smaller. This is important as SRAMs go to ever higher densities and smaller geometries.

As cells are "shrunk", i.e., made geometrically smaller as though increased production equipment resolution, a first approximation would say that most electrical characteristics remain the same. In a geometric shrink, the resistance of R5/R6 in the 4T cell should remain constant if the ohms/square remain the same because the number of squares is the same in a geometrical shrink. However, as the cell is made smaller, this does not hold true.

As you shrink the X and Y dimensions, you must also shrink the Z dimension, the thickness of the polysilicon. This increases the ohms/square, increasing the value of the resistor. Not only does the ohms/square number increase, but it increases non-linearly. A small decrease in polysilicon thickness can result in a large increase in the ohms/square, significantly above the linear increase with decreasing thickness one would expect. This makes the polysilicon resistivity harder to control.

As you shrink the absolute distances involved, the polysilicon begins to be affected by the silicon it contacts. There is diffusion of dopant from the substrate into the polysilicon. This causes two problems. Diffusion of dopant into the relatively undoped polysilicon will reduce its resistivity in a relatively uncontrolled manner. It will also create the conditions for breakdown, or punch-through, of the resistor at normal operating voltages, giving high and erratic currents in the cell.

Another problem associated with shrinking the 4T cell is that the subthreshold leakages of the devices increase in absolute terms as they are made smaller. Increasing subthreshold leakage coupled with higher and more poorly controlled resistor values is a recipe for static hold problems.

The net result of these mechanisms is that shrinking the 4T cell causes manufacturing problems related to control of the polysilicon load resistors, R5/R6. These manufacturing problems show up as yield loss and reliability problems such as static hold.

The 6T cell does not have these problems because it does not use polysilicon load resistors. The shrink of the 6T cell is an exercise in shrinking the geometry of the transistors themselves, a better known and controlled operation.

Alpha Particle Soft Error Performance of 4T and 6T Cells

The 6T cell has better alpha particle error characteristics than the 4T cell. This problem is, again, related to the resistor pull-up in the 4T cell. An alpha particle is a charged helium nucleus which has a high energy level and can penetrate significant distances through solid matter, such as an IC package or piece of silicon. Alpha particles are generated by radioactive decay. Every package, plastic or ceramic, has trace elements of radioisotopes which generate alpha particles as they decay. Alpha particles can also be generated from other materials in and around the equipment where the SRAM is installed.

When an alpha particle passes through a piece of silicon, it leaves a trail of ionized particles, i.e. hole-electron pairs. If the particle passes through the depletion region of a SRAM bit cell transistor, it can cause a transient current in that transistor. The particle passes through very quickly, on the order of 100 picoseconds. If this happens to Q1, it will have a momentary pulse of drain current corresponding to the charge generated by the particle. This will immediately discharge the capacitance at node A, the capacitance associated with the drain of Q1 and Q3 and the gate of Q2. This looks very much like writing a zero to the cell. If the charge generated by the particle is large enough, this is what happens.

There will be some alpha particles (or combinations of particles) which generate sufficient charge to flip the cell, i.e. do a false write. This means that the alpha particle problem cannot be absolutely eliminated, only reduced. The alpha particle problem is therefore defined as a soft error rate probability per alpha particle, or alternatively a soft error rate as a function of alpha particle emission rate.

When an alpha particle has discharged the stray capacitances associated with Q1, the cell must now recover. In the 4T cell, this means that R6 must recharge the capacitance of node A. Although the capacitance at this node is small (50 fF typical) the pull up resistor is so large (100 $g\Omega$) that the time constant of this node is in milliseconds. During this interval, the cell is in an internally metastable state. If the cell is selected, the pull up resistors now become R1/R2, a much smaller value. However, the node must still stabilize. The metastability still exists, but with a shorter resolution time. Although the values of R1/R2 are small, the capacitance of the bit lines is relatively large. The result is that the metastable settling time may be significant with respect to the access time of the device.

Because of the metastable action of the 4T cell, alpha particle impact can result in lengthened access times as well as simple flipped cells. The lengthened access times export metastability to the next system interface, resulting in soft errors due to transiently exceeding timing margins. This increases the effective soft error rate of the 4T cell.

The 6T cell does not have this metastability problem, in a practical sense. In the 6T cell, the Q5/Q6 pull up transistor results in a much lower effective time constant, on the order of a few nanoseconds rather than a few milliseconds. As a result, the probability of a metastable stretchout of the access time is very small. The alpha particle would have to hit during the access itself to cause this to happen. This reduces the probability of this type of error by approximately the ratio of the two time constants, several orders of magnitude.

Conclusion

The 4T cell was preferred for fast RAM designs below 64K bits and using 1.2 μM or larger lithography because of its smaller cell size. Its problems were born because of the benefits of yield and speed that small cell size gave. New techniques have allowed the 6T cell to approach the 4T cell in relative size, eliminating the need to suffer the tradeoffs of the 4T cell. This has happened just in time because as SRAM densities progress beyond 256K and lithography resolution drops below 1.0 μM , the 6T cell becomes a necessity for fast, high yield SRAM design.

Alpha Particle Soft Error Phenomena of 4T and 6T Cells

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When an alpha particle has discharged the stray capacitances associated with Q1, the cell must now recover. In the 4T cell, this means that F8 must recharge the capacitance of node A. Although the capacitance at this node is small (50 fF typical) the pull up resistor is so large (100 GΩ) that the time constant of this node is in milliseconds. During this interval, the cell is in an internally metastable state. If the cell is isolated, the pull up resistor now becomes R1/R2, a much smaller value. However, the node must still stabilize. The metastability still exists, but with a shorter resolution time. Although the values of R1/R2 are small, the capacitance of the bit lines is relatively large. The result is that the metastable settling time may be significant with respect to the access time of the device.

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High Speed SRAMs and Bus Contention Issues

Application
Note
AN-04

by
Suneel Rajpal

Memory devices are mainly used in bus-oriented systems. Fast SRAMs with common I/O data may encounter bus contention while switching from read operations to write operations and vice versa. Figure 2-1 shows a common I/O SRAM connected to an external driver. Figure 2-2 shows an SRAM output being disabled due to a write operation, and the system placing data on the RAM data inputs. Bus contention can occur when two devices drive the bus simultaneously. The data is in high impedance t_{WHZ} ns after the write line goes low. This can directly affect the write pulse width minimum specification which is the sum of t_{WHZ} and t_{DS} , the data setup time.

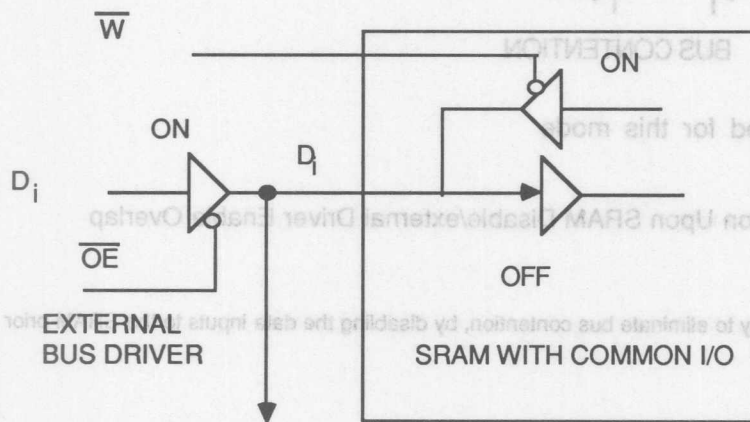


Figure 2-1. Possible Data Contention in SRAM with Common I/O

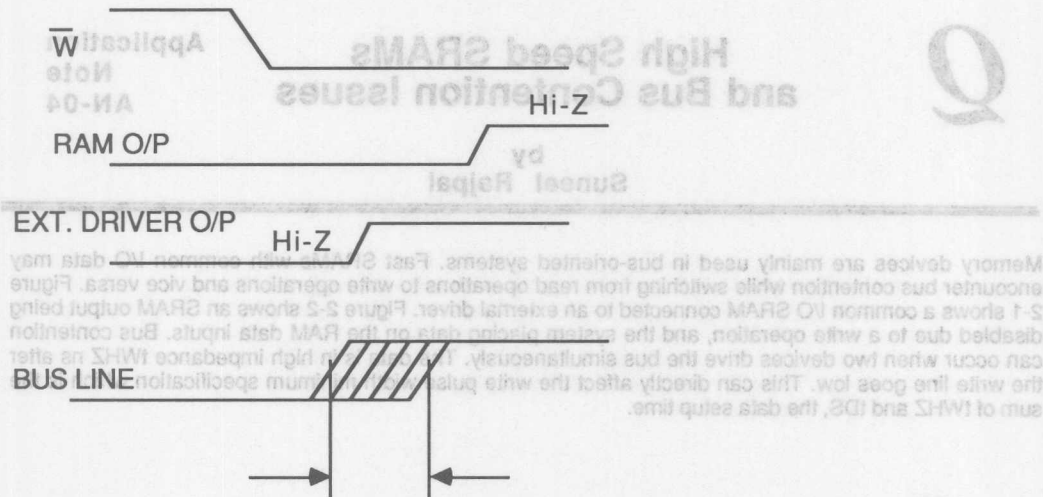


Figure 2-2. Bus Contention Upon SRAM Disable/external Driver Enable Overlap

Figure 2-3 shows another way to eliminate bus contention, by disabling the data inputs to the SRAM prior to enabling the output.

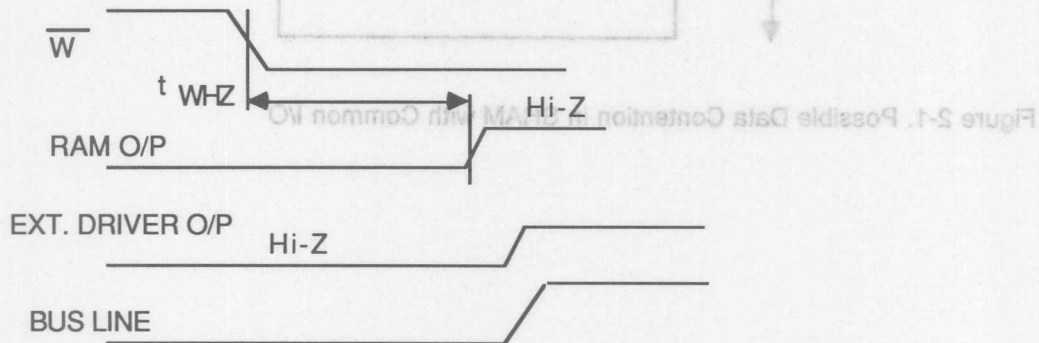


Figure 2-3. Input Driver Disabled Prior to Disabling RAM Output

Figure 2-4 shows the chip select being used to avoid bus contention. The chip is deselected before the write operation begins. The write signal is asserted t_{CHZ} ns after the chip select is deasserted. There is no disadvantage from a speed viewpoint because the write pulse width in this case is measured from the falling edge of $\overline{CS}$ to the rising edge of $\overline{CS}$ or $\overline{WE}$. However bus contention is eliminated.

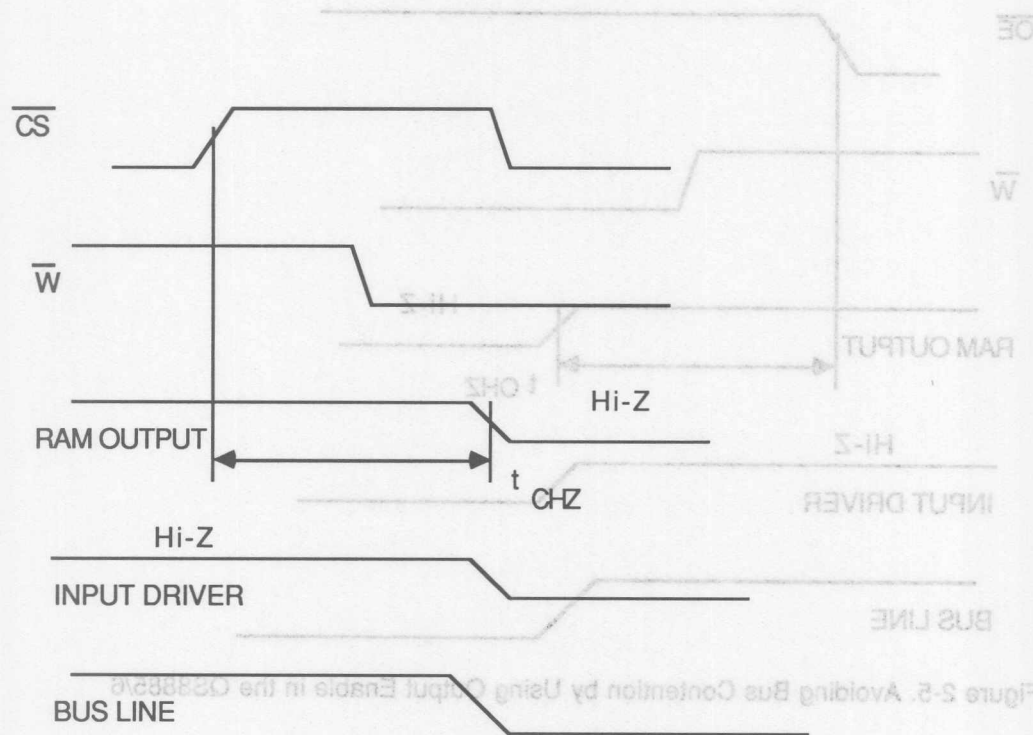


Figure 2-4. Avoiding Bus Contention by Using $\overline{CS}$

Another way to avoid contention in the common I/O devices is to use the output enable control to keep the outputs in high impedance. This is shown in figure 2-5. Quality Semiconductor's 16Kx4 SRAMs have output enables in the QS8886 and QS8885. These are suitable building blocks for cache memory and high-speed add-on memories for applications with zero wait state operations.

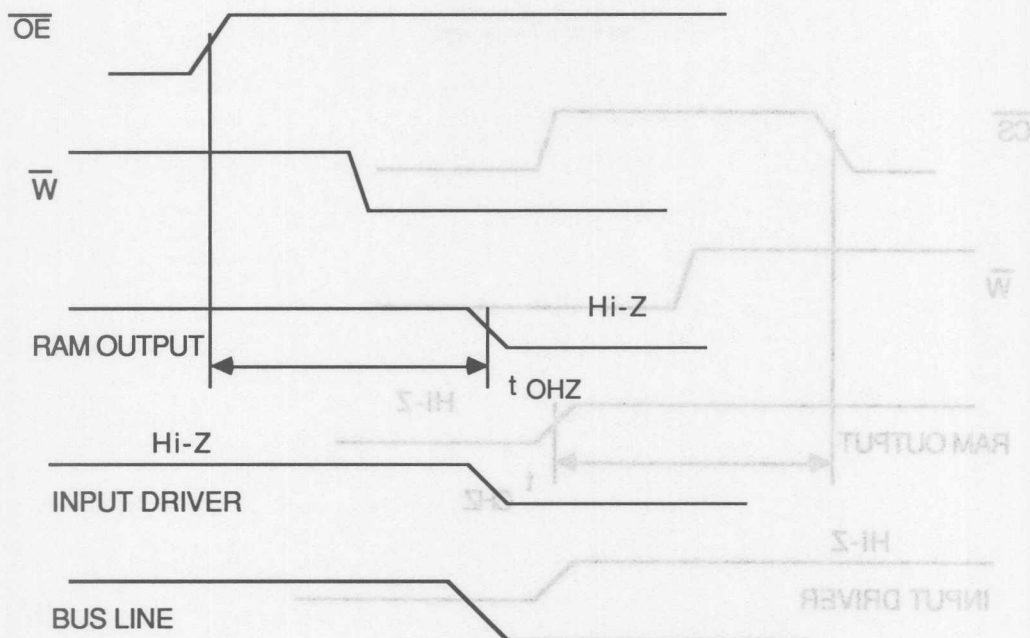


Figure 2-5. Avoiding Bus Contention by Using Output Enable in the QS8885/6

Devices with separate I/O do not have bus contention problems because dedicated ports are assigned for the input and output. QS8881/2 are devices with separate I/O. These are useful in implementing control stores for bit-slice and DSP systems, and for data caches. These applications are covered in Chapter 3.

HIGH-SPEED DESIGN ISSUES AND BOARD LAYOUT CONSIDERATIONS

Microprocessors operate at speeds of 33 MHz and RISC-based processors operate at 40 MHz in TTL-compatible systems. This places a greater challenge on SRAM circuit designers with the requirements for access times, data set up times and output enable/disable times. Another consideration is the characteristic of high-speed buses.

High-speed microprocessor buses tend to operate in harsh, noisy environments and sometimes the buses are unterminated. Unterminated bus lines can receive and radiate Electromagnetic Interference (EMI) because they act like antennas. The best way to reduce this EMI is to ensure that the each bus line is terminated with a low-impedance load that is a pull-up or pull-down resistor.

If the value of the termination resistor is equal to the value of the characteristic impedance of the bus line, it provides the best incident switching and it minimizes the amount of reflection. The smaller the resistor, the greater the power consumption. If the resistor is too small, its value can approach the source impedance value of the transmitting device, leading to a noise margin degradation on the receiving device. A large resistor value, typically between $1K\Omega$ and $10 K\Omega$, can be selected after experimentation.

Another consideration is the ground bounce current. Due to fast switching times and high current switching, the level of the on-chip ground may change from the external ground as the device charges and discharges. The on-chip ground voltage is affected by the inductive coupling and changing current. Since 8-bit SRAM devices can have all eight outputs switching, there is a possibility of an even greater ground bounce effect. Spurious noise spikes on the power lines can affect the data contents of the device and also affect neighboring devices' power supplies. Circuit designers have developed circuitry that controls the rise and fall time to minimize undershoot, overshoot and ringing. This is inherently why 8-bit SRAM devices are slower than 4-bit SRAM devices for the same density.

Noise can be induced into SRAM devices by inadequate power supply feeds and power supply decoupling. Ground planes should be used extensively to minimize resistances and inductances. Otherwise, Vcc or ground bounce will occur. Typically, the resistance should be less than 0.1Ω . A multilayer board with at least one ground plane is recommended. High-quality decoupling capacitors with values between .01 to $.1 \mu F$ must be located near the power pins. A large capacitor of about $1 \mu F$ must be used on each Vcc line to provide for current surges. If the devices are socketed, sockets with gold-plated copper contacts containing built-in decoupling capacitors are recommended.

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High Speed SRAMs in Cache and Bit Slice Applications

Application
Note
AN-05

by Suneel Rajpal

Introduction

This application note deals with applications requiring high-speed RAMs for caches, modifiable storage and control stores for CISC-, RISC- and bit-slice-based systems. There are different requirements for primary and secondary caches. Quality Semiconductor devices extend from 4Kx4 cache tag RAMs to 16Kx4 cache tag RAMs and 16Kx4 SRAM. Higher density products, such as 8Kx18, 8Kx16, 32Kx8 and 64Kx4 are also in development.

SRAM requirements for Cache Memory Implementations

Cache memories are prevalent in high-end CPU designs. They increase system performance by reducing main memory accesses. A cache is a small high-speed memory that is placed between a CPU and a larger, slower main memory. The cache keeps a copy of main memory data. When the CPU does a memory operation it looks up a cache tag RAM which determines if the requested word is present in the cache data memory. If the data is present in the cache, the main memory does not have to be accessed on read operations. If not, a main memory cycle is initiated and the cache data and tag RAM are updated.

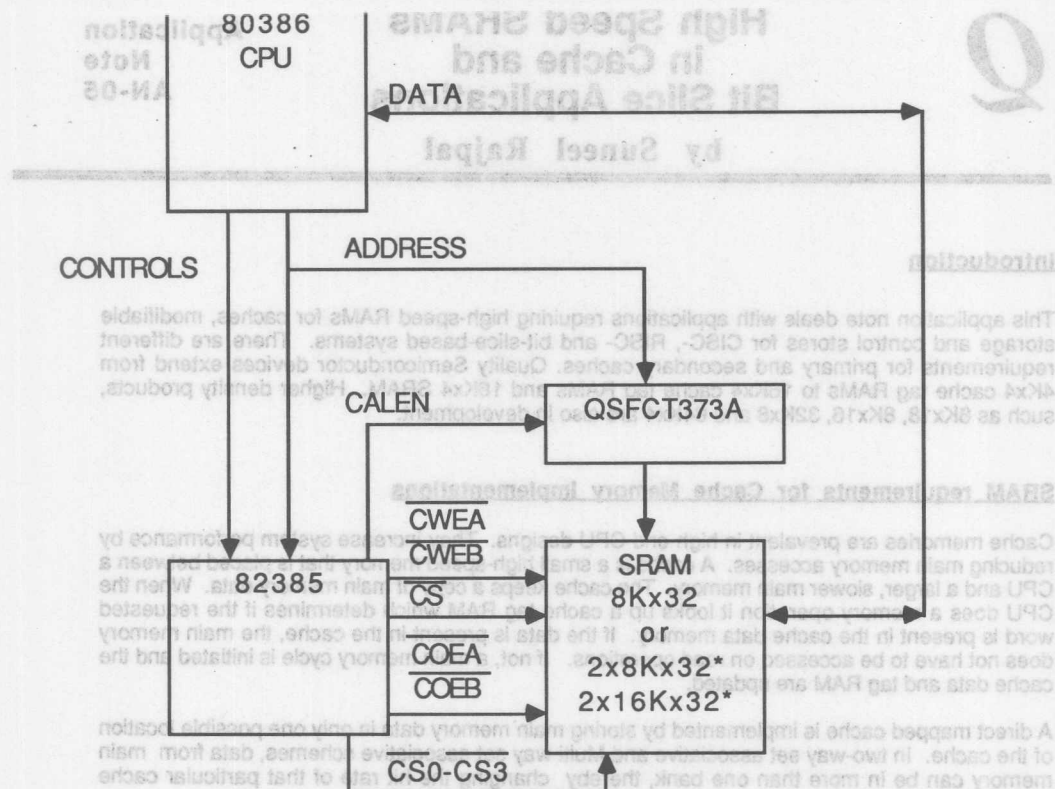
A direct mapped cache is implemented by storing main memory data in only one possible location of the cache. In two-way set associative and Multi-way set associative schemes, data from main memory can be in more than one bank, thereby changing the hit rate of that particular cache organization.

Some of the features required in implementing cache data and cache tag RAMs are high speed accesses, very fast enable and disable times and short write pulse widths. Quality Semiconductor SRAMs are to be ideal for cache implementations.

The Intel 80386 Cache Requirements

The high speed versions of the Intel 80386 CPU enhance their performance with an external cache. There are two popular approaches: (1) a cache controller-based design, such as the Intel 82385 that contains the tag portion and generates the controls for the cache data RAM, or (2) a cache controller that is user-defined, built of discrete logic and PALs, for which both tag and data RAM have to be added externally.

Figure 3-1 shows an Intel 82385 cache controller that accesses a 32-Kbyte cache. The external cache can be organized as a 2-way set associative or direct mapped. Figure 3-1 shows the 80386 with the 82385, and the cache data RAM in this application is without a buffer. A QSFCT373/A device that stores the 80386 local address is shown.



* These configurations are possible with very little external logic and can be done using QS8816 or QS8817, which are 2x4Kx16 SRAMs with on-chip latches.

Figure 3-1. The Intel 80386 with 82385 Cache Controller and Data Cache

The critical path of the SRAM is estimated as follows for a 33 MHz CPU. The 82385 controller contains the cache tag RAMs that determine if a cache hit occurred (implying a match condition existed in the tag RAMs). On a hit condition the outputs of the data SRAM are enabled by the /COE signal from the 82385. The data accessed from the SRAM has to be valid before the setup time of the 80386 processor. The SRAM requirements are computed as follows:

Read Cycles

$2 \times \text{CLK2 period} - t_{25b}(82385\text{-}/\text{COE delay}) - \text{SRAM}(/OE \text{ to data valid}) - t_{21}(80386 \text{ data setup}) \geq 0$

$30 - 15 - t_{OE} - 5 \geq 0$

t_{OE} (output enable to valid data) of the SRAM must be ≤ 10 ns

$4 \times \text{CLK2} - t_{21b}(\text{CALEN valid delay}) - t_{pd} \text{ Latch to output (QS FCT373/A)} - \text{SRAM adrs to data} - t_{21}(80386 \text{ data setup}) \geq 0$

$60 - 20 - t_{pd}(\text{FCT373/A}) - \text{SRAM}(t_{AA}) - 5 \geq 0$

$t_{pd}(\text{QS FCT373/FCT373A LE to Output delay}) + \text{SRAM adrs to data delay} \leq 35$ ns

Cache Read Cycle followed by a Write

Data turn-off = $t_{25c}(82385 / \text{COE delay}) + \text{SRAM Output Disable } t_{OHZ}$

Data turn-off = $12 + t_{OHZ}$

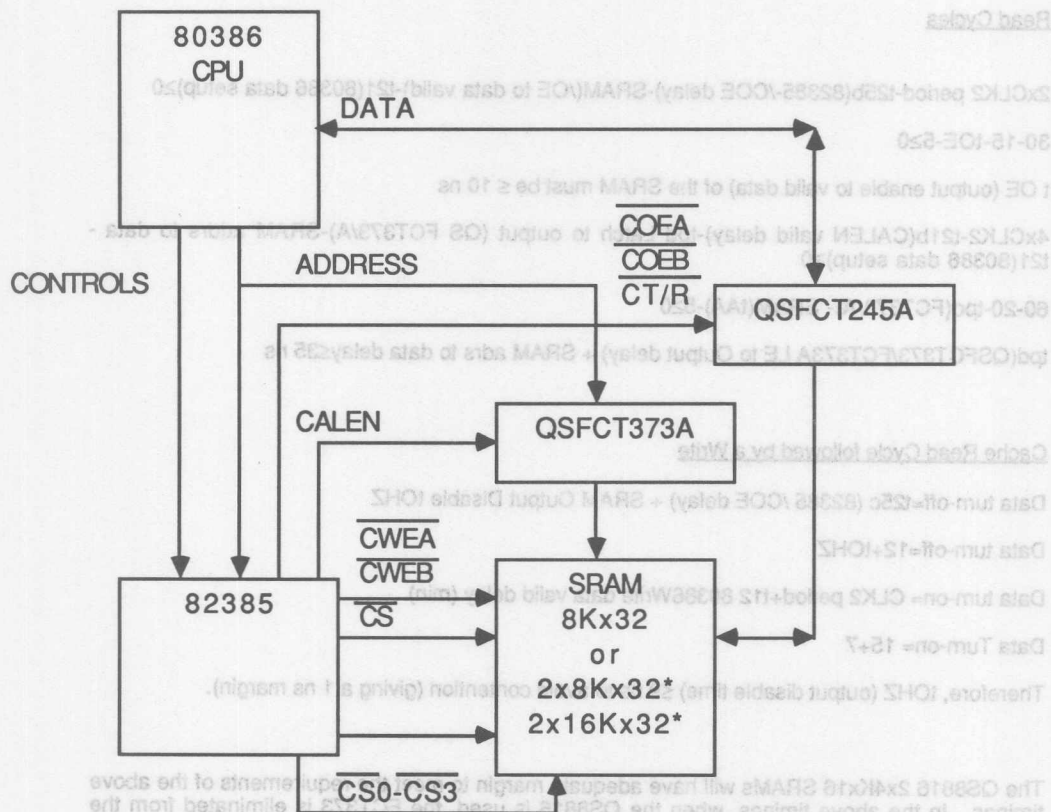
Data turn-on = $\text{CLK2 period} + t_{12} 80386 \text{ Write data valid delay (min)}$

Data Turn-on = $15 + 7$

Therefore, t_{OHZ} (output disable time) ≤ 9 ns to avoid contention (giving a 1 ns margin).

The QS8816 2x4Kx16 SRAMs will have adequate margin to meet the requirements of the above timings. In the above timings, when the QS8816 is used, the FCT373 is eliminated from the access time computations, as the 8816 has an on-chip latch for address storage. You can also calculate the values for write cycles. However, read timings require faster specifications.

Figure 3-2 shows the cache data RAM being buffered with QSFCT245 devices. In this configuration, the read followed by a write is not as critical as the previous non-buffered case because the buffer disable time is much faster than an SRAM disable time.



* These configurations are possible by using QS8816/7

2x4Kx16 SRAMs

Figure 3-2 The 80386 with 82385 Cache Controller and External Buffers

The critical path for read operations is estimated as follows: the 82385 provides the control signals for the QSFCT245 buffers that enable the data to the 80386 bus before the required set up time.

2xCLK2 period -t25b (82385- $\overline{COE}$ delay) -tpd ($\overline{OE}$ to A delay) -t21 (80386 data setup) ≥ 0

30 -15- tpd(QS FCT 245) -5>0

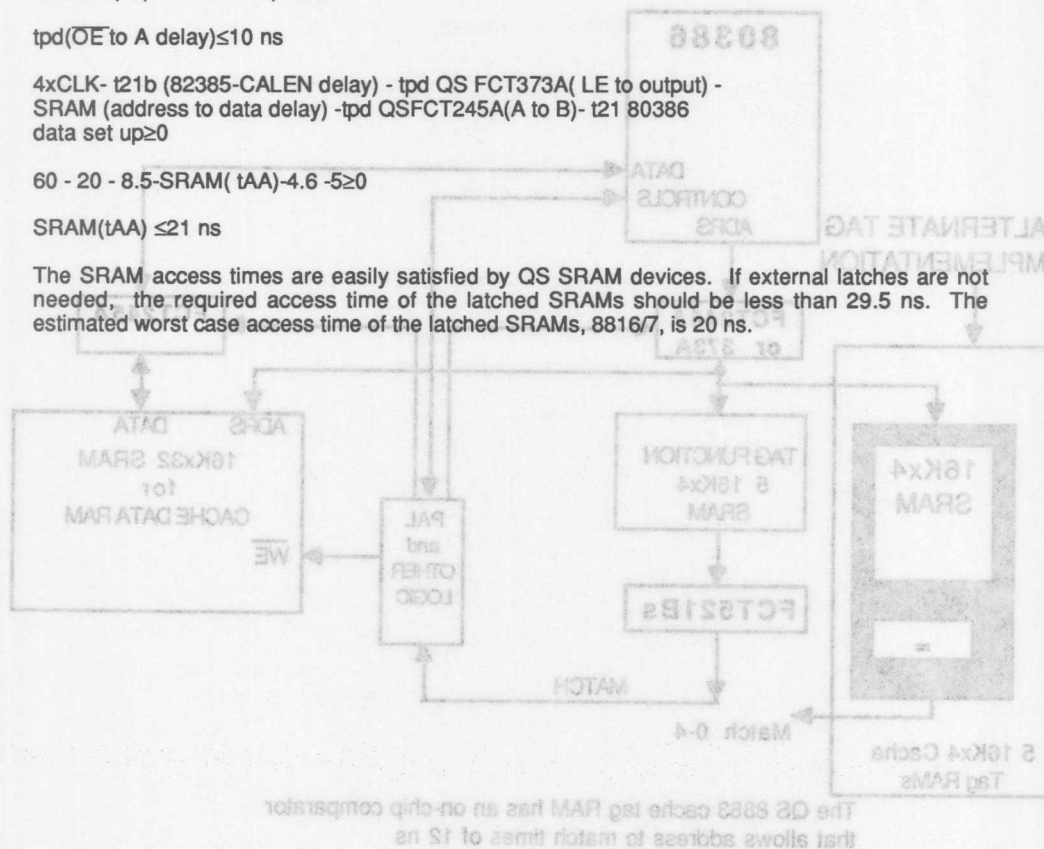
$$\text{tpd}(\overline{\text{OE}} \text{ to A delay}) \leq 10 \text{ ns}$$

4xCLK- t21b (82385-CALEN delay) - tpd QS FCT373A(LE to output) -
SRAM (address to data delay) -tpd QSFCT245A(A to B)- t21 80386
data set up>0

60 - 20 - 8.5-SRAM(tAA)-4.6 -5≥0

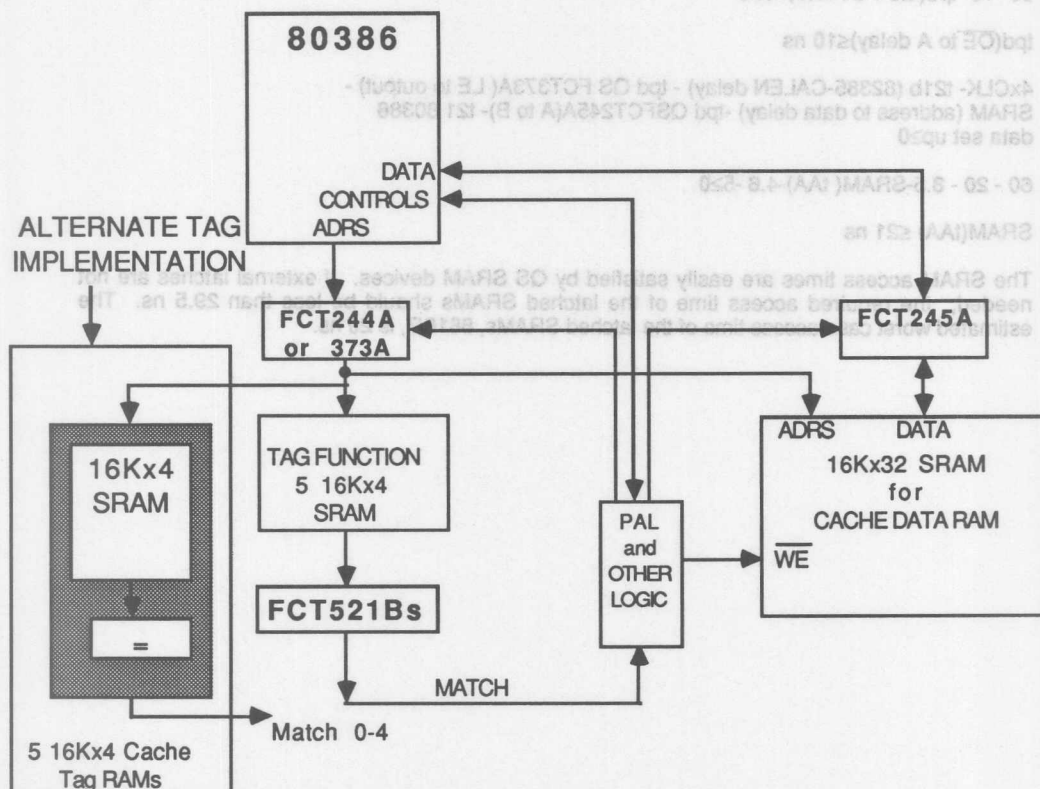
SRAM(t_{AA}) ≤ 21 ns

The SRAM access times are easily satisfied by QS SRAM devices. If external latches are not needed, the required access time of the latched SRAMs should be less than 29.5 ns. The estimated worst case access time of the latched SRAMs, 8816/7, is 20 ns.



Intel 386 CPU Non-82385 Applications

Customized cache controller designers use separate cache tag RAMs and cache data RAMs. Typically a 4K, 8K or 16K deep tag RAM is used. The data RAM can be 8K or 16K deep. Figure 3-3 shows a typical application where a 16K-deep tag RAM and 16K-deep data RAM are used.



The QS 8883 cache tag RAM has an on-chip comparator that allows address to match times of 12 ns

Figure 3-3 The 80386 with an External Direct Mapped Cache

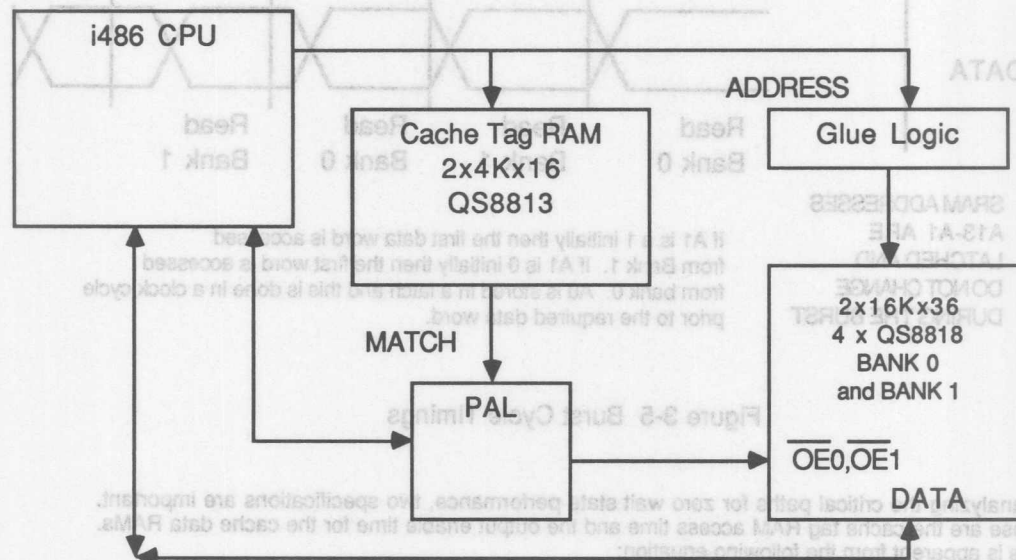
On memory accesses it can be determined if the requested word is present in the cache tag RAM by examining the match output. The assertion of the match signal indicates that the previously stored tags are equal to the current access, and on read requests the main memory does not have to be accessed. On processor writes, main memory is updated on every cycle if a write-through scheme is implemented. A dirty bit is set on the write-back scheme and the main memory is updated later.

The critical timing in these applications are the address to match (maximum) specification and the write pulse width (minimum) specification. The first critical parameter is directly used in the path to turn on the QSFCT245A device during read hits. The second parameter is based on the write miss operation, and an entry may have to be invalidated in the cache tag RAM. This assumes that on write operations the data is always updated in the cache data RAMs, and if a cache miss

occurred, the corresponding entry in the tag RAM is invalidated. This update technique generates a particular critical path, and the data setup time and the write pulse widths are key parameters for no wait state operations. The QS8883 cache tag RAM devices are ideal for building cache tag and data RAMs and eliminating wait states. The QS8883 cache tag RAM combines the comparator inside the device so that the address to match time is only 12 ns.

The Intel 80486 CPU and an External Cache

The Intel 80486 has an on-board 8 Kbyte cache, and its performance can be enhanced with an external second-level cache. Figure 3-4 shows an 80486 CPU with an external, 2-way set-associative 64 Kbyte cache.



The critical path includes the tag RAM access time plus the output enable to data valid specification of the cache data RAM

Figure 3-4. The Intel 486 with an External Cache

The external memory used in 80486 applications must support burst transfers. The first word is accessed in two 80486 clock cycles and the subsequent three words are accessed in one clock cycle each. The external system indicates that it can present valid data by asserting the BRDY# signal to the processor. If the BRDY# is not asserted at the appropriate rising clock edge, then a wait state is inserted. The 80486 address signals are switching during burst mode operations. However, these cannot be used to access the SRAMs as there will be insufficient time to execute the burst without adding wait states. The high-speed burst access can be accomplished by enabling the outputs on one of the two banks and also by toggling the least significant address bit. This is explained in the timing diagram shown in Figure 3-5.

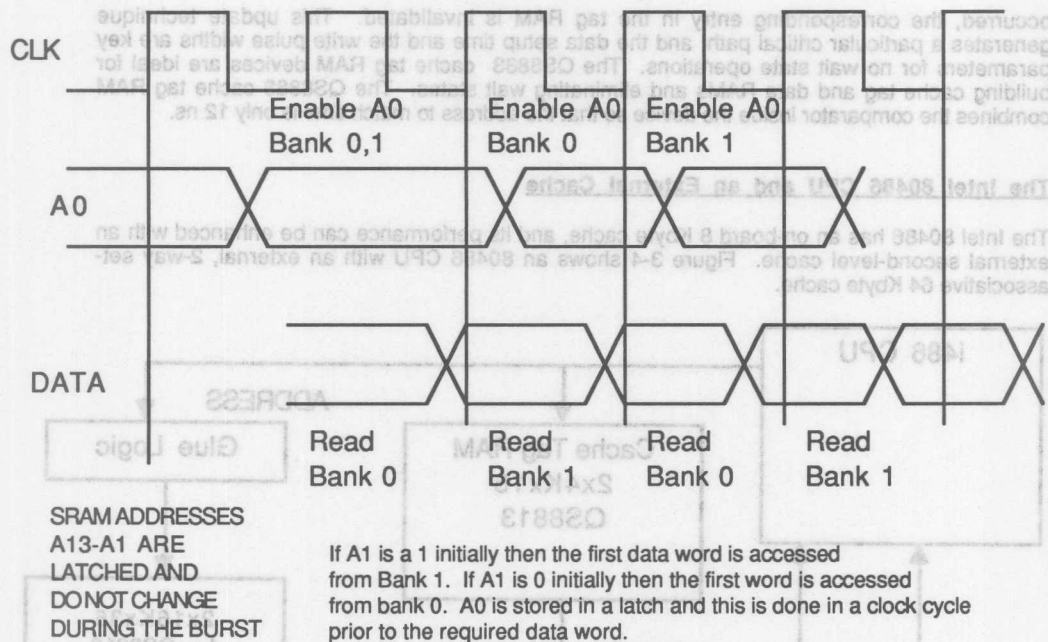


Figure 3-5 Burst Cycle Timings

In analyzing the critical paths for zero wait state performance, two specifications are important. These are the cache tag RAM access time and the output enable time for the cache data RAMs. This is apparent from the following equation:

Address Valid (t_6 -80486 spec) + Tag ram Access + PAL delay + Output Enable Time(Cache data RAM) + data setup time (t_{22} -80486 spec) + derating ≤ 60 ns

Inserting $t_6=16$ ns, $t_{22}=5$ ns, PAL delay= 7.5 ns, derating = 2ns,
Tag RAM access address to match delay + Output Enable to valid data(Cache Data RAM) ≤ 29.5 ns

As one designs with higher speed processors, there is increased demand for faster access times, faster enable and disable times, and integration of latches or self-timed write operations.

Quality Semiconductor, Inc. makes high speed logic devices such as latches and registers. The SRAMs have fast enable and disable times as well. This allows 2-1-2 cycles (two cycles for the first read, one cycle each for the next three reads, and two cycles for a write) for the 80486 processor. The 8Kx18 SRAMs also has on-chip counters to support burst mode operations transferring four words to the CPU. Quality Semiconductor is also defining SRAMs and modules that are application-specific for Intel microprocessors.

The MIPS RISC processor

The MIPS RISC processor requires external caches for instructions and data. The processor provides the necessary control signals to latch the instruction and data address, and also stores the corresponding data. Figure 3-6 shows the bus operations during Phases 1 and 2 of the clock. Figure 3-6 shows the ping-pong effect of the processor caches. Every cycle, either the instruction or data cache are accessed. On the following cycle, the other cache is accessed.

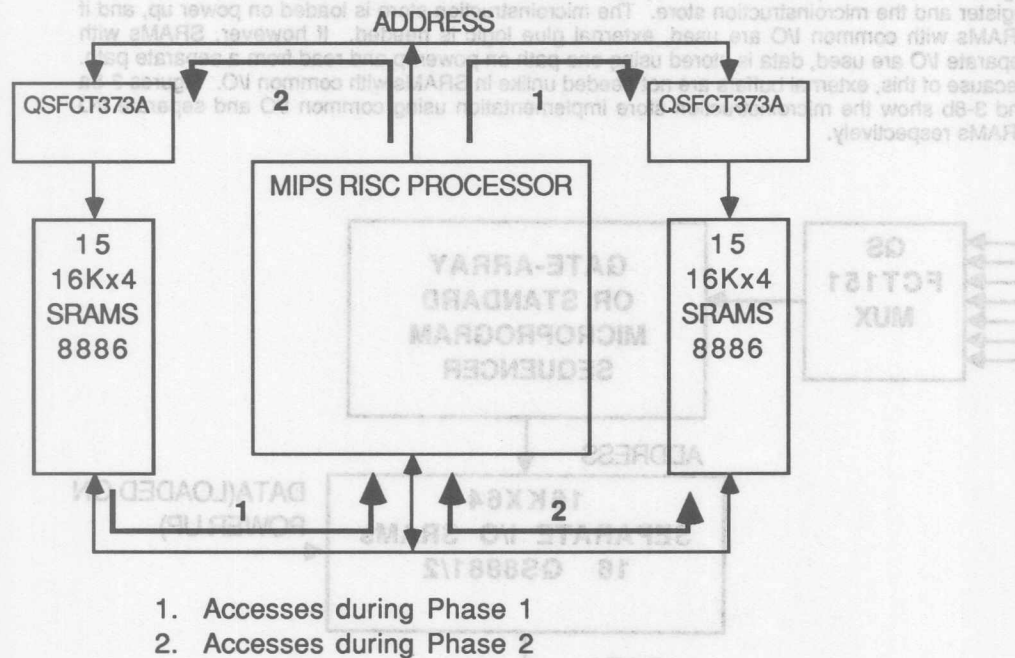


Figure 3-6 The Instruction and Data cache for the MIPS RISC Processor

Bus contention is possible, and this demands fast enable and disable times for any selected SRAM. Also, if you analyze the 25 MHz RISC processor specification, the access times of the SRAM have to be 19 ns or less for proper operation, and the data setup time must be less than 11 ns. The SRAMs must have zero hold time for both address and data from the end of write. The SRAM devices made by Quality Semiconductor, Inc. either meet or exceed the requirements for the MIPS RISC processor at 33 MHz. All of the key requirements such as access times, output enable times and data set specifications are met by the 16Kx4 SRAMs made by Quality Semiconductor.

Bit Slice Processors

In the high-performance end for controllers and graphics, users often implement their systems based on bit-slice type machines. This gives a performance edge for certain applications. The numbercrunching elements can be based on bit slice, gate arrays or discrete elements. However, the memory portion is always based on high-speed SRAMs and can not be integrated.

Figure 3-7 shows a portion of the implementation with the address sequencer, the pipelined register and the microinstruction store. The microinstruction store is loaded on power up, and if SRAMs with common I/O are used, external glue logic is needed. If however, SRAMs with separate I/O are used, data is stored using one path on powerup and read from a separate path. Because of this, external buffers are not needed unlike in SRAMs with common I/O. Figures 3-8a and 3-8b show the microinstruction store implementation using common I/O and separate I/O SRAMs respectively.

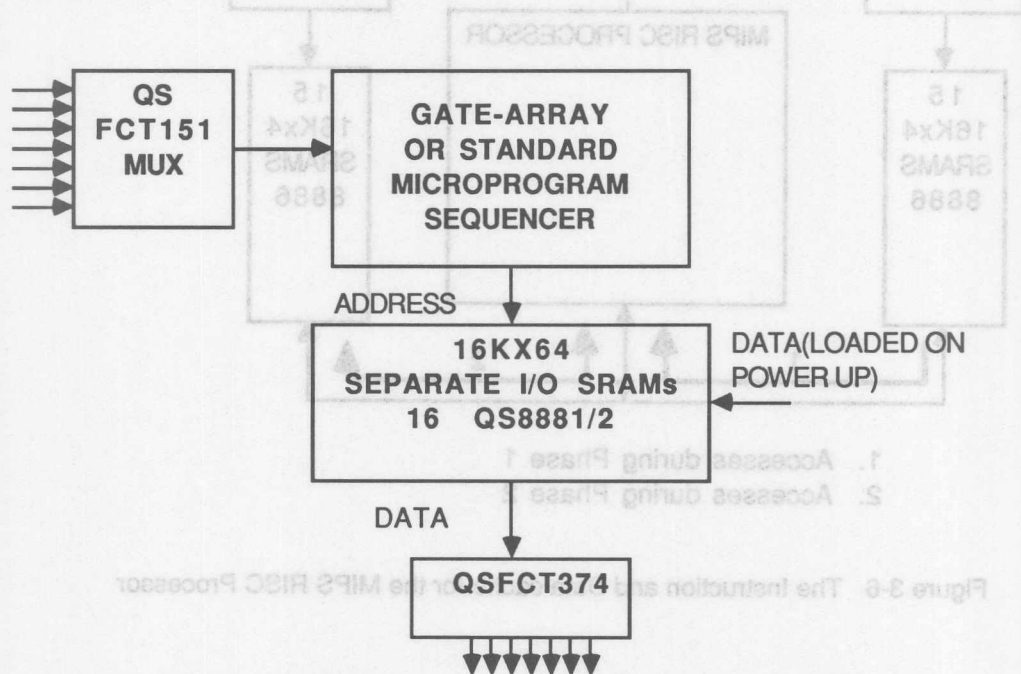


Figure 3-7: An Implementation of Microinstruction Store

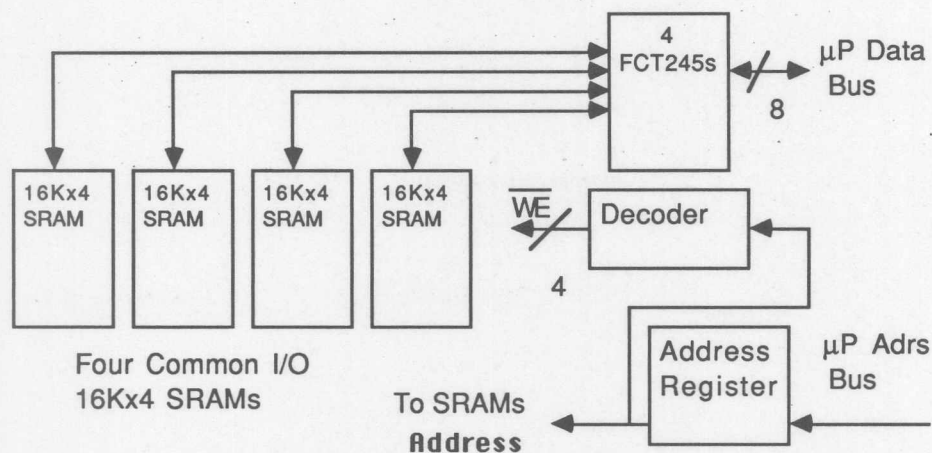


Figure 3-8a Implementation of Microinstruction Store Using Common I/O SRAMs

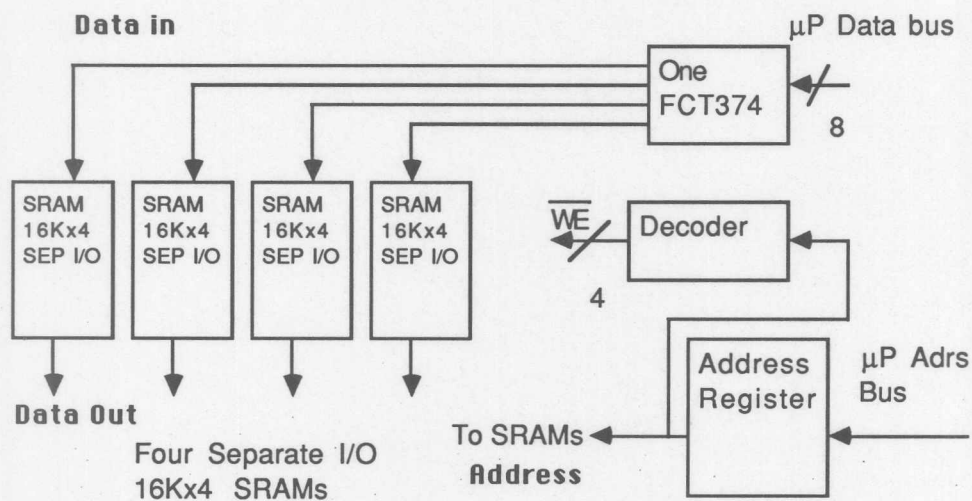


Figure 3-8b Implementation of Microinstruction Store With Separate I/O SRAMs

The SRAMs in this application are in the critical path for the overall cycle times. The applications generally require 15 ns to 35 ns SRAM access time. Separate I/O RAMs are also used for data caches and memory mapping SRAMs.

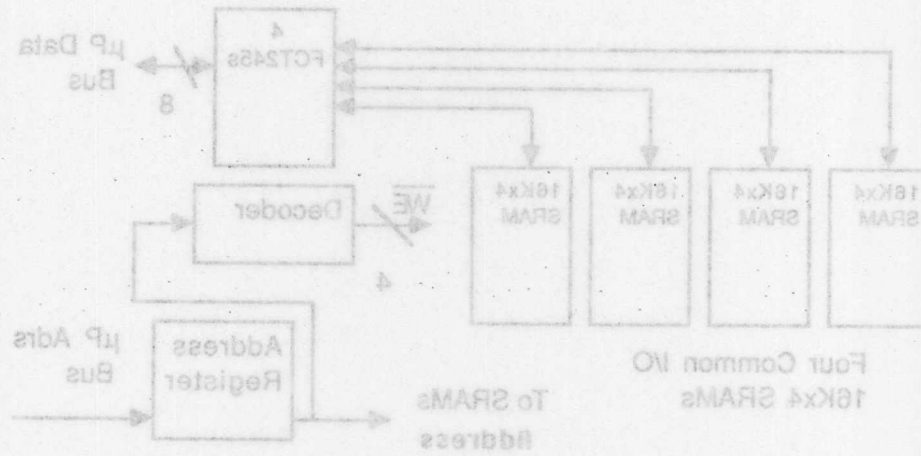


Figure 3-8a Implementation of Microinstruction Store Using Common I/O SRAMs

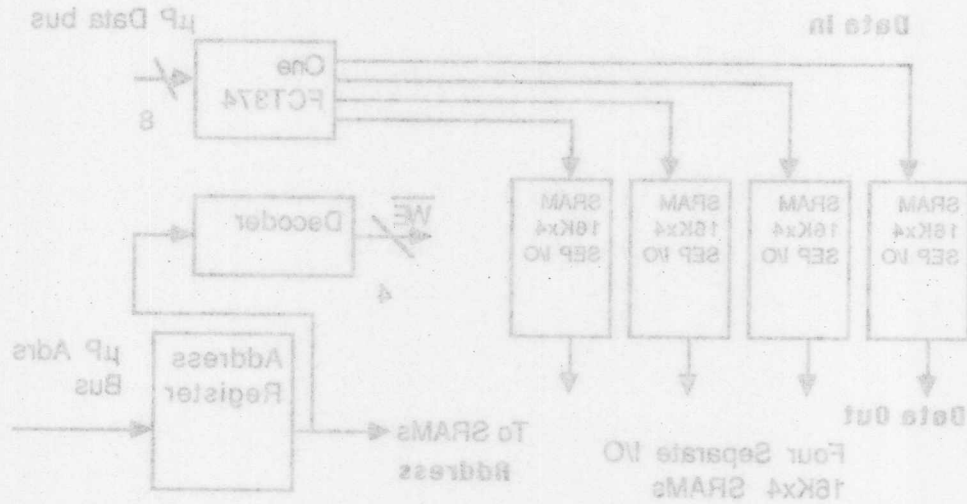


Figure 3-8b Implementation of Microinstruction Store With Separate I/O SRAMs

The SRAMs in this application are in the critical path for the overall cycle times. The applications generally require 15 ns to 25 ns SRAM access time. Separate I/O RAMs are also used for data caches and memory mapping SRAMs.

Q

ZIP Packages for Logic Provide High Density and High Speed

**Application
Note
AN-06**

by
David Wyland

ZIP packages for high speed logic such as the FCT family provide high packing density in a through-hole package coupled with superior speed and ground bounce performance. ZIP packages provide density improvements of almost 2X over DIP packages and 1.2X over SOIC packages. In addition, they provide a low ground inductance package which allows high speeds with much lower ground bounce noise than DIP packages.

ZIP packages are not new. Millions of DRAMs in ZIP packages have been shipped over the last few years. Recently, however, the advantages of ZIP packages for high speed logic have been discovered. QSI introduced ZIP packaging for their FCT line of fast TTL logic. In addition to the expected benefits of high board density in a through hole package, the additional benefits of high speed with superior ground bounce noise performance were provided.

ZIP For Density

The density comparison between the ZIP, DIP, and SOIC for 20-pin packages can be seen in Figure 1. A 300 mil DIP requires approximately 400 mils of board width to allow for the pads. This results in a board area of 0.400 square inches. The equivalent ZIP requires only 200 mils of width but an additional 50 mils of length to compensate for the staggered leads for a board area of 0.21 square inches. The area ratio is $0.40/0.21 = 1.90$ X improvement in area.

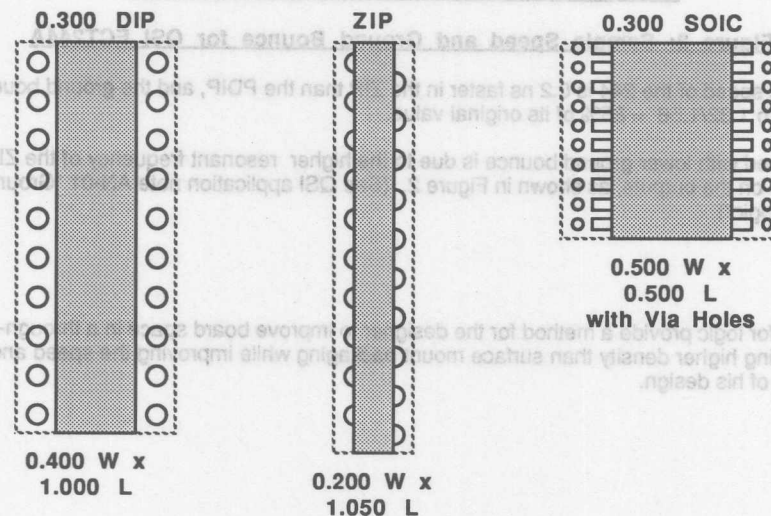


Figure 1: Board Footprints of ZIP, DIP, and SOIC

The SOIC requires only 0.400 by 0.500 for the basic footprint for a total of 0.20 square inches, the same as the ZIP. In reality, however, via holes are required to communicate between the SOIC leads on the surface of the board and the internal and back layers of the board. Via holes are provided free in through-hole DIP and ZIP packages. These holes and their associated pads add another approximately 50 mils to each side of the 400 mils of width. This results in a footprint of 0.500 by 0.500 for 0.25 square inches. The area ratio is $0.25/0.21 = 1.19$ X improvement in area of the ZIP over the SOIC.

ZIP For Speed with Low Ground Bounce Noise

ZIP packages are faster than DIP for TTL logic because the ZIP package has lower ground lead inductance. FCT in ZIP packages with the same pin numbering as the DIP results in the ground lead (pin 10 in a 20 pin package) being in the middle of the package, the shortest lead. As a result, the ZIP has less ground bounce noise than the DIP for the same chip. Figure 2 shows a table which compares FCT244A drivers in both DIP and ZIP packages.

Parameter	QSI FCT 244A		Units
	PDIP	ZIP	
Tphl 7 Outputs Switching	4.10	3.90	ns
Volp (Ground Bounce)	1.56	1.32	Volts
Package Resonance @ 50 pF/Output	72	120	mHz

Figure 2: Sample Speed and Ground Bounce for QSI FCT244A

In Figure 2, the speed of the 244 is 0.2 ns faster in the ZIP than the PDIP, and the ground bounce has been reduced to $1.32/1.56 = 85\%$ of its original value.

The higher speed with lower ground bounce is due to the higher resonant frequency of the ZIP package for 50 pF loads on the outputs, as shown in Figure 2. (See QSI application note AN-01 "Ground Bounce Noise in TTL Logic")

Conclusion

ZIP packages for logic provide a method for the designer to improve board space in a through-hole design, achieving higher density than surface mount packaging while improving the speed and noise characteristics of his design.

Q

Resistor Output Logic Gives High Speed with Low Noise

Application
Note
AN-07

by
David Wyland

Resistors on the outputs of TTL logic gates have long been used as a technique to damp board reflection noise. These resistors are typically approximately 25Ω in value, an empirical value giving the best noise reduction with minimal loss in speed. With the advent of very high speed TTL logic such as FCT and the desire to eliminate the board space required by the 25Ω resistor package, there has been a need for logic parts that incorporate the 25Ω resistor on the silicon. QSI has responded to this need by introducing the FCT2000 logic series which provides 25Ω resistor output options for virtually all of the devices in the FCT family. A block diagram of the FCT2000 series is shown in Figure 1.

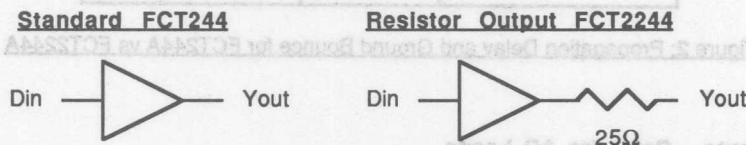


Figure 1: 2000 Series Resistor Output Logic

Resistor Output Logic - Putting the Resistor On the Silicon

The technique of adding resistors to logic was so common in applications such as high speed drivers for DRAM arrays that logic parts with 25Ω outputs were introduced as early as the 1970's in devices such as the Am2965/66, the 25Ω equivalent of the 74S240/244 octal drivers. Since that time, resistor output parts have been added in piecemeal fashion to a variety of logic parts in a variety of families.

Resistor output parts are quite simple in concept: a 25Ω resistor is added to each active output. This is shown in Figure 1. The advantages of including it in the IC are the savings in board space and the fact that the composite circuit of IC plus resistor is specified for speed and DC parameters.

The QSI FCT2000 Series: Low Noise Without Loss of Speed

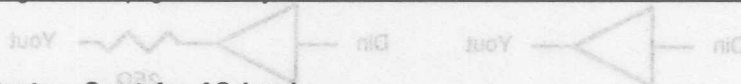
The QSI FCT2000 series is designed to help the designer by providing resistor equivalents of standard parts which have the same speed ratings. For example, the QSI FCT2000 resistor series parts meet the same propagation delay specifications as their non-resistor equivalents in the A and non-A speed grades. This allows a designer to substitute a resistor part for a standard part to reduce system noise without suffering a speed penalty.

Adding Resistors: Full Speed Without Ground Bounce

Adding resistor outputs can produce dramatic reduction in ground bounce noise and system noise. The table in Figure 2 compares resistor and non-resistor parts for speed and ground bounce. The resistor part is 0.30 ns slower than the non-resistor part for the full 50 pF load; however, the ground bounce has been reduced from 1.56 volts to 0.80 volts. The resistor ground bounce is 51% of its original value for a 7% increase in propagation delay.

Parameter	FCT244A	FCT2244A	Units
Tphl 7 Outputs Switching	4.10	4.40	ns
Volp (Ground Bounce)	1.56	0.80	Volts

Figure 2: Propagation Delay and Ground Bounce for FCT244A vs FCT2244A

**Resistor Outputs - Great for AC Loads**

Resistor outputs sacrifice DC drive for improved AC noise. Because of the 25Ω resistor at the output, a 0.50V Vol can be met at only 12 mA rather than 64 mA. This is a problem only if driving a DC terminated backplane or transmission line. However, in the common application of driving local, unterminated buses such as on PC cards, this does not represent a problem. The 64 mA capability is still there to provide the transient AC drive. The actual requirement is that the speed be there and the noise be gone for real loads.

Conclusion

Resistor output parts have become a sub-family of logic in the industry. They have come into existence because of the invention of system designers solving system speed and noise problems. The simple addition of a resistor to the output of a logic driver can provide dramatic reduction in noise with a small penalty in speed. Providing the resistor in the logic IC allows its operation with the resistor to be specified and tested. The result is a powerful and useful tool for the designer to allow the achievement of speed with reliability.



QSOP Packages Provide High Density in 32-Bit Bus Designs

Application
Note
AN-08

by
David Wyland

QSOP (Quarter Size SOIC Outline Package) packages for high speed logic such as the FCT family provide 2.5 to 3 times the packing density of the SOIC packages they replace. QSOPs in bus designs provide the highest board density, higher than any other package including gate arrays in PQFP. This results in significant savings in board space and trace delay in 32-bit bus systems common in high speed RISC and CISC designs.

The QSOP package is a new package based on a standard JEDEC outline. The QSOP is called Quarter Size because it is approximately one half the length and one half the width of its corresponding SOIC package. This is done by combining a double density, 25 mil leadframe with a JEDEC standard 14 pin, 150 mil SOIC body. The result is a package that is 340 mils long and 235 mils wide versus 600 mils long and 406 mils wide for a 24 pin, 300 mil SOIC. Although significantly smaller, the QSOP can use the same handling equipment as the existing 14-pin, 150 mil SOIC. Also, its 25 mil lead spacing poses no more problems than existing 25 mil QFP packages.

The space savings provided by the QSOP are significant, particularly in 32-bit and 36-bit bus applications. Table 1 shows the relative area used by QSOP, SOIC, TI Widebus™ and PQFP gate array solutions to connecting two 32-bit and 36-bit buses with transceivers. (Note that there is no current 18-bit part currently available for the 36-bit Widebus™ case. Availability of an 18-bit is assumed for comparison purposes only, rather than using additional packages to make up the 36 bits.)

Table 1: Board Area for 32-bit and 36-bit Bus Transceivers

	QSOP	SOIC	Widebus™	PQFP	PQFP
Bits	32	32	32	32	64
Pins/Package	20	20	48	84	160
Number Pkgs	4	4	2	1	1
Pins, Total	80	80	96	84	160
Length, mils	342	500	600	780	1255
Width, mils	235	406	406	780	1255
Area/Pkg, Sq Mils	80,370	203,000	243,600	608,400	1,575,025
Total Area	321,480	812,000	487,200	608,400	1,575,025
Relative Area	1.00	2.53	1.52	1.89	2.45
Bits	36	36	36	36	72
Pins/Package	24	24	24	100	200
Number Pkgs	4	4	4	1	1
Pins, Total	96	96	96	100	200
Length, mils	342	600	600	880	1252
Width, Total	235	406	406	880	1252
Area, Sq Mils	80,370	243,600	243,600	774,400	1,567,504
Total Area	321,480	974,400	985,768	774,400	1,567,504
Relative Area	1.00	3.03	1.52	2.41	2.44

The QSOP requires the least area of the four. The next smallest package, the TI Widebus™, requires 1.52 times as much board space. What is more interesting is that the equivalent gate array solution in the smallest practical Quad Flat Pack (QFP) package requires 1.89 times as much area for 32-bit buses and 2.41 times the area for 36-bit buses. Doubling the bus to 64 or 72 bits makes the situation worse. A 64-bit or 72-bit gate array in PQFP requires 2.44 times the area of that required by the equivalent 8 QSOPs.

QSOPs Provide Higher Density Than Gate Arrays

A QSOP design uses approximately half the board area of a gate array design.

At first, it may seem surprising that the QSOP provides higher density than an equivalent gate array in a high density PQFP package. This goes against current conventional wisdom. Gate arrays do provide high density for logic functions, such as PC chip sets which combine the logic for several packages into one gate array. This eliminates pins, packages and board area.

When two buses must be connected, however, the pins cannot be eliminated. Two 32-bit buses require 64 pins to connect them, plus power, ground and control signals. This adds up to approximately 80 pins. The question then becomes how to most efficiently put these 80 pins on a board. The QSOP collects these pins in four groups of 20 with each group of 20 in two closely spaced rows of 10 pins on 25 mil centers. The PQFP places these 80 pins around the perimeter of a square. The problem is that the area of this square goes up as the square of the number of pins. Doubling the number of pins increases the board area by a factor of four, not two. This is why the increasing the size of the PQFP makes the problem worse, not better.

An additional advantage of the QSOP approach is that the parts are already designed. Not only designed, but available. Over 70 FCT parts are immediately available in the QSOP package, including the fastest speed C and D grades and the FCT2000, 25Ω output series for high speed with low noise.

FCT In QSOP Solves Board Area, Trace Delay and Noise Problems

The designer of high speed 32-bit RISC or CISC systems has a problem. Address drivers and data transceivers are required to drive RAM and I/O buses. These transceivers require significant board area, even when packaged in SOIC. Using a gate array does not solve the problem; it makes it worse. In addition, the board area required by these parts increases trace length on the PC board causing trace delay and ringing. At 150-200 picoseconds per inch, it does not take very many inches of trace to add significant delay to a 33 to 50 mHz design. By minimizing the board area required for bus control, the QSOP can make the overall design smaller, faster, and lower in noise.

Because the QSOP package is small, it provides logic parts such as the FCT family with higher speed and lower ground bounce due to its lower lead inductance. Also, the FCT2000 series with 25Ω outputs is also available in the QSOP package for noise critical high speed applications. The internal 25Ω resistors in the FCT2000 parts save board space. In fact, adding an external SOIC resistor pack would require almost three times as much additional area as the QSOP itself!

QSOP - The Choice for High Density Designs

QSOP packages significant provide reduction in board space, trace delay and noise for high speed RISC and CISC designs as well as for high density designs such as laptop and notebook PC's. Because of its clear advantages and the availability of a full family of parts in the package, the QSOP will become the package of choice for advanced designs in the 90's.

Q

CMOS Bus Switches Provide Zero Delay Bus Communication

Application
Note
AN-09

by
David Wyland

The 74QST3383 and 74QST3384 CMOS Bus Switches by Quality Semiconductor are high speed TTL bus connect devices. When they are enabled, the bus switches directly connect two buses with a connection resistance of less than 5Ω . They are like a 5 nanosecond multi-pole relay for TTL signals with an on resistance of 5Ω . Since these devices directly connect the bus signals they introduce no additional propagation delay, timing skew or noise. They are also inherently bidirectional and dissipate no additional power. They can replace traditional TTL buffers and transceivers to reduce propagation delay, noise, control complexity and power dissipation.

A block diagram of the 74QST3384 CMOS Bus Switch is shown in Figure 1. This device consists of ten switches arranged as two banks of five. This allows the 3384 to be used as a 10-bit switch or as a 5-bit, 2-to-1 multiplexer. A block diagram of the 74QST3383 CMOS Bus Exchange Switch is shown in Figure 2. This device consists of two banks of ten switches arranged to gate through or exchange two banks of five signals. This allows the 3384 to be used as a 10-bit switch or as a 5-bit, two way bus exchange device. This part is particularly useful for exchange and routing operations such as byte swap, crossbar matrices, and RAM sharing.

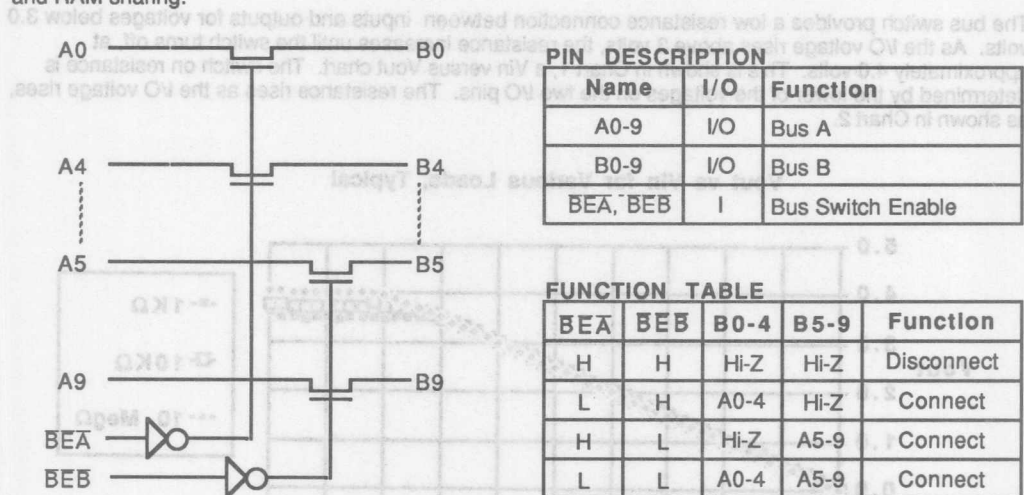


Figure 1: 74QST3384 CMOS Bus Switch Block Diagram

Each switch consists of an N channel MOS transistor driven by a CMOS gate. When the switch is enabled, the gate of the N channel transistor is at V_{cc} (+5 volts) and the device is on. These devices have an on resistance of less than 5Ω for voltages near ground and will drive in excess of 64 mA each. The resistance rises somewhat as the I/O voltage rises from a TTL low of 0.0 volts to a TTL high of 2.4 volts. In this region the A and B pins are solidly connected, and the bus switch is specified in the same manner as a TTL device over this range. As the I/O voltage rises to approximately 4.0 volts, the transistor turns off. This corresponds to a typical TTL high of 3.5 to 4.0 volts.

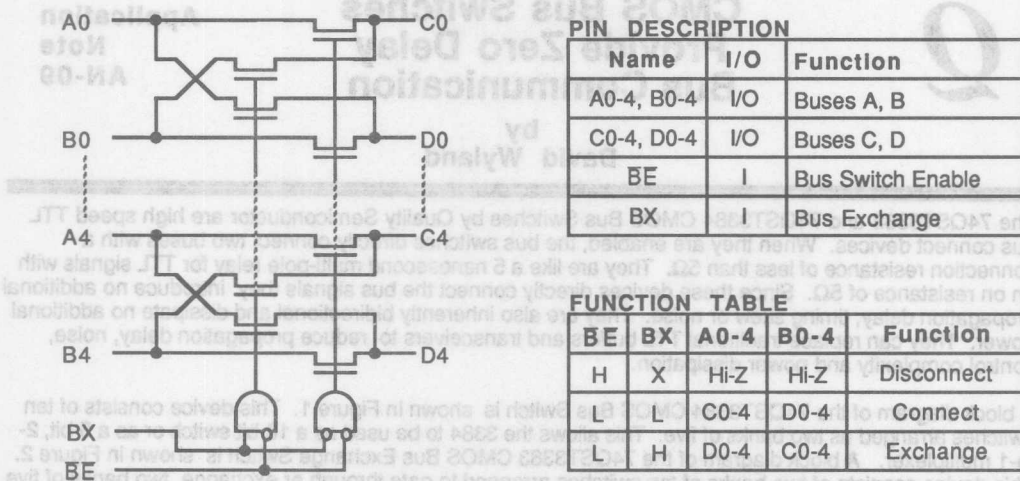


Figure 2: 74QST3383 CMOS Bus Exchange Switch Block Diagram

The bus switch provides a low resistance connection between inputs and outputs for voltages below 3.0 volts. As the I/O voltage rises above 3 volts, the resistance increases until the switch turns off, at approximately 4.0 volts. This is shown in Chart 1, a V_{in} versus V_{out} chart. The switch on resistance is determined by the lower of the voltages on the two I/O pins. The resistance rises as the I/O voltage rises, as shown in Chart 2.

Vout vs Vin for Various Loads, Typical

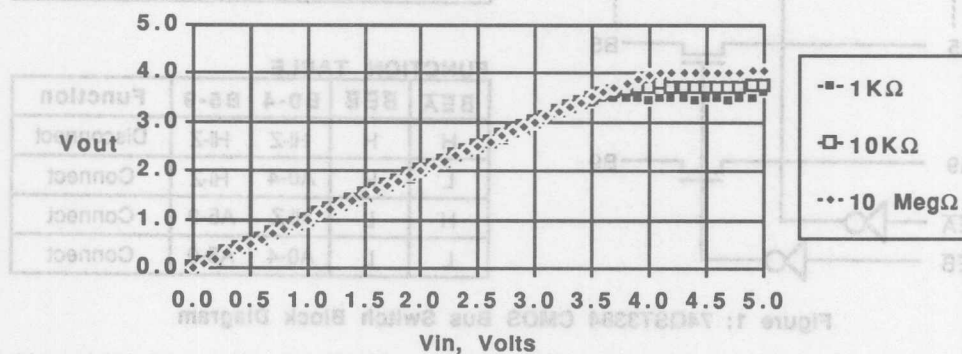
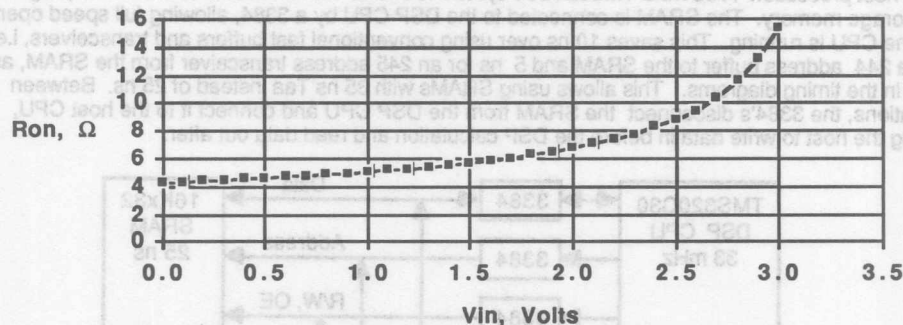


Chart 1: Vout vs Vin

On Resistance vs V_{in} @ 4.75 Vcc

Chart 2: Switch On Resistance vs V_{in}

The bus switch provides a path for a driving device to drive capacitance to ground and to drive capacitance up from ground. This is shown in Figure 3. When the A (or B) input is driven to a TTL low of 0.0 volts, the N channel transistor is fully on and the B (or A) output will follow it. Likewise, when the A (or B) input is driven from a TTL low of 0.0 volts to a TTL high, the capacitor side of the N channel switch is at 0.0 volts, the switch is fully on and the B (or A) output will follow it through threshold and beyond. This means that the rise and fall time characteristics and waveforms of the B (or A) output will be determined by the TTL driver, not the bus switch. The switch introduces no propagation delay, to a first approximation.

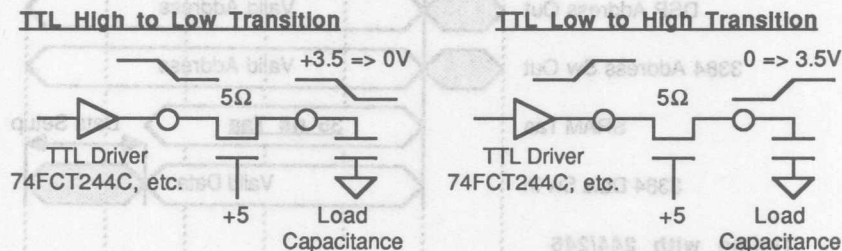


Figure 3: CMOS Bus Switch Operation

When the bus switch is disabled, the N channel transistor gate is at 0.0 volts, and the transistor is off. By the nature of the N Channel transistor design, the A and B pins are fully isolated when the transistor is off. Leakage and capacitance is to the chip substrate (i.e., ground) rather than between input and output. This minimizes feedthrough in the off state. Because only an N channel transistor is used, either A or B pin(s) can be taken to Vcc and above, and the device can be powered down without loading either bus.

The bus switch can replace drivers and transceivers in systems if bus repowering is not required. Since the bus switch directly connects two buses, it provides no drive of its own but relies on the device that is driving data onto the connected buses. If the additional loading of the connected bus is small enough, there is a net gain in speed. For example, the sensitivity to loading of a driver such as the 74FCT244 is typically 2 ns/100 pF. If the connected bus adds 50 pF of loading the added delay will be 1 ns. This is much less than the 4 to 10 ns delay of the buffer or transceiver the bus switch replaces.

Microprocessor Shared Memory Connect for Slave Processor

Figure 4 shows the 3384 bus switch used to allow the memory for a DSP slave processor to be accessed by the host processor. A 33 mHz TMS320C30 system is shown with a 16Kx32 SRAM as its program and data storage memory. The SRAM is connected to the DSP CPU by a 3384, allowing full speed operation while the CPU is running. This saves 10 ns over using conventional fast buffers and transceivers, i.e. 5 ns for a 244 address buffer to the SRAM and 5 ns for an address transceiver from the SRAM, as shown in the timing diagrams. This allows using SRAMs with 35 ns Taa instead of 25 ns. Between calculations, the 3384's disconnect the SRAM from the DSP CPU and connect it to the host CPU, allowing the host to write data in before the DSP calculation and read data out after.

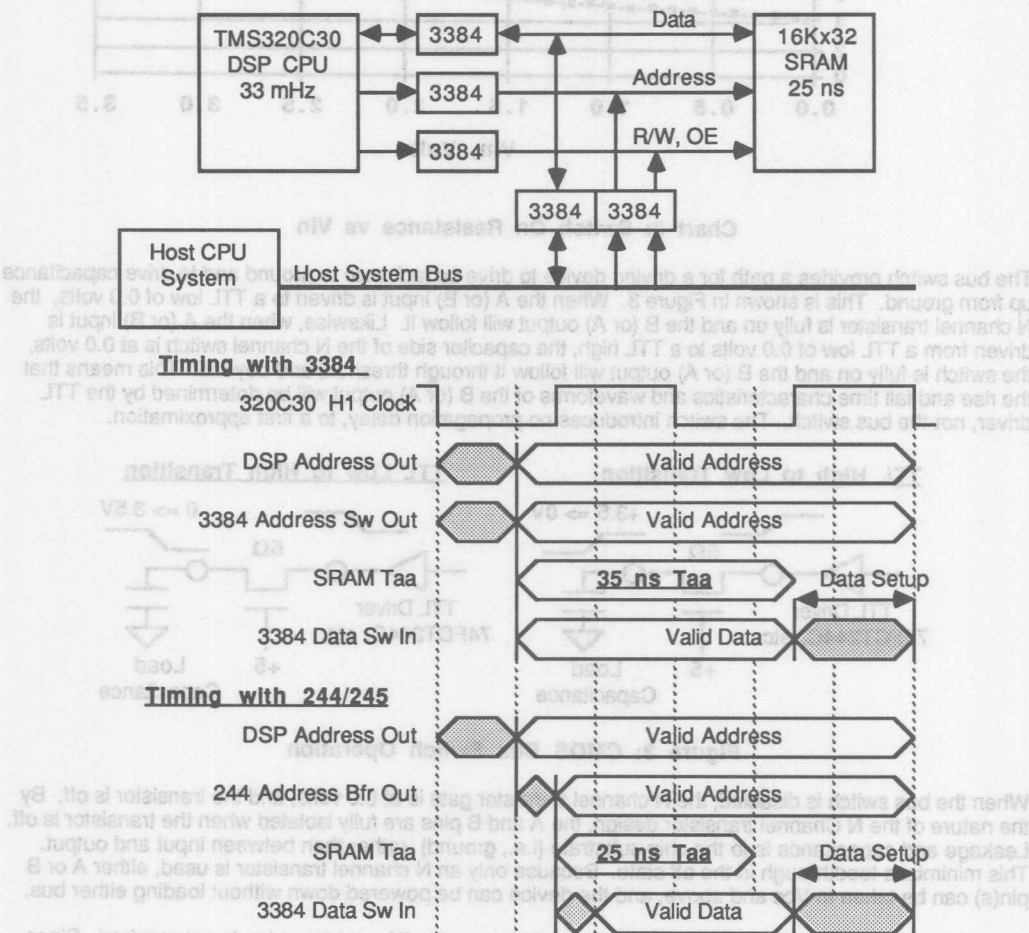


Figure 4: 74QST3384 as DSP Shared Memory Connect

Multiprocessor System Fast Bus Connect

Figure 5 shows the 3384 bus switch used as a fast bus connect in a high performance multiprocessor system. Four 32-bit processors are shown, each with its own cache or other local memory. Each processor is connected by a 3384 bus switch to a 1 meg x 32, 25 ns cycle time fast SRAM main memory. The 3384 is used to connect the address, data, and control lines of the SRAM directly to each processor. When one of the 3384's is active, the main memory appears as a simple SRAM to the connected CPU. This provides a simple, very fast interface with no additional delays for buffers or data direction logic and no timing skew in the control signals.

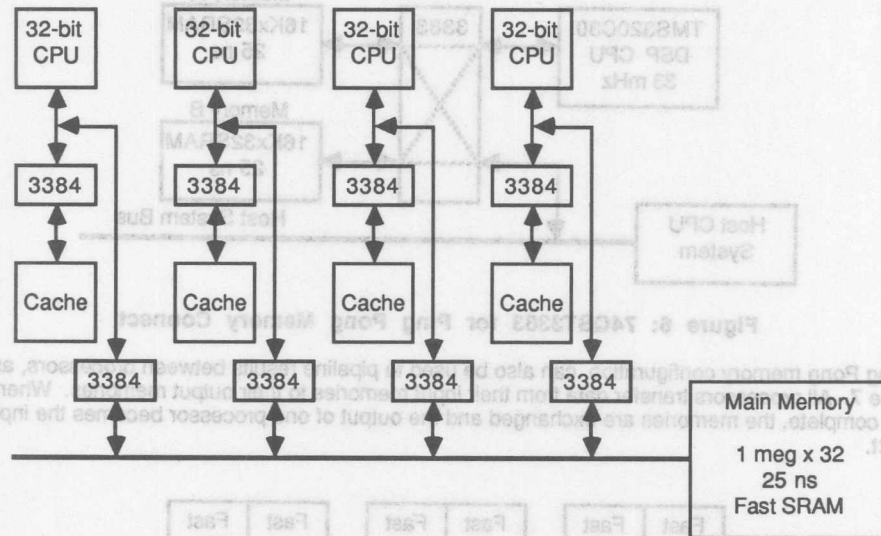


Figure 5: 74QST3384 as Multiprocessor System Bus Connect

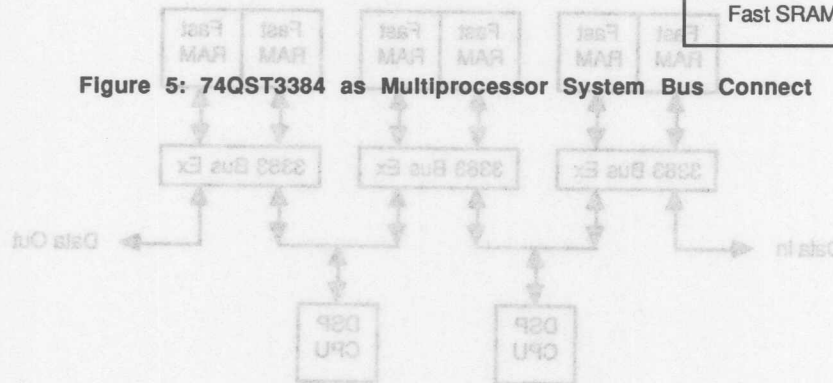


Figure 7: 74QST3383 for Ping Pong Pipeline Memory

Bus Exchange Switch for Ping Pong Memory Connect

Figure 6 shows the 3383 bus exchange switch used to connect two memories to a DSP processor and a host CPU bus. The 3383 connects Memory A to either the DSP or host CPU, and Memory B to the host CPU or DSP CPU, respectively, depending on the state of the bus exchange control. This configuration allows the host CPU to be accessing one memory for loading program and data or retrieving results while the DSP CPU is running out of the other memory. When the calculation is complete, the memories are exchanged, and the DSP CPU can continue with another calculation while the results of the last one are accessed. This configuration allows both high speed and high throughput.

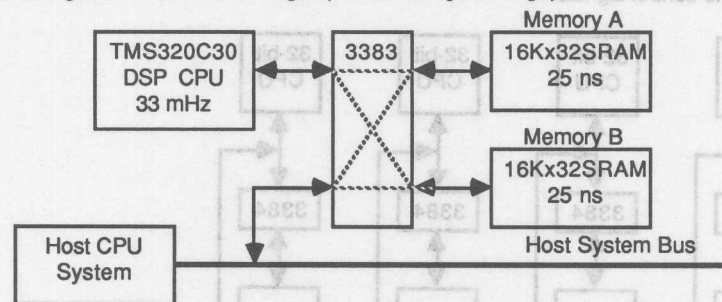


Figure 6: 74QST3383 for Ping Pong Memory Connect

The Ping Pong memory configuration can also be used to pipeline results between processors, as shown in Figure 7. All processors transfer data from their input memories to their output memories. When one pass is complete, the memories are exchanged and the output of one processor becomes the input of the next.

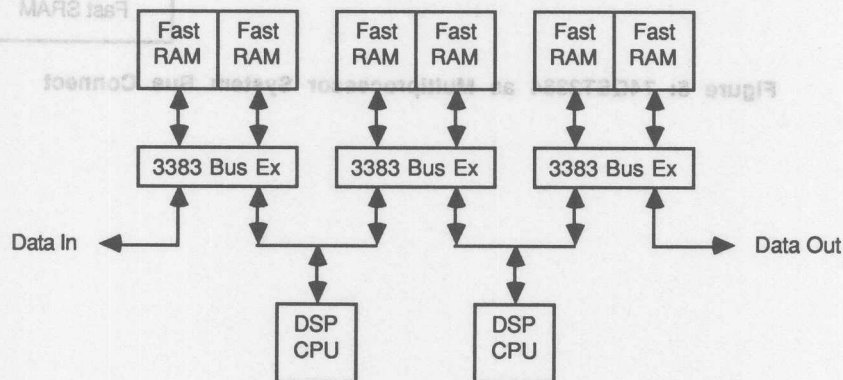


Figure 7: 74QST3383 for Ping Pong Pipeline Memory

Bus Exchange Switch for Crossbar Systems

Figure 8 shows the 3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration. In this configuration, any CPU can be connected to any memory. If there is no conflict by two CPUs for the same memory, any valid combinations of CPU and memory can be made by appropriate selection of the 3383 controls. Two layers of 3383 bus exchange switches are required for this four-way crossbar. Three layers will be required for an 8-way crossbar, etc.

The 3383 bus exchange switch is ideal for crossbar work because it introduces no delay of its own. A 16-way crossbar with four layers of switches adds little or no delay over direct connection of the RAM to the CPU. Also, the CPU sees a simple RAM interface without the complicated timing skew requirements which might be imposed by using bus transceivers instead of 3383 switches.

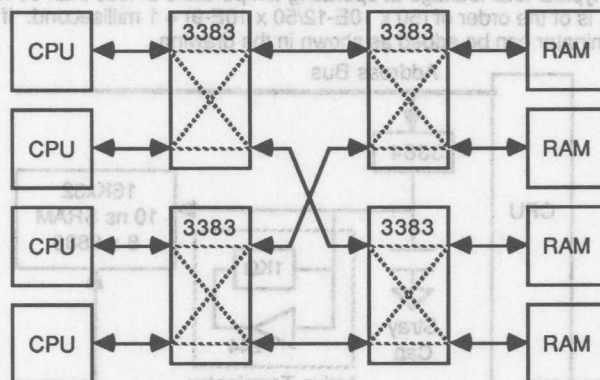


Figure 8: 74QST3383 Crossbar Switch

Bus Exchange Switch for Bus Byte Swap and Barrel Shift

A scheme similar to the one shown in the diagram of Figure 8 can also be used to provide byte swap capability between a CPU and memory. This is useful in systems where big-endian and little-endian byte orders are mixed within the same system. If the CPU and RAM blocks of figure 8 are interpreted as bytes of a CPU and memory bus respectively, the crossbar switch scheme shown allows any combination of byte swapping or shifting desired without introducing any additional propagation delay or control considerations. If this concept is extended to the bit level, a barrel shifter results.

Fast Address Latch

Figure 9 shows the 3384 bus switch used as a fast address latch in an SRAM memory subsystem. In this system, the 3384 connects the SRAM to the address bus, which drives the stray capacitance of the SRAM array. When the 3384 turns off, the stray capacitance holds the TTL level. The advantage of using the 3384 instead of a fast latch such as the 74FCT373 is that the effective throughput delay is much less. The delay caused by the additional 50 pF load on the address bus may be 1 ns as compared to 4 ns for the fastest latch. Also, the 3384 does not introduce additional noise.

The hold time for typical capacitances and leakages can be quite long compared to the clock cycle times of fast systems. For the 16Kx32 configuration of eight 16Kx4 SRAMs shown, the stray capacitance is of the order of 50 pF. The turn off transient of the 3384 will typically be less than 50 millivolts. Assuming a 1 volt change in level and a typical total leakage at operating temperature of less than 50 nanoamperes, (SRAMs + 3384), the hold time is of the order of $(50 \times 10^{-12} / 50 \times 10^{-9}) = 1$ millisecond. If an indefinite hold is desired, an active terminator can be added as shown in the drawing.

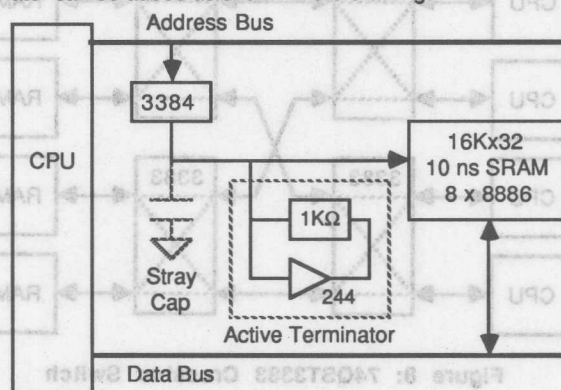


Figure 9: 74QST3384 Fast Address Latch

A scheme similar to the one shown in the diagram of Figure 8 can also be used to provide byte swap capability between a CPU and memory. This is useful in systems where big-endian and little-endian byte orders are mixed within the same system. If the CPU and RAM blocks of Figure 8 are interpreted as bytes of a CPU and memory bus respectively, the crossover switch scheme shown allows any combination of byte swapping or shifting desired without introducing any additional propagation delay or control considerations. If this concept is extended to the bit level, a parallel shifter results.

ATE Load Switch

Figure 10 shows the 3384 bus switch used as a load switch for an automated test equipment (ATE) load board. ATE equipment requires custom design of the load board (i.e. electrical test fixture) for a given device to be tested. A common problem to be solved is the connection and disconnection of load resistor network to each pin of the device under test (DUT). The load must be connected during parts of the test and disconnected during other parts. This connection is typically done with small relays because of their low on resistance. However, relays are large and slow. The 3384 bus switch can replace up to 10 relays in this application, in a smaller package, and with an actuation time of 6 nanoseconds rather than 5 milliseconds. This can significantly speed up test time.

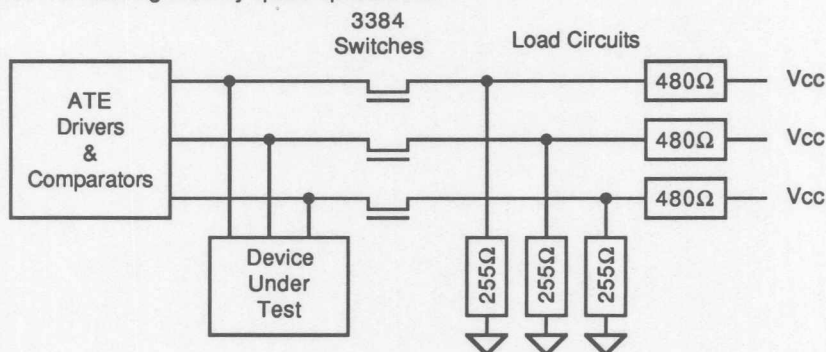


Figure 10: 74QST3384 ATE Load Switch

Conclusion

The 74QST3383 and 3384 bus switches are new tools for the system designer. They can be used to reduce propagation delay and to create high speed systems with simplified interfaces, improved timing margins and reduced noise.

ATE Load Switch

Figure 10 shows the 3384 bus switch used as a load switch for an automated test equipment (ATE) load board. ATE equipment requires custom design of the load board (i.e. electrical test fixture) for a given device to be tested. A common problem to be solved is the connection and disconnection of load resistor network to each pin of the device under test (DUT). The load must be connected during parts of the test and disconnected during other parts. This connection is typically done with small relays because of their low on resistance. However, relays are large and slow. The 3384 bus switch can replace up to 10 relays in this application, in a smaller package, and with an actuation time of 5 nanoseconds rather than 5 milliseconds. This can significantly speed up test time.

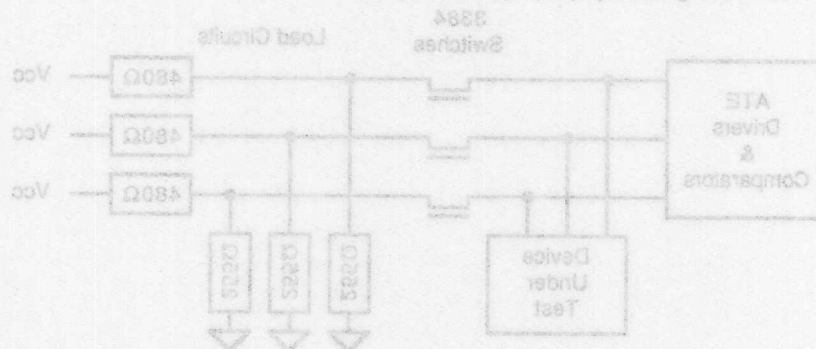


Figure 10: 74023384 ATE Load Switch

Conclusion

The 74023383 and 3384 bus switches are new tools for the system designer. They can be used to reduce propagation delay and to create high speed systems with simplified interfaces, improved timing margins and reduced noise.

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Quality and Reliability Program

QUALITY AND RELIABILITY PROGRAM

- The technology enables the assembly of any number of different configurations
- Detect failures are low enough to allow efficient and economical manufacturing
- Circuit design and layout rules have sufficient margins

Quality and Reliability Operation Overview

At Quality Semiconductor Inc., we are committed to maintaining the highest possible standards of quality and reliability in our products. We do not merely screen for quality -- we design our products for quality and reliability. We consider our quality/reliability goals met when customers are satisfied with our products.

We achieve high standards of quality and product excellence by using better materials, controls and designs. This translates to building quality into the product from its inception.

We use three quality enhancement techniques: (1) We build product reliability into each design, and every employee is responsible for ensuring we attain such reliability; (2) We build product quality into all stages of the manufacturing process through strict inspections of incoming materials and conformance checks after critical process steps. We monitor all processes to ensure they adhere to specifications; (3) After burn-in, we perform stringent inspections and reliability conformance checks on products to ensure they meet final product quality requirements.

Quality and Reliability in the Design Stage

Our development philosophy maintains a team effort among design, layout, technology, package, testing and product engineers who are involved throughout the product cycle.

The Quality and Reliability organization is ultimately responsible for assuring our products meet established standards. This group supervises fabrication techniques, assembly processes, packages and product designs.

At QSI we are expert in fabrication process reliability, assembly/process/package reliability and product reliability. All development group team members address quality and reliability issues early in the development cycle. Our goal is to build a product to the highest possible standard and to satisfy our customers.

Our Technology Development and Production Engineering groups work as a team from the early development stage to ensure a smooth transition of technology into production. The development activity begins with the need for a higher speed product at small die sizes, or a reduced die size product or even a new product. To transfer a process to production requires that the process be capable of meeting the performance, cost-effectivity and manufacturability targets. To satisfy these goals, the Technology Development group balances many variables to produce fabrication technology. QSI's Process Reliability group scales geometries in the quest for higher speed products, simultaneously ensuring the technology is inherently reliable.

Quality and Reliability Program

To guarantee reliable operation throughout the lifetime of the product, the following must be true:

- The technology ensures the absence of any intrinsic wearout mechanisms
- Defect densities are low enough to allow efficient and economical manufacturing
- Circuit design and layout rules have sufficient margins

Our Package Development team satisfies the constant demand for newer packages and assembly processes. The performance requirements for newer packages and assembly processes are very complex. As we push performance limits, the electrical parasitics of a package can impact the overall device specification. The team carefully selects packages to meet the increased speed requirements. Our Package Reliability and Technology Development teams share a common goal: to produce a reliable, manufacturable product that meets the customers' need for functionality, performance and cost.

QSI's Production Engineering team ensures the functionality and performance targets have been met. This team concentrates on all the above-mentioned areas, especially design and test. Extensive test programs excite every node in the device to ensure excellent fault coverage. The team resolves product yields and performance issues and handles product failure analysis. Production Engineering provides feedback to other QSI teams and to customers on any detected failure mechanisms. The team immediately implements a corrective action procedure to remedy the problem.

Product Testing Categories

Quality Semiconductor uses MIL-STD-883 to determine test methods, procedures and specifications. Thus, our customers purchase commercial devices that receive military patterned process flow at no additional cost.

At QSI, we offer three distinct testing categories:

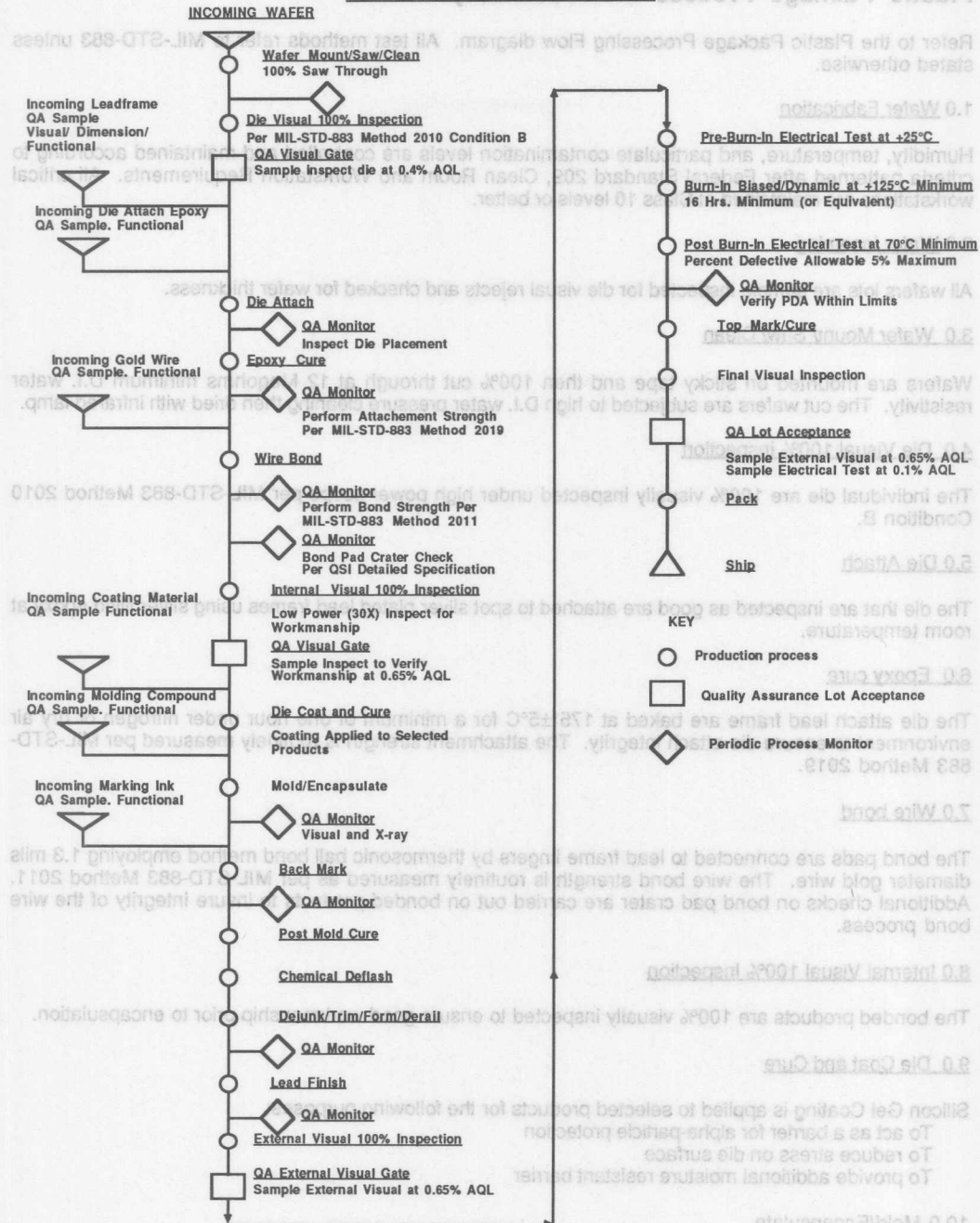
- 1) Commercial operating range 0°C to +70°C.
- 2) Military Grade product processed to MIL-STD-883 and operating from -55°C to +125°C.
- 3) SMD (Standard Military Drawing) approved product; Military operating range; -55°C to +125°C, electrical tested per the applicable Military drawing.

Flow Charts

The Commercial Test Flow Charts are shown on the following pages. Detailed process flows for plastic and hermetic packages are discussed.

Quality and Reliability Program

PLASTIC ASSEMBLY FLOW



Quality and Reliability Program

Plastic Package Process Flow Summary

Refer to the Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless stated otherwise.

1.0 Wafer Fabrication

Humidity, temperature, and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 10 levels or better.

2.0 Wafer Incoming

All wafers lots are sample inspected for die visual rejects and checked for wafer thickness.

3.0 Wafer Mount/ Saw/ Clean

Wafers are mounted on sticky tape and then 100% cut through at 12 Megohms minimum D.I. water resistivity. The cut wafers are subjected to high D.I. water pressure cleaning then dried with infrared lamp.

4.0 Die Visual 100% inspection

The individual die are 100% visually inspected under high power scope per MIL-STD-883 Method 2010 Condition B.

5.0 Die Attach

The die that are inspected as good are attached to spot silver plated lead frames using silver filled epoxy at room temperature.

6.0 Epoxy cure

The die attach lead frame are baked at $175^{\circ}\pm 5^{\circ}\text{C}$ for a minimum of one hour under nitrogen or dry air environment to ensure die attach integrity. The attachment strength is routinely measured per MIL-STD-883 Method 2019.

7.0 Wire bond

The bond pads are connected to lead frame fingers by thermosonic ball bond method employing 1.3 mils diameter gold wire. The wire bond strength is routinely measured as per MIL-STD-883 Method 2011. Additional checks on bond pad crater are carried out on bonded products to insure integrity of the wire bond process.

8.0 Internal Visual 100% Inspection

The bonded products are 100% visually inspected to ensure good workmanship prior to encapsulation.

9.0 Die Coat and Cure

Silicon Gel Coating is applied to selected products for the following purposes:

- To act as a barrier for alpha-particle protection
- To reduce stress on die surface
- To provide additional moisture resistant barrier

10.0 Mold/Encapsulate

Quality and Reliability Program

The bonded products are molded to protect the dice and wires using low stress molding compound at $175^{\circ}\pm 5^{\circ}\text{C}$. X-ray, on the molded products, is routinely carried out to address wires sweep and internal package void

11.0 Back Mark

All products are marked on the back to maintain lot traceability and assembly location traceability.

12.0 Post Mold Cure

Molded and marked products are baked at $175^{\circ}\pm 5^{\circ}\text{C}$ for a minimum of six hours to ensure optimum plastic sealing.

13.0 Chemical Deflash

Products are subjected to heated M-pyrol to remove plastic bleed and flash on leads outside the package body. This step is necessary to ensure good lead finish coverage.

14.0 Dejunk/Trim/Form/ Derail

These steps remove mechanical flash between leads, cut off dambar from external leads, form the leads to specific shapes and singulate products into individual units. Packages outline are routinely measured to ensure that singulated units meet specified dimensions.

15.0 Lead Finish

All product leads are protected for corrosion by solder dip for through-hole packages and by solder plate for surface mount packages. Solder thickness measurements and solderability tests are routinely carried out to ensure the integrity of the soldering process.

16.0 External Visual 100% inspection

The finished products are 100% inspected for external mechanical and lead finish quality. All inspected lots are sampled per AQL method for lot acceptance.

17.0 Pre-burn-in Electrical Test

Every product is 100% electrically tested at $+25^{\circ}\text{C}$ to QSI data sheet specification or customer given specification.

18.0 Burn-In/ Dynamic

All plastic package products are burned-in at $+125^{\circ}\text{C}$ for a minimum of 16 hours.

19.0 Post Burn-In Electrical Test

All plastic package products are electrically tested to QSI data sheets or customer given specifications at $+70^{\circ}\text{C}$ minimum. The Percent Defective Allowable (PDA) is 5% maximum. All tested lots are 100% verified to ensure PDA is within limits.

20.0 Top Mark

All products are top marked with product type and date code

21.0 Final Visual Inspection

Quality and Reliability Program

Each product is 100% inspected for conformance to package specification.

22.0 QA Lot Acceptance

All final products are visually sampled and also electrically tested on a sample basis to comply with all AQLs.

All products are marked on the back to maintain lot traceability and assembly location traceability.

12.0 Post Mold Cure

Molded and marked products are baked at $175 \pm 5^\circ\text{C}$ for a minimum of six hours to ensure optimum plastic sealing.

13.0 Chemical Degas

Products are subjected to heated M-pyrol to remove plastic bleed and flash on leads outside the package body. This step is necessary to ensure good lead finish coverage.

14.0 Delint/Thinfilm Detail

These steps remove mechanical flash between leads, cut off damper from external leads, form the leads to specific shapes and singulate products into individual units. Packages outline are routinely measured to ensure that singulated units meet specified dimensions.

15.0 Lead Finish

All product leads are protected for corrosion by solder dip for through-hole packages and by solder plate for surface mount packages. Solder thickness measurements and solderability tests are routinely carried out to ensure the integrity of the soldering process.

16.0 External Visual 100% Inspection

The finished products are 100% inspected for external mechanical and lead finish quality. All inspected lots are sampled per AQL method for lot acceptance.

17.0 Pre-burn-In Electrical Test

Every product is 100% electrically tested at $+25^\circ\text{C}$ to OSI data sheet specification or customer given specification.

18.0 Burn-In Dynamic

All plastic package products are burned-in at $+125^\circ\text{C}$ for a minimum of 16 hours.

19.0 Post Burn-In Electrical Test

All plastic package products are electrically tested to OSI data sheets or customer given specifications at $+70^\circ\text{C}$ minimum. The Percent Defective Allowable (PDA) is 5% maximum. All tested lots are 100% verified to ensure PDA is within limits.

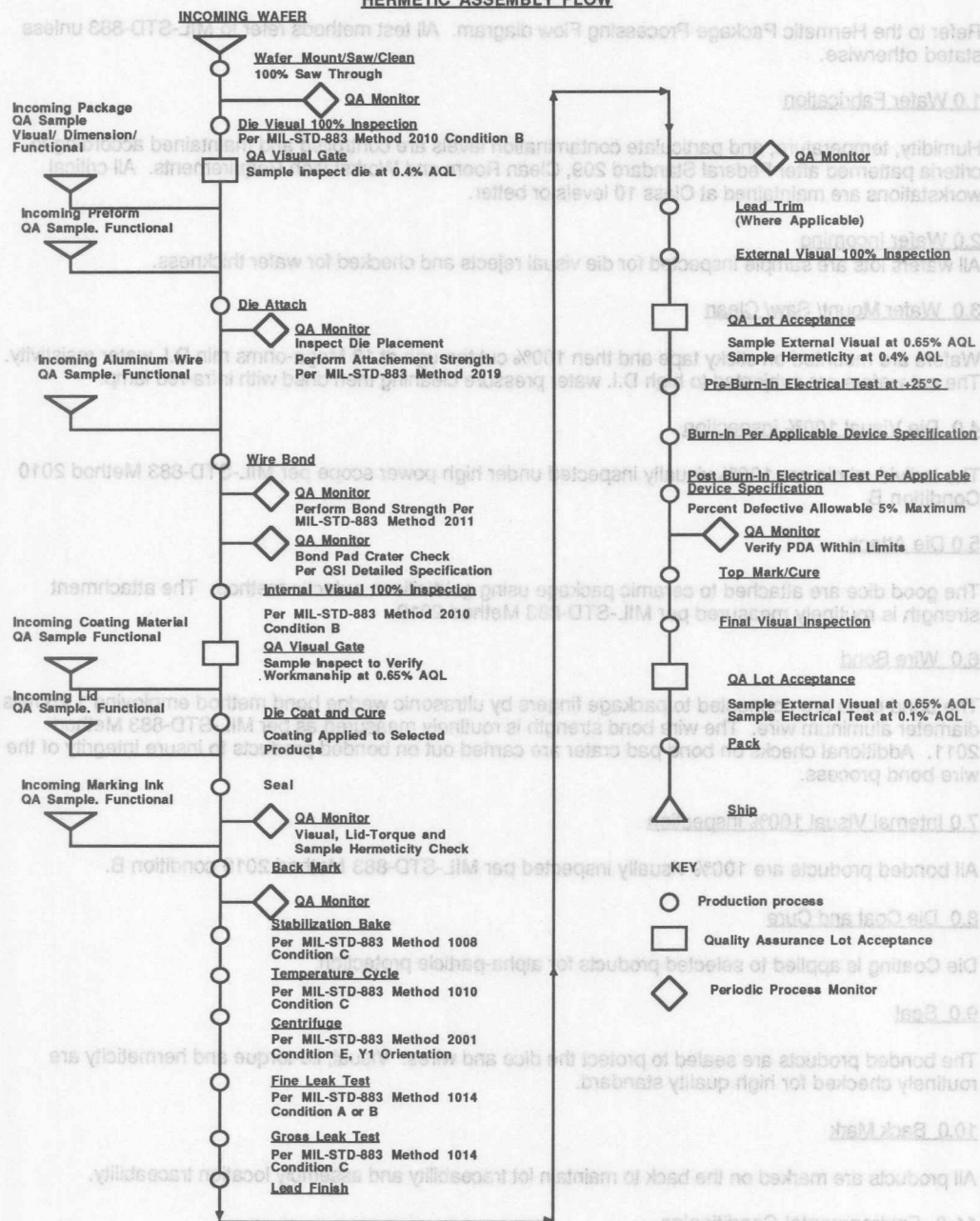
20.0 Top Mark

All products are top marked with product type and date code.

21.0 Final Visual Inspection

Quality and Reliability Program

HERMETIC ASSEMBLY FLOW



Hermetic Package Process Flow Summary

Quality and Reliability Program

Refer to the Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless stated otherwise.

1.0 Wafer Fabrication

Humidity, temperature, and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 10 levels or better.

2.0 Wafer Incoming

All wafers lots are sample inspected for die visual rejects and checked for wafer thickness.

3.0 Wafer Mount/ Saw/ Clean

Wafers are mounted on sticky tape and then 100% cut through at 12 Mega-ohms min D.I. water resistivity. The cut wafers are subjected to high D.I. water pressure cleaning then dried with infra-red lamp.

4.0 Die Visual 100% inspection

The individual die are 100% visually inspected under high power scope per MIL-STD-883 Method 2010 Condition B.

5.0 Die Attach

The good dice are attached to ceramic package using gold/silicon eutectic method. The attachment strength is routinely measured per MIL-STD-883 Method 2019.

6.0 Wire Bond

The bond pads are connected to package fingers by ultrasonic wedge bond method employing 1.25 mils diameter aluminum wire. The wire bond strength is routinely measured as per MIL-STD-883 Method 2011. Additional checks on bond pad crater are carried out on bonded products to insure integrity of the wire bond process.

7.0 Internal Visual 100% Inspection

All bonded products are 100% visually inspected per MIL-STD-883 Method 2010 condition B.

8.0 Die Coat and Cure

Die Coating is applied to selected products for alpha-particle protection.

9.0 Seal

The bonded products are sealed to protect the dice and wires. Visual, lid-torque and hermeticity are routinely checked for high quality standard.

10.0 Back Mark

All products are marked on the back to maintain lot traceability and assembly location traceability.

11.0 Environmental Conditioning

All sealed products are subjected to thermal and mechanical stress tests. This is to eliminate products with marginal die attach, wire bond or seal integrity.

Quality and Reliability Program

12.0 Hermetic Testing

All stress tested products are subjected to fine and gross leak tests to eliminate marginally sealed products or products whose seals may have become defective as a result of environmental conditioning tests.

13.0 External Visual 100% Inspection

The finished products are 100% inspected for external mechanical and lead finish quality. All inspected lots are sampled per AQL method for lot acceptance.

14.0 Pre-burn-in Electrical Test

Every product is 100% electrically tested at +25°C to QSI data sheet specification or customer given specification.

15.0 Burn-In/ Dynamic

All hermetic package products are burned-in per QSI applicable device specification.

16.0 Post Burn-In Electrical Test

All hermetic package products are electrically tested per QSI applicable device specification. The Percent Defective Allowable (PDA) is 5% maximum. All tested lots are 100% verified to ensure PDA is within limits.

17.0 Top Mark

All products are top marked with product type and date code

18.0 Final Visual Inspection

Each product is 100% inspected for conformance to package specification.

19.0 QA Lot Acceptance

All final products are visually sampled and also electrically tested on a sample basis to comply with all AQLs.

Quality and Reliability Program

Reliability Monitor Program

The Reliability Monitor Program is Quality Semiconductor procedure described under Quality Specification QARP-00001-00, which is available to customers upon request. This specification describes a procedure that provides for periodic reliability monitors to ensure all Quality Semiconductor products comply with established goals for improving reliability and minimizing reliability risks to our customers. The Reliability Monitor program is based on monitoring key products within each generic process family. This procedure requires that detailed failure analysis be performed on all test rejects and corrective action be taken as indicated by the analysis. A summary of the Reliability Monitor Program test and sampling plan is shown below.

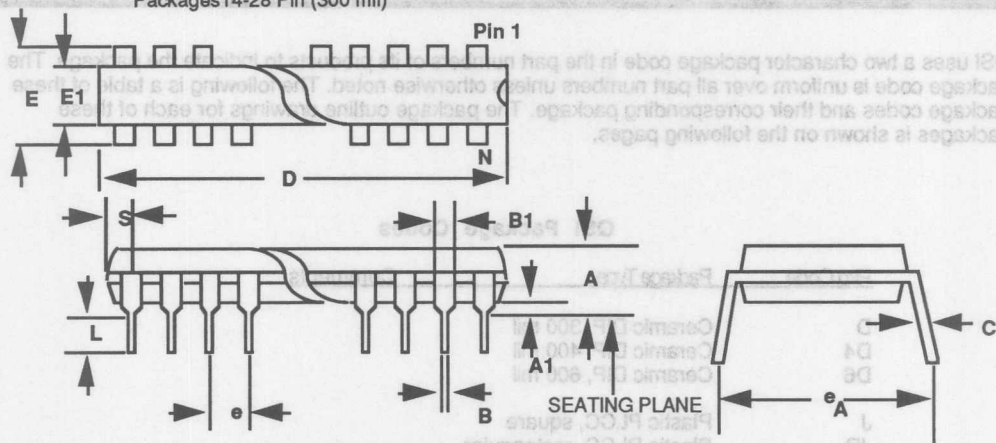
Reliability Monitor Program Sampling Plan

Test	Conditions	LTPD	Sample Size / Acceptance		Frequency
			Plastic	Hermetic	
Infant Mortality	160 Hours @ 125 °C/5.5V Dynamic burn-in	3	129/1	129/1	Monthly
Operating Life	1000 Hours @ 125 °C/5.5V Dynamic burn-in	5	105/2	105/2	Quarterly
Thermal Shock	100 Cycles: -65 °C to 150 °C, MIL-STD-883, Method 1011	5	105/2	105/2	Monthly
Temperature Cycle	100 Cycles: -65 °C to 150 °C, MIL-STD-883, Method 1010	5	105/2	105/2	Quarterly
Pressure Cooker	160 Hours @ 121 °C 15 PSI, Unbiased	3	129/1	NA	Monthly
85/85 Moisture, Biased	1000 Hours @ 85 °C, 85% Relative Humidity, Biased	5	105/2	NA	Quarterly

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Ceramic Dual In-Line
Packages 14-28 Pin (300 mil)

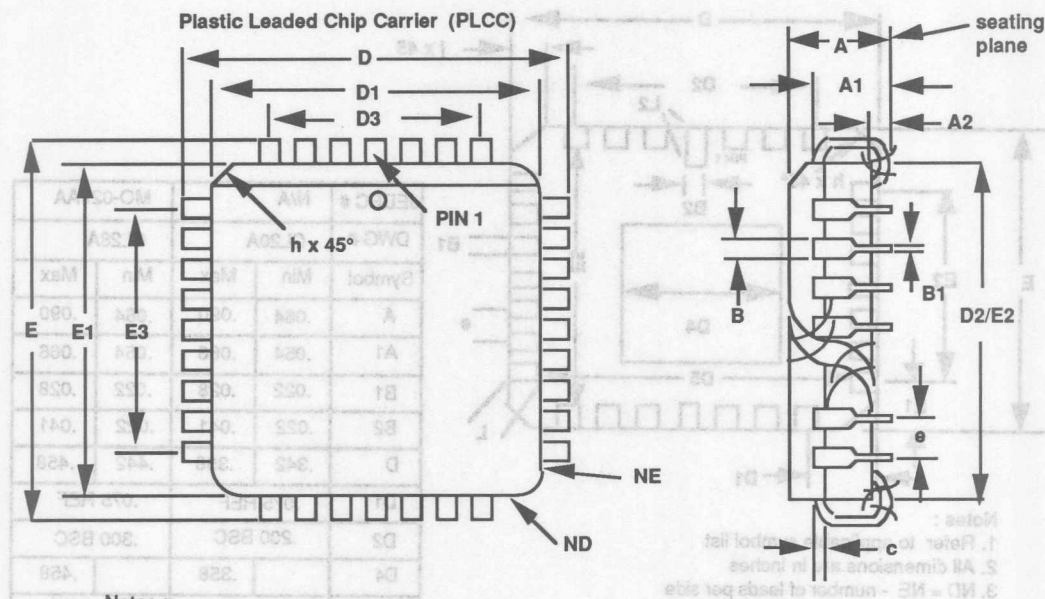


Notes: 1. Refer to applicable symbol list. 2. N is the maximum quantity of lead positions. 3. All dimensions are in inches. 4. Dimensions D and E1 are to be measured at maximum material condition.

JEDEC #	MO-036AC		MO-036AD		N/A		N/A		MO-058AA		MO-058AB	
DWG #	CD 14A		CD 16A		CD 20A		CT 22A		CT 24A		CT 28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.135	.175	.135	.175	.160	.200	.160	.200	.160	.200	.160	.200
A1	.025	.040	.025	.040	.015	.040	.015	.040	.015	.040	.015	.040
B	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020
B1	.045	.060	.045	.060	.045	.070	.045	.070	.045	.070	.045	.060
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012
D	.770	.810	.770	.810	.950	.990	1.060	1.100	1.240	1.280	1.440	1.480
E	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325
E1	.240	.290	.240	.290	.260	.310	.260	.310	.260	.310	.260	.310
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
e _A	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150
S	.070	.090	.025	.045	.025	.045	.030	.050	.070	.090	.070	.090
N	14		16		20		22		24		28	

Package Information

PLCC (Leadless Chip Carrier)



Notes :

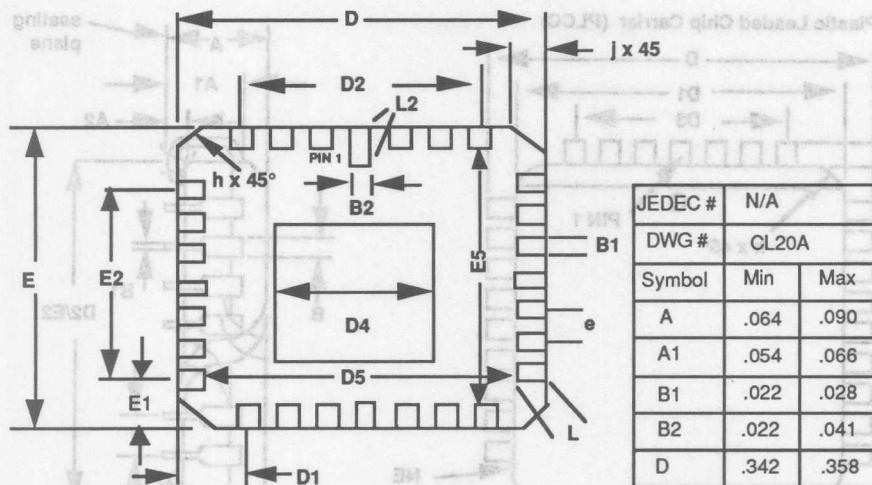
1. Refer to applicable symbol list
2. All dimensions are in inches
3. Dimensions D1 and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 inch per side
4. Lead coplanarity is 0.004 inch maximum.

JEDEC #	M0-052 AE		M0-047 AD	
DWG #	PL32A		PL52A	
Symbol	Min	Max	Min	Max
A	.115	.135	.165	.180
A1	.070	.090	.090	.120
A2	.015	.035	.015	.035
B	.026	.032	.026	.032
B1	.014	.019	.014	.019
C	.009	.012	.009	.012
D	.485	.495	.785	.795
D1	.448	.452	.750	.756
D2	.390	.430	.690	.730
D3	.300 REF		.600 REF	

JEDEC #	M0-052 AE		M0-047 AD	
DWG #	PL32A		PL52A	
Symbol	Min	Max	Min	Max
E	.585	.595	.785	.795
E1	.548	.552	.750	.756
E2	.490	.530	.690	.730
E3	.400 REF		.600 REF	
e	.044	.056	.044	.056
h	.042	.048	.042	.048
ND	7		13	
NE	9		13	

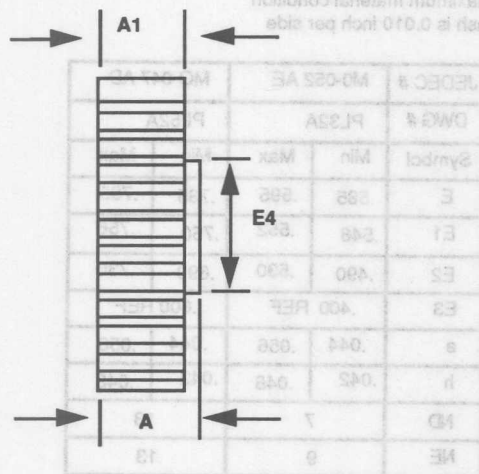
Package Information

Leadless Chip Carrier (LCC)



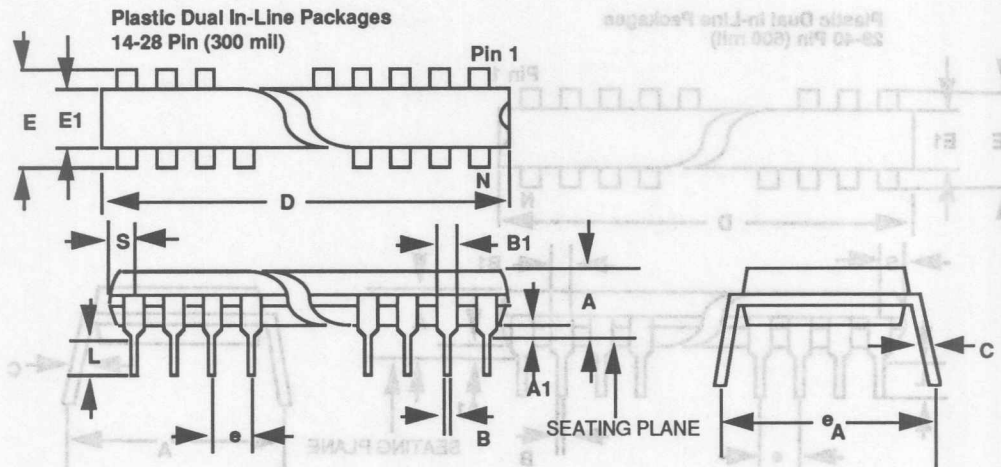
- Notes :
1. Refer to applicable symbol list
 2. All dimensions are in inches
 3. ND = NE - number of leads per side

JEDEC #	N/A		MO-027AA	
DWG #	CL20A		CL28A	
Symbol	Min	Max	Min	Max
A	.064	.090	.064	.090
A1	.054	.066	.054	.066
B1	.022	.028	.022	.028
B2	.022	.041	.022	.041
D	.342	.358	.442	.458
D1	.075 REF		.075 REF	
D2	.200 BSC		.300 BSC	
D4		.358		.458
D5	.250 REF		.350 REF	
E	.342	.358	.442	.458
E1	.075 REF		.075 REF	
E2	.200 BSC		.300 BSC	
E4		.358		.458
E5	.250 REF		.350 REF	
e	.050 BSC		.050 BSC	
h	.040 REF		.040 REF	
j	.020 REF		.020 REF	
L	.045	.055	.045	.055
L2	.077	.093	.077	.093
N	20		28	
ND	5		7	



Package Information

300 Mil PDIP



Notes:

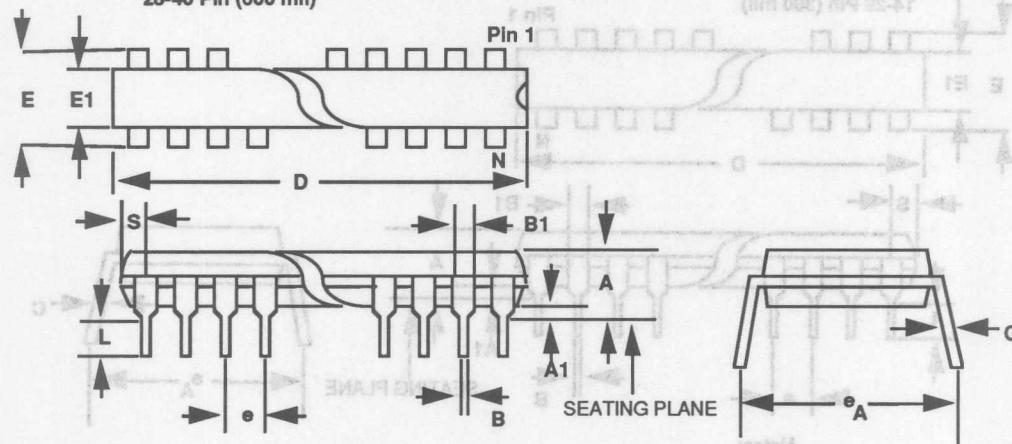
1. Refer to applicable symbol list
2. N is the maximum quantity of lead positions
3. All dimensions are in inches
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash.

JEDEC #	MS-001 AC		MS-001 AA		MS-001 AE		N/A		MS-001 AF		MO-095 AH	
DWG #	PD 14A		PD 16A		PD 20A		PT 22B		PT 24A		PT 28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.130	.170	.130	.170	.130	.170	.130	.170	.130	.170	.130	.180
A1	.015	.040	.015	.040	.015	.040	.015	.040	.015	.040	.015	.040
B	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020
B1	.045	.070	.045	.070	.045	.070	.045	.070	.045	.070	.045	.060
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012	.009	.012
D	.745	.765	.745	.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325	.300	.325
E1	.240	.270	.240	.270	.240	.270	.240	.270	.250	.280	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
e _A	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380	.310	.380
L	.120	.140	.120	.140	.120	.140	.120	.140	.120	.140	.120	.140
S	.070	.080	.020	.035	.060	.070	.010	.020	.025	.080	.020	.040
N	14		16		20		22		24		28	

Package Information

600 Mil PDIP

Plastic Dual In-Line Packages
28-40 Pin (600 mil)



Notes:

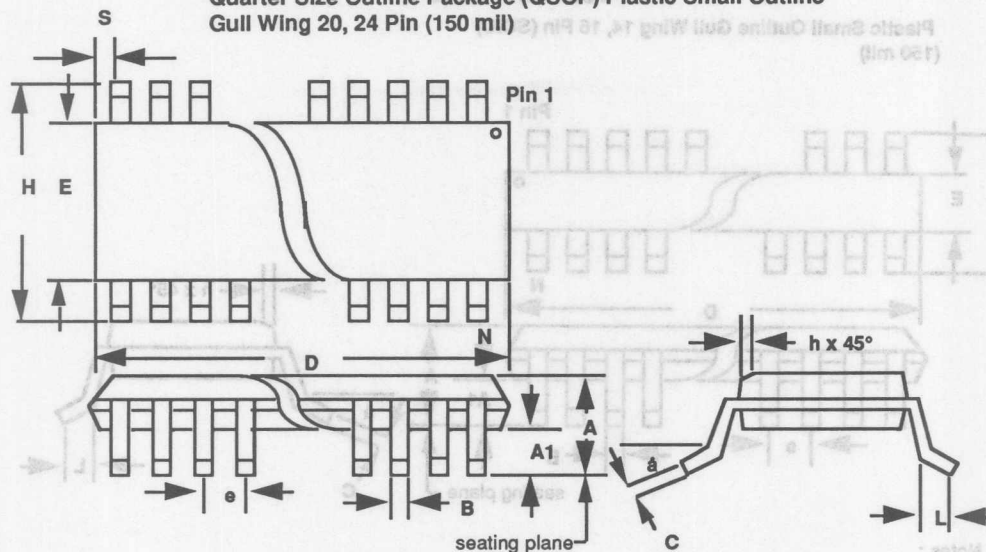
1. Refer to applicable symbol list
2. N is the maximum quantity of lead positions
3. All dimensions are in inches
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 inch per side.

material condition but do not include mold flash. Allowable mold flash is 0.010 inch per side.					
JEDEC #		MS-011 AB		MS-011 AC	
DWG #		PD 28A		PD 40A	
Symbol	Min	Max	Min	Max	
A	.150	.190	.150	.190	
A1	.015	.040	.015	.040	
B	.016	.020	.016	.020	
B1	.045	.070	.045	.070	
C	.009	.012	.009	.012	
D	1.440	1.460	2.050	2.070	
E	.600	.625	.600	.625	
E1	.530	.560	.530	.560	
e	.090	.110	.090	.110	
e _A	.610	.680	.610	.680	
L	.120	.140	.120	.140	
S	.070	.090	.070	.090	
N	28		40		

Package Information

150 MIL QSOP

Quarter Size Outline Package (QSOP) Plastic Small Outline Gull Wing 20, 24 Pin (150 mil)



JEDEC #	TBD			TBD		
DWG #	PSS-20A			PSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.0075	0.008	0.098	0.0075	0.008	0.098
D	0.337	0.342	0.346	0.337	0.342	0.346
E	0.150	0.155	0.157	0.150	0.155	0.157
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
α	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.060	0.031	0.033	0.035

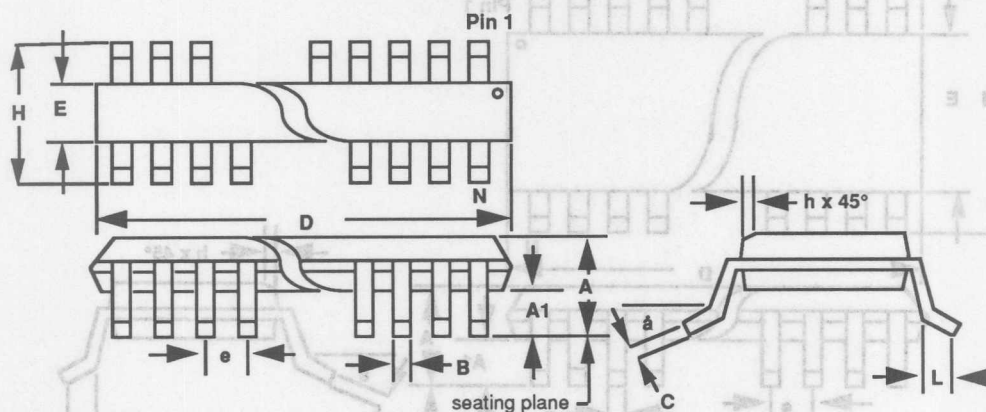
Notes :

1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.
5. Lead coplanarity is 0.004 inch max.

Package Information

150 Mil SOIC

Plastic Small Outline Gull Wing 14, 16 Pin (SOIC)
(150 mil)



Notes :

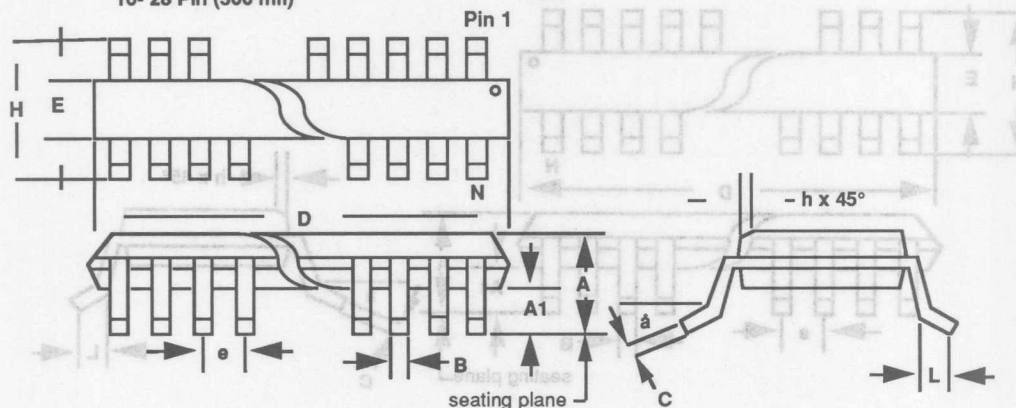
1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.
5. Lead coplanarity is 0.004 inch maximum

JEDEC #	MS-012AB			MS-013AC		
DWG #	PS-14B			PS-16B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.014	0.016	0.019	0.014	0.016	0.019
C	0.0075	0.008	0.009	0.0075	0.008	0.009
D	0.337	0.342	0.346	0.386	0.391	0.393
E	0.150	0.155	0.157	0.150	0.155	0.157
e	0.050 BSC			0.050 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035
N	14			16		
α	0°	5°	8°	0°	5°	8°

Package Information

300 Mil SOIC

Plastic Small Outline Gull Wing (SOIC)
16- 28 Pin (300 mil)

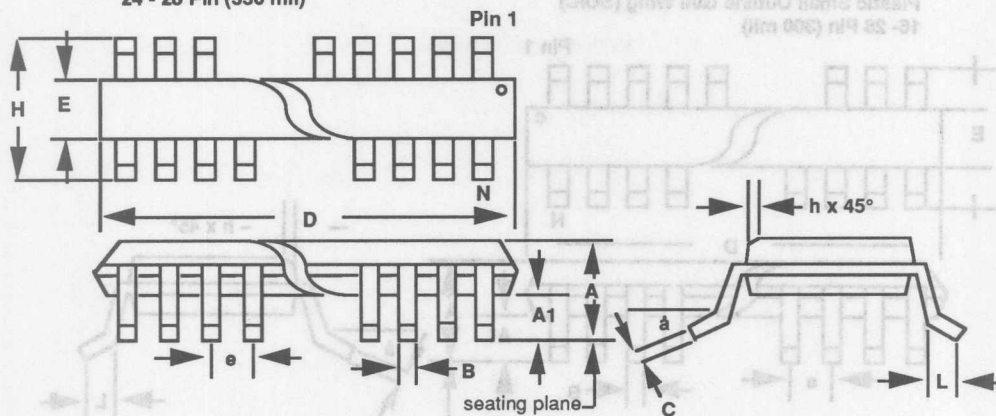


Notes :

1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.

JEDEC #	MS-013 AA		MS-013 AC		MS-013 AD		MS-013 AE	
DWG #	PS 16A		PS 20A		PS 24A		PS 28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	.096	.104	.096	.104	.096	.104	.096	.104
A1	.005	.011	.005	.011	.005	.011	.005	.011
B	.014	.019	.014	.019	.014	.019	.014	.019
C	.009	.012	.009	.012	.009	.012	.009	.012
D	.402	.412	.500	.510	.602	.612	.701	.711
E	.292	.299	.292	.299	.292	.299	.292	.299
e	.044	.056	.044	.056	.044	.056	.044	.056
H	.396	.416	.396	.416	.396	.416	.396	.416
h	.010	.016	.010	.016	.010	.016	.010	.016
L	.020	.040	.020	.040	.020	.040	.020	.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

Plastic Small Outline Gull Wing (SOIC)
24 - 28 Pin (330 mil)



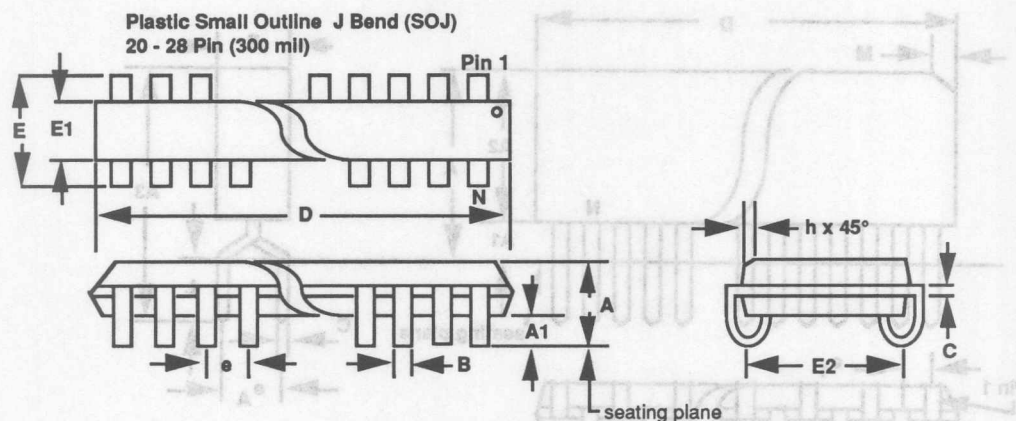
Notes :

1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.

JEDEC #	MO-059 AA		MO-059 AC	
DWG #	PS 24B		PS 28B	
Symbol	Min	Max	Min	Max
A	.080	.100	.080	.100
A1	.005	.014	.005	.014
B	.014	.020	.014	.020
C	.006	.010	.006	.010
D	.624	.634	.718	.728
E	.325	.335	.325	.335
e	.044	.056	.044	.056
H	.453	.477	.453	.477
h	.010	.030	.010	.030
L	.020	.050	.020	.050
N	24		28	
a	0°	8°	0°	8°

Package Information

300 Mil SOJ



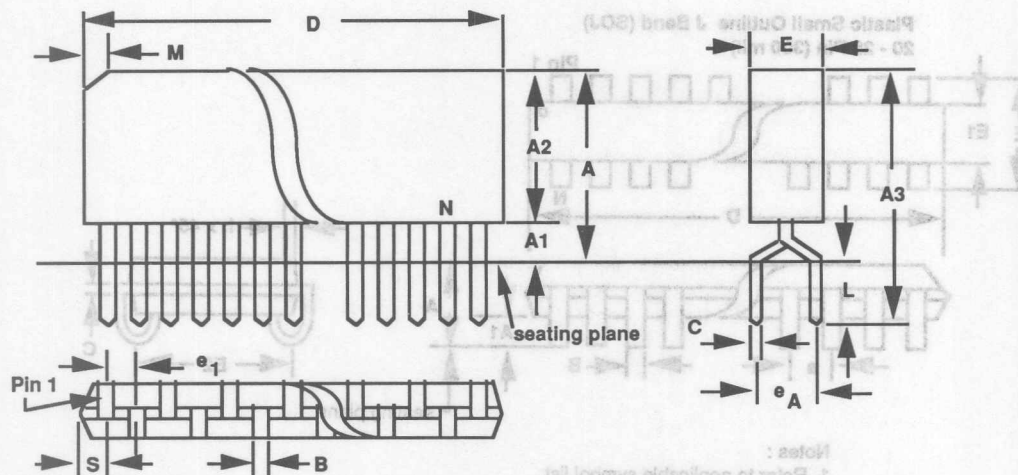
Notes :

1. Refer to applicable symbol list.
2. N is the maximum quantity of lead positions.
3. All dimensions are in inches.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 inch per side.

JEDEC #	MO-088 AD		MO-088 AE		MO-088 AF	
DWG #	PJ 20A		PJ 24A		PJ 28A	
Symbol	Min	Max	Min	Max	Min	Max
A	.120	.140	.120	.140	.120	.140
A1	.025	.045	.025	.045	.025	.045
B	.014	.019	.014	.019	.014	.019
C	.009	.012	.009	.012	.009	.012
D	.502	.512	.602	.612	.701	.711
E	.336	.347	.336	.347	.336	.347
E1	.292	.299	.292	.299	.292	.299
E2	.262	.272	.262	.272	.262	.272
e	.044	.056	.044	.056	.044	.056
h	.010	.016	.010	.016	.010	.016
N	20		24		28	

Package Information

16-24 Pin PZIP



- Notes:**
1. Refer to applicable symbol list.
 2. N is the maximum quantity of lead positions.
 3. All dimensions are in inches.
 4. Dimensions D and A2 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 inch per side.

JEDEC #	MO-054AA		MO-072AB		MO-072AC	
DWG #	PZ 16A		PZ 20A		PZ 24A	
Symbol	Min	Max	Min	Max	Min	Max
A	.290	.350	.350	.400	.350	.400
A1	.060	.100	.030	.070	.030	.070
A2	.250	.270	.280	.340	.320	.350
A3	.390	.500	.450	.550	.450	.550
B	.015	.024	.015	.024	.015	.024
C	.008	.012	.008	.012	.008	.012
D	.786	.814	1.008	1.030	1.200	1.250
E	.100	.120	.100	.120	.100	.120
e1	.050 BSC		.050 BSC		.050 BSC	
eA	.100 BSC		.100 BSC		.100 BSC	
L	.100	.150	.100	.150	.100	.150
M	.035	.085	.035	.085	.035	.085
N	16		20		24	
S	.018	.032	.018	.032	.018	.032